Mechanism and Application of NMOS Leakage with Intra-Well Isolation Breakdown by Voltage Contrast Detection

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***Abstract*—An innovative application of voltage-contrast (VC) inspection allowed inline detection of NMOS leakage in dense SRAM cells is presented. Cell sizes of SRAM are continual to do the shrinkage with bit density promotion as semiconductor technology advanced, but the resulting challenges include not only development of smaller-scale devices, but also intra-devices isolation. The NMOS leakage caused by the underneath n+/P-well shorted to the adjacent PMOS/N-well was inspected by the proposed electron-beam (e-beam) scan in which VC images were compared during the in-line process step of post contact tungsten (W) CMP (Chemical Mechanical Planarization) instead of end-of-line electrical test, which has a long response time. A series of experiments based on the mechanism for improving the intra-well isolation was performed and verified by the inline VC inspection. An optimal process-integration condition involved to the tradeoff between the implant dosage and photo CD was carried out.**

***Index Terms*—Voltage contrast, e-beam inspection, intra-well isolation, defect inspection, NMOS leakage**

I. INTRODUCTION

SRAM is the priority vehicle for technology development and process line monitoring because its end-of-line logical failure bins can address to the location of in-line physical defects for analysis [1]. As the rapid advance of semiconductor technology, SRAM is continual to do the shrinkage, reduce cell size and promote the bit density. The shrinking geometrics such as poly and active area sizes are noted as the key dimensions. However, invisible shapes such as N/P-well, source and drain are rarely discussed for inline measurements. At nanometre technology node, these implant process-related invisible profiles are increasingly important since it is difficult for immediate measurement during the process but does affect the end-of-line device performance.

An e-beam scan with VC images comparison is an effective inspection method and a good alternative to bright and dark field ones as tolerance of defects in the semiconductor process decreases [2]. With the scanning electron microscope (SEM) image observation, VC inspection able to detect tiny defects nonvisual to optical inspection [3], furthermore, the under layer defect is possible to be found by the surface charging [4]. Some applications even use dedicated test structures [5] for VC inspection as a routine monitoring vehicle to sweep the line defects. Advanced semiconductor process line inclines to require more e-beam scans, especially for the early phase of technology development [6]. The small wavelength of electron beams presents superior resolution that able to inspect sub-design rule defects in nanometre-scale process [7]. Although the low throughput usually is the cost of the high-resolution e-

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beam inspection, the smart sampling scan can be applied for dedicated defect cases [8]. Usual cases of those applications are aimed at detecting physical defects, either very small defects on the surface or the open/ short ones under the surface. The study herein further extends VC inspection to detect the leakage, one key electrical parameter of the device; moreover, the surface VC charging by electron signal observed is from the deep bulk silicon and related to the shapes of N/P wells.

In this paper, a methodology allowed inline detection of NMOS leakage of the SRAM by VC inspection is described. The mechanism of the leakage defect was analyzed and verified by changing the implant conditions and by performing an inline VC inspection. The methodology was used during advanced technology developments, which require cycles of evaluating wafer runs to figure out the correct path. Insteading of end-of-line electrical tests, the methodology provides a tremendous speed advantage for evaluating split experiments and hence shortens the development period for yield ramping up. After performing a series of splits to reduce NMOS leakage, the optimal process integration conditions involved the implant dosage and photo CD was carried out.

The contents and highlights of the study are breakdown into the 5 points below.

(1) The first presentation of intra-well isolations monitoring by e-beam inspection.

(2) The inline detection instead of end-of-line electrical tests gained time advantage.

(3) One of the current most advance e-beam inspection tools used herein.

(4) A close loop solution with robust process was achieved.

(5) The methodology would apply to the next technology nodes.

II. In-line Voltage Contrast Inspection

1. Scan Step

Front-end-of-line (FEOL) process used for fabricating CMOS device features,, however, the most right scan step for the VC inspection is at MEOL (middle-end-of-line), post W CMP of contact layer. In the process step of post contact W CMP, the each W conducting plug separated by oxide insulating film surrounding and landed to the different region of the device such as source/drain and poly gates either in N or PMOS, which constructs a pure metric condition to VC inspection. For conventional six-transistor SRAM, the three different landing groups of W plus connections are P+/N-well in PMOS, N+/P-well in NMOS and poly gates. Since each group has unique electrical characteristic, the VC image presents different gray level. The feature is just right for VC inspection.

2. SRAM Structures with Voltage Contrast

The four structures of the six-transistor SRAM proposed to be inspected is shown in Fig. 1. The first structure is a shared contact landed on both P+/N-well and poly gate, which was used to improve the bit density and integration of SRAM. The second, third and fourth structures are the contacts connected to P+/N-well, N+/P-well and poly gate, respectively. Using the positive charging mode of electron beam inspection, either bright or dark VC image can be detected as the schematic top view of Fig. 1. In the prior two structures,(Fig. 1(1)(2)) electrons in the N-well of bulk silicon are ejected through P+ region to the top of the W plug and appear as a bright VC image; on the other hand, electrons intrinsically cannot be ejected from P to N, and the third structure, as shown in Fig. 1(3), with connection of P-well and N+ in

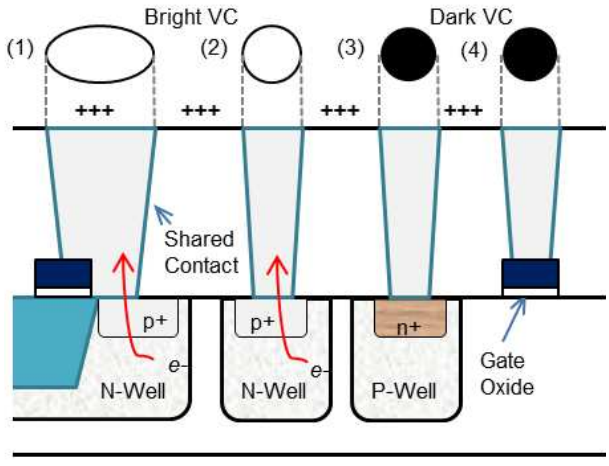

Fig. 1. Schematic cross section of the four structures of SRAM by the categories of VC inspection. The top view of the W plugs showed bright or dark VC by the positive charging mode of electron beam inspection. The dimensions are not drawn to scale.

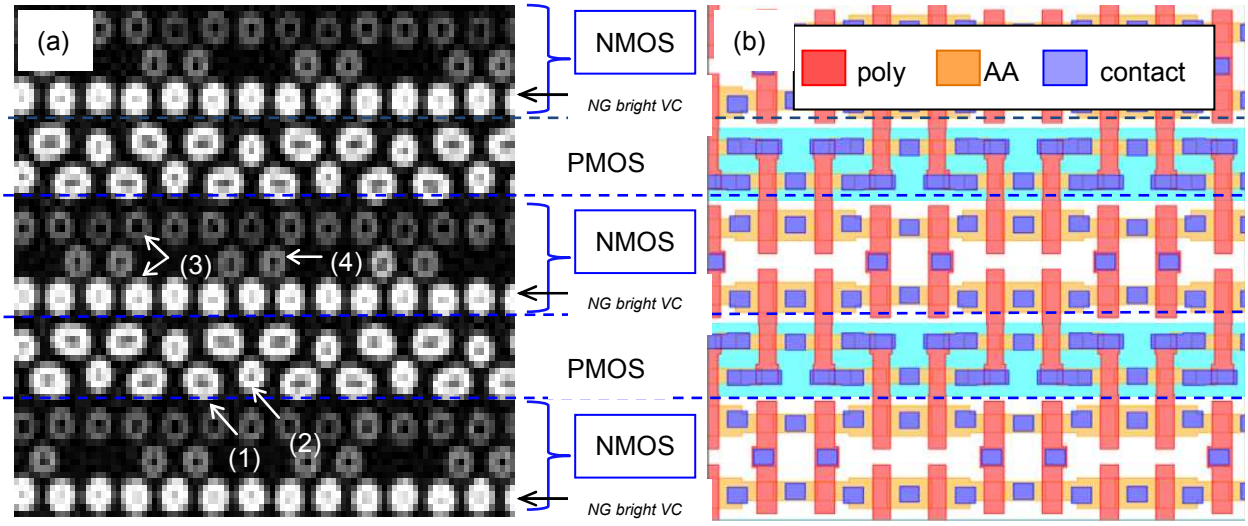

Fig. 2. (a) Top views of SEM with VC for the NMOS leakage, contact W plug landed at (1) shared contact, (2) P+/N-well in PMOS and (3) N+/P-well (4) gate poly in NMOS. (b)Layout of the under layers, poly, contact, and active area (AA).

bulk silicon therefore has fewer electrons reached to the top and showed dark VC. Similarly, Fig. 1(4) shows that, in the fourth structure, the gate oxide cuts off the bulk-to-top path of the electrons and results in a dark VC.. Those structures and corresponding VC conditions above are with correct and uniform process; in reverse, the VC inspection of those structures able to capture the process variation or defect happened.

3. NMOS Leakage

The normal VC image for NMOS is dark, however, an abnormal row of bright VC was found as shown in Fig. 2. A dark VC indicates an underlying open loop while a bright VC is short that electrons able to go out from the bottom bulk silicon to the top. The structure of NMOS is either N+/P-well or gate as open loops for electrons, thereby showing dark VC. The row of bright VC in NMOS is leakage of the device, which results in a failure in the end-of-line electrical test. The location of the NMOS leakage (layout in Fig. 2(b)) is the contact with active area (AA) just against the PMOS. Besides, the defects only appear on one side even though the two sides of the NMOS structure are symmetrical. No physical difference can be found by the comparison between good and no-good structures; even high resolution TEM (tunneling electron microscopy) was adopted. The cross-section cuts of TEM showed very correct of the physical sizes regarding the interface of the inter-connection and geometrical scale of the structure, but they cannot reveal those incorrect shapes of N/P-wells profiles just being the root cause of the leakage. Leakage caused by improper N/P-wells shapes is further described below.

4. Retrograde Well Implants

High-energy ion implanters are often used for deep well formation and the intra-well isolation becomes an issue as device scaling down. The Retrograde well involves several steps of implants with energy varied from high to low, corresponding to the implant depth from deep bulk to near the surface. The deep-depth implants with high energy provides anti-punch-through (APT) and channel stop while a near-the-surface implant with low energy provides threshold voltage adjustment.

The high-energy implants are often done at a tilt angle since <001> axial channeling occurs for 0° implants. The tilt angles cause a lateral offset of the dopant and shadowing; in contrast, a zero degree implant reduces process robustness by causing channeling-induced profile variations. The practical manufacturing adopts tradeoff with a small tilt angle close to zero.

The shadowing from photo resist features is unavoidable once with tilt implant, and besides lateral offset of the other side against the shadowing may affect the adjacent well. The intra-well isolation therefore could be broken following the shrinkage of the device but stay

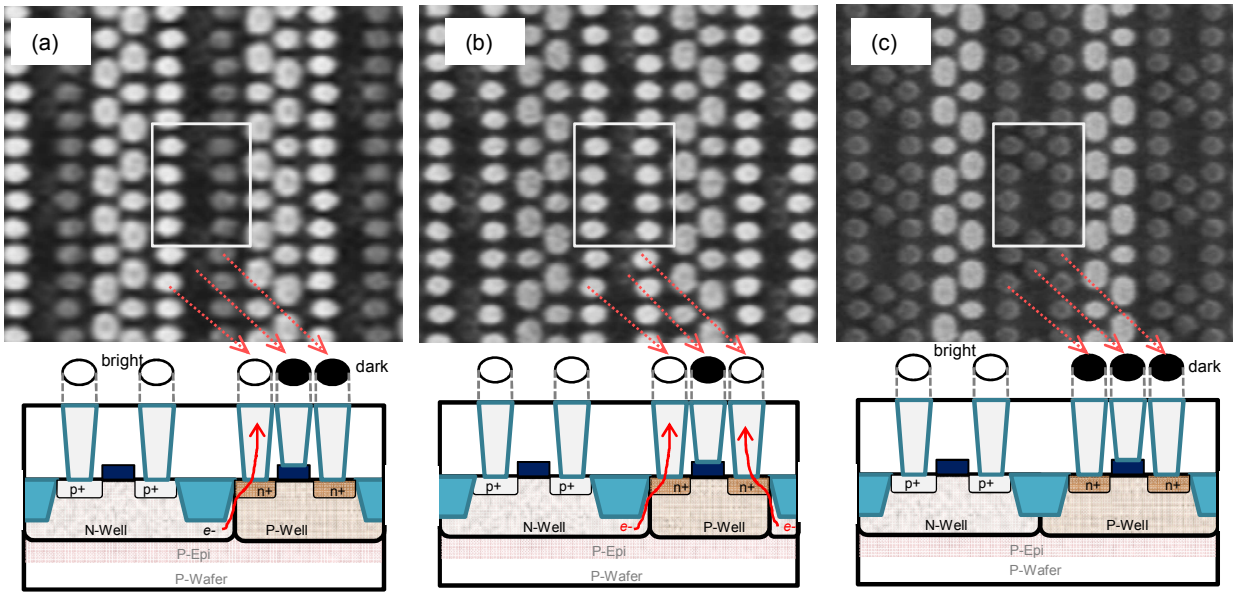

Fig. 3. The intra-well isolation broken by improper shapes of the adjacent N- and P-well profiles (a) one, (b) two colums of bright VC defects indicated NMOS leakage by the shortage of source/ drain and adjacent N-wells, (c) the norma/ darkl VC of NMOS without leakage.

the same tilt angle of the implant. A true zero-degree implant without shadowing substantially improves intra-well isolation; however, the channeling increases vertical profile variations.. This study showed that interacting effects of intra wells can be controlled by adjusting the photo resist CD (critical dimension), the tilt angle and the implant dosage.

5. Intra-well Isolation

The broken of intra-well isolation was found at the proposed e-beam scan step, post contact W CMP. Fig. 3(a) shows one column of bright VC in NMOS caused by the underlying n+/ source or drain shorted to the adjacent PMOS/ N-well. Electrons flow from PMOS/ N-well through n+/ source or drain of NMOS to the top surface resulted in bright VC. Fig. 3(b) shows an even more severe case, in which both source and drain of the NMOS are shorted, thereby showing two columns of bright VC. Fig. 3(c) shows the normal reference condition with bright and dark VC on PMOS and NMOS, respectively. The schematic cross section below shows satisfactory intra-well isolation and a satisfactory shape of deep well profiles.

Fig. 4. illustrates the implant process for deep well formation. Here, “implant tilt angle”, “dosage”, “PR thickness” and “PR space CD” are directly related to the process robustness. Excluding thermal budget and ion diffusion, tradeoff conditions between process requirement and precise control of deep wells formation with isolation are shown below.

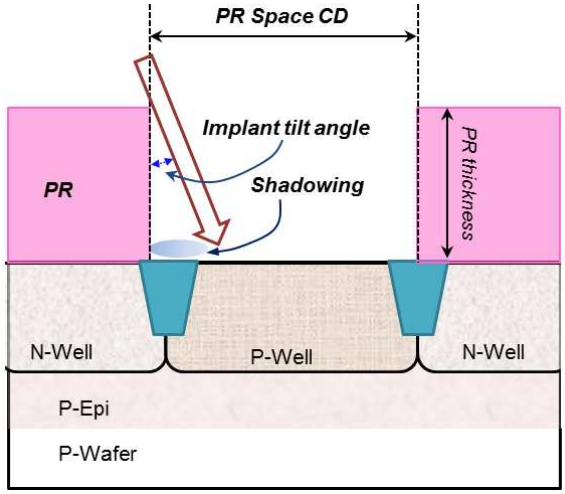

Fig. 4. Schematic cross section of the deep well implant with “tilt angle”, “shadowing”, “PR thickness” and “PR Space CD”.

(1) A smaller tilt angle of the implant can have less lateral offset. However, the tilt angle more closer to zero would lead to worse channeling with diffused distribution.

(2) Less PR (photo resistor) thickness would reduce

the shadowing by tilt implants. However, the PR still require at least enough thickness to block the implant bombardment.

(3) A smaller dosage would prevent the ion dose diffused everywhere at the subsequent thermal process. However, the dosage must be comparable with each other and adequately molds the characteristics of the devices.

(4) The PR CD (critical dimension) of N-/P-wells compromised with a large process window gained. The regions of the device does not have physical features and borders but can be referred to the open space of implant mask layers, in which, SRAM N-/P-wells space region are reversed to each other. Even mask layouts defined the regions of N-/P-well, it can be adjusted by varying PR CD.

III. EXPERIMENTS AND RESULTS

1. Equipment

The e-beam inspection system of HMI 315xp designed for 45 nm technology node was used to inspect the VC defect in the research. The machine was operated at a positive mode with electron yield >1, and a positive surface charge results from the greater number of electrons leaving the surface compared to those reaching the surface. The NMOS leakage can only be detected by the positive mode; in contrast, the negative mode [9, 10] would miss it. To achieve a high resolution and signal-to-noise during VC detection, the parameters of the inspection recipe content low landing energy with 500-V, high beam current with 100-nA, and small pixel size with 50-nm. The subsequent SEM review step is needed after the inspection to determine the precise features of the reported defects. However, the review step can and better be performed on HMI 315xp as well. Otherwise, some VC defects may be undetectable by standard review SEM tools. The reason for e-beam inspection reported defects becomes invisible under review SEM is because of the different designs of their electron-gun columns; *e. g.* the beam current of HMI 315xp is ten times higher than that of usual SEM tools.

2. Quad Implants with A Very Small Tilt Angle

The initial implant process for deep N-/P-wells used a conventional way done at a 7 degree tilt angle without wafer repositioning for the two high-energy implants of retrograde wells. Revering to Fig. 3(a), however, the one column in either source or drain found leakage with bright VC, which indicates only one side of the NMOS abnormal. The cause of the asymmetric pattern is from the tilt angle resulting in shadowing, and two direct measures then were experimented accordingly. The tilt angle was reduced from 7 to 2 degrees to minimize the shadowing. Then the quad implant, four equal dose implant segments with one quarter wafer rotation per segment used, was instead of the one shot process. The quad implant provides even dosage to vertical and horizontal couples of the wafer, but the drawback obviously is the almost four-fold increase in process time and the reduced throughput. The asymmetric pattern of the NMOS finally was fixed, however, the result trended to worse actually. The NMOS bright VC defects overspread from one to two columns as shown in Fig. 3(b).

The quad implants with a very small tilt angle did improve the process uniformity without asymmetric patterns but was clearly insufficient for preventing NMOS leakage. Additional process changes with split conditions are introduced and evaluated in the next section.

3. Split Experiments

Since the NMOS leakage was caused by the overly diffused PMOS/N-well shorted to N+ S/D, the area for deep well implants and resulting changes in well shapes were adjusted to reduce the defects. The regions of SRAM N- and P-wells are complementary; *i.e.,* one shrinks while the other expands. The P-well line CD has the same trend with N-well space CD, and *vice versa*. Therefore, additional split experiments of PR CD for N-/P-wells were performed. Besides, the dosages of the two-step retrograde well implants were considered into the splits as well. The experimental wafers were firstly done lithography splits within the wafer. The focus or energy of the lithography recipes varied one by one from the total 61 shots as shown in Fig. 5(a). As a result, the PR CD would vary accordingly and be measured within each shot of the whole wafer. Secondly, the dosages of implant I and II differed in each wafer. Implant I and II with the top-two highest energy decide the profile of

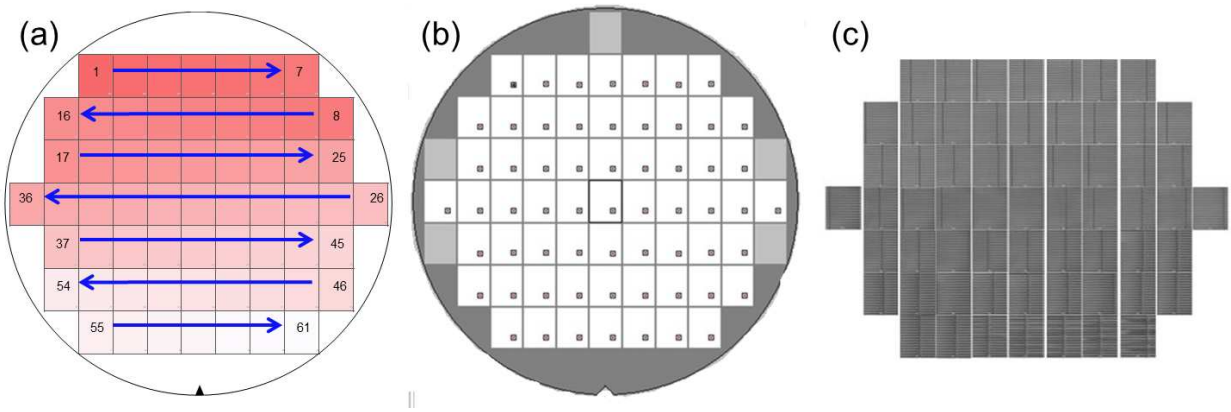

Fig. 5. Methodology of the PR CD split with e-beam scan (a) 61 sequence shots with various PR CD, (b) the fixed location of each die inspected by e-beam scan, (c) the corresponding 61 SEM images of the locations.

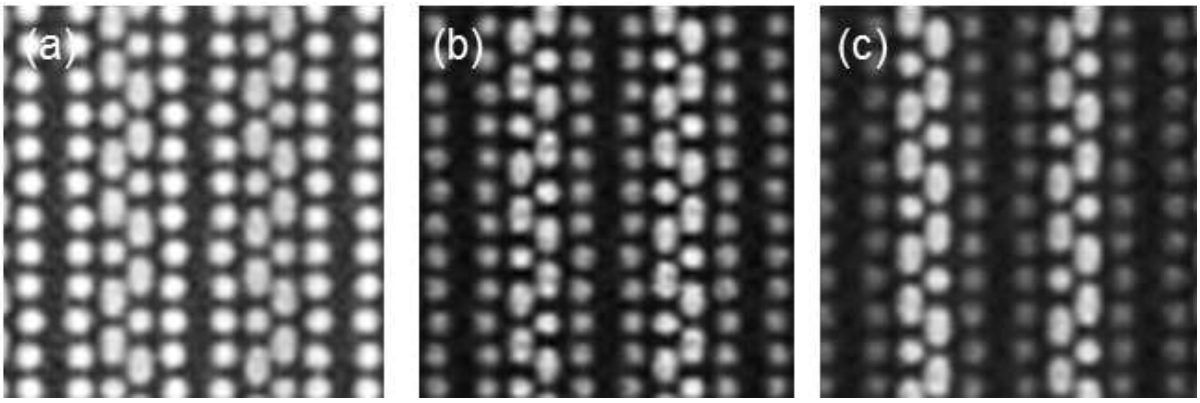

Fig. 6. SEM images with worse bright trend to normal dark VC of the NMOS following the PR CD changing (a) very bright VC of NMOS as bright as PMOS, (b) mild bright VC of NMOS, (c) normal VC of NMOS and PMOMS with dark and bright, respectively.

deep wells, and the recipe combination greatly affect to the intra-well isolation. In the split summary of photo and implant modules, each wafer has its own conditions combined with implant I and II; each shot also has its own PR CD within the whole wafer.

Subsequent processing of the batch of experimental wafers completed the FEOL physical geometries and characteristics of devices, till the MEOL step of post contact W CMP. Finally, e-beam scan was used to verify the NMOS leakage with bright VC defects. Fig. 5(b) shows that a fixed location of each shot was chosen for the scan, and Fig. 5(c) shows the corresponding SEM pictures. The VC status of the each SEM represents availability of each shot with the corresponding split condition. In Fig. 6, magnified SEM images clearly show two-column bright VC defects (see Fig. 6(a)) becomes mild (see Fig. 6(b)) and even normal dark (see Fig. 6(c)) eventually. The CD of the shot firstly has preferred dark VC with the implant split conditions of the wafer.

4. Results

By the methodology, the biggest "P-well line CD" available to normal dark VC was record for each split wafer, and the summary turns into Fig. 7. Totally, twelve wafers contented three implant I and four implant II conditions (see I, II, III and (I), (II), (III), (IV) in Fig. 7), and in which the dosage of each of the implant trends high as the sequence. Fig. 7(a) shows higher implant II dosage allowed bigger P-Well line CD within the 3 implant I groups. After swapping the sorting of implant I and II, Fig. 7(b) shows an even stronger trend that the allowed line CD all the way up as the sequence as the dosage increased. Therefore, either a heavy dosage, especially for implant II, or a small line CD with a large area of P-well can insulate itself from the affection of adjacent wells. According to the result combined with the

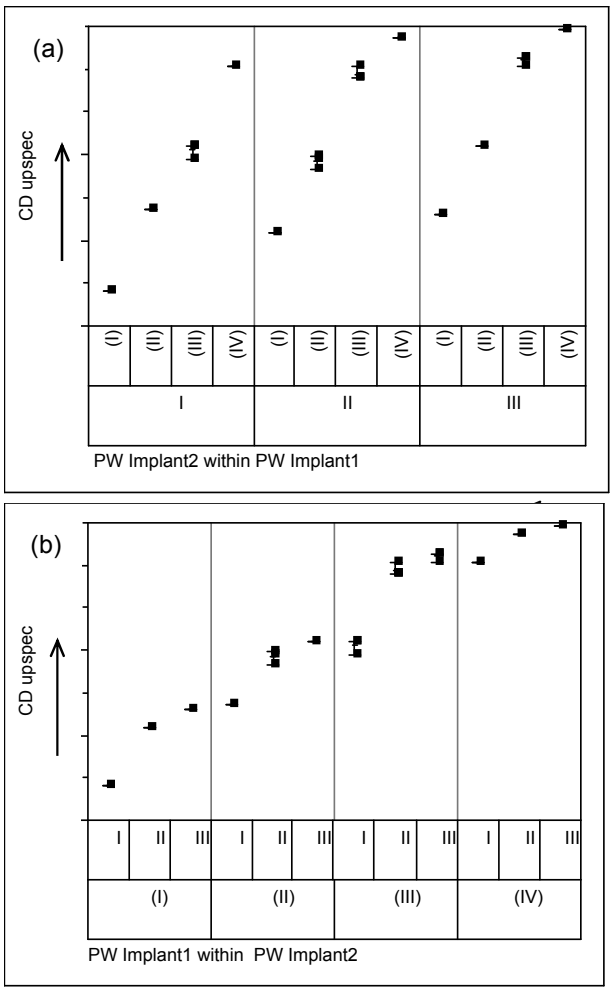

Fig. 7. The charts of implant conditions versus PR CD allowed with normal VC of NOMS. Higher dosages as the sequence of both (a) PW implant II within I, (b) PW implant I within II allowed higher PR CD; in which, II compared to I has more significant contribution to allowed CD.

requirement of device characteristics, the conditions of PW implant I and II were modified to retain intra-well isolation.

The mechanism and experiments also extended to other layers and eventually have an optimal combination of integration recipes with large process window gained. Even when process drift occurred, *e.g.* PR CD varied, the NMOS leakage never happened again.

IV. CONCLUSIONS

A methodology was proposed for using VC inspection to verify NMOS leakage of the SRAM regarding to the integrality of implant process. The mechanisms of NMOS leakage caused by broken intra-well isolation as SRAM scaling was explored and demonstrated. A series of experiments, involving tilt angles, wafer reposition, dosages of the implants and CD of the lithography, were performed and inspected by the e-beam scan, which was done within fab process instead of end-of-line electrical tests. The methodology enabled inline verification and substantially reduced the time required for the split experiment evaluation, and the cycle runs turned out a just right process integration condition with a large process window. The NMOS leakage is only one example of early detection by inline VC inspection. The inspection can be extended to other applications of semiconductor technology as the line width continually shrinking.

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