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Sub-0.1µm MOSFET의 게이트전압 종속 캐리어 속도를 위한 정확한 RF 추출 방법

(Accurate RF Extraction Method for Gate Voltage-Dependent Carrier Velocity of Sub-0.1µm MOSFETs in the Saturation Region)

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요 약

Sub-0.1µm로 스케일이 감소함에 따라 기생 저항 효과가 크게 발생되는 dc Ids 측정 데이터 없이 측정 S-파라미터로부터 얻 어진 RF Ids를 사용하여 벌크 MOSFET의 포화영역에서 게이트 전압 종속 유효 캐리어 속도를 추출하는 새로운 방법이 개발 되었다. 이 방법은 바이어스 종속 기생 게이트-소스 캐패시턴스와 유효 채널 길이의 복잡한 추출 없이 포화영역의 유효 캐리 어 속도를 추출할 수 있게 한다. 이러한 RF 기술을 사용하여 벌크 포화 속도를 초과하는 전자 속도 overshoot 현상이 0.065µm 게이트 길이의 벌크 N-MOSFET에서 관찰되었다.

Abstract

A new method using RF Ids determined from measured S-parameters is proposed to extract the gate-voltage dependent effective carrier velocity of bulk MOSFETs in the saturation region without additional dc Ids measurement data suffering parasitic resistance effect that becomes larger with continuous down-scaling to sub-0.1µm. This method also allows us to extract the carrier velocity in the saturation region without the difficult extraction of bias-dependent parasitic gate-source capacitance and effective channel length. Using the RF technique, the electron velocity overshoot exceeding the bulk saturation velocity is observed in bulk N-MOSFETs with a polysilicon gate length of 0.065µm.

Keywords: MOSFET, CMOS, RF, carrier velocity, device modeling, S-parameter, parameter extraction

I. INTRODUCTION

As successful down-scaling of channel length is continued below 0.1μ m for MOSFETs, accurate values of experimentally determined effective carrier velocity v_{eff} in the saturation region are very important to determine the intrinsic speed and carrier transport

behavior in the channel region. Generally, the gate-voltage dependent v_{eff} is extracted by the following equation^[1]:

$$v_{eff} = \frac{I_{ds}}{WQ_{in}}$$

$$= \frac{I_{ds}}{W\int_{0}^{V_{gs}} C_{gsd}'(V_{gs}')dV_{gs}'}$$

$$= \frac{I_{ds}}{\int_{0}^{V_{gs}} [C_{gsd}(V_{gs}')/L_{eff}]dV_{gs}'}$$
(1)

where L_{eff} is the effective channel length, W is the

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channel width and C_{gsd} '(= C_{gsd} /WL_{eff}) is the gate-source-drain capacitance between gate and tied source and drain at Vds=0V per unit channel area. However, the measurements of C_{gsd} at V_{ds}=0V using a very long-channel test device lead to velocity extraction errors, because the actual incremental charge dQin in the saturation region becomes smaller than that of $C_{gsd}dV_{gs}$ at V_{ds} =0V. An another method using dQ_{in} at high V_{ds} is reported^[2], but dQ_{in} nomalized by Cox is still overestimated where Cox is the oxide capacitance per unit channel area. Recently, a novel method^[3] using g_{mi}/(WC_{gsi}') = g_{mi}/K at high V_{ds} where g_{mi} is the intrinsic transconductance, C_{gsi} is the intrinsic gate-source channel capacitance per unit channel area, and K is the slope of the plot of C_{gs} versus L_{poly} is reported to avoid the errors in the traditional ones. However, this method produces the local carrier velocity at the point in the channel where $\partial v_{eff} / \partial V_{gs} = 0$ ^[1,2].

The carrier velocity extracted from $g_{mi}/(WC_{gsi}')$ is overestimated when $\partial v_{eff}/\partial V_{gs}>0$ because $g_{mi}/(WC_{gsi}') = v_{eff} + (Q_{in}/C_{gsi}')(\partial v_{eff}/\partial V_{gs})$ obtained by differentiating (1) in terms of $V_{gs}^{[2]}$. Thus, the best way to extract the average carrier velocity in the saturation region is to use $I_{ds}/(WQ_{in})$ at high V_{ds} directly.

It is well known that the measured dc I_{ds} is degraded by the reduction of internal V_{gsi} due to the potential drop between source resistance of MOSFETs. This degradation may be negligible in typical submicron MOSFETs, but it becomes much larger due to the increase of I_{ds} per unit width as channel length is scaled down to the sub-0.1 μ m regime. Thus, the previous methods^[1-2] using $I_{ds}/(WQ_{in})$ lead to underestimated extraction of v_{eff} due to a degraded dc I_{ds} value in sub-0.1 μ m devices.

Thus, in this paper, a new RF method based on the removal of the $I_{\rm ds}$ degradation effect using measured S-parameters is proposed to extract the effective carrier velocity of actual sub-0.1 μm bulk MOSFETs accurately in the saturation region.

II. NEW EXTRACTION METHOD

S-parameters are measured on typical bulk N-MOSFETs with different polysilicon gate length L_{poly} and 10 gate fingers of 5µm unit finger width. To remove RF probe pad parasitics, the accurate de-embedding technique was carried out by subtracting parasitics of open and short test structures from measured device S-parameters^[4]. In order to reduce v_{eff} extraction error due to the overestimated Q_{in} in the conventional methods using (1) at V_{ds}=0V, the following equation in the saturation region is used:

$$v_{eff}(V_{gs}, V_{ds}) = \frac{I_{ds}}{\int_{0}^{V_{gs}} [C_{gsi}(V_{gs}', V_{ds})/L_{eff}] dV_{gs}'}$$
(2)

where $C_{\rm gsi}$ is the intrinsic gate–source capacitance in the saturation region.

To obtain C_{gsi} and L_{eff} accurately using C-V measurements, the parasitic overlap and fringe capacitance C_{gso} should be subtracted from the extracted gate-source capacitance C_{gs} . However, the accurate determination of C_{gso} that contains the voltage-dependent component is very difficult in sub-0.1 μ m CMOS technology.

In order to extract v_{eff} without the difficult extraction of voltage-dependent C_{gso} and L_{eff} , the following new equation is derived by substituting C_{gsi} = KL_{eff} into (2):

$$v_{eff} (V_{gs}, V_{ds}) = \frac{I_{ds}}{\int_0^{V_{gs}} K(V_{gs}', V_{ds}) dV_{gs}'}$$
 (3)

In (3), K can be obtained by the slope of the plot of C_{gs} versus L_{poly} , because $C_{gs} = C_{gso} + K(L_{poly} - \Delta L)$ where ΔL is the channel length reduction.

Since dc I_{ds} in the saturation region is degraded by source resistance, a RF value of $I_{ds}(rf)$ determined by the following voltage-integral of g_{mi} and the output conductance g_{ds} is used for removing the source resistance effect:

$$I_{ds(rf)} (V_{gs}, V_{ds}) = \int_{0}^{V_{ds}} g_{ds}(0, V_{ds}') dV_{ds}' + \int_{0}^{V_{gs}} g_{mi}(V_{gs}', V_{ds}) dV_{gs}' (4)$$

In order to extract C_{gs} , g_{mi} , and g_{ds} from the measured S-parameters, a direct extraction technique ^[5-7] using a small-signal MOSFET equivalent circuit model in Fig. 1 has been applied.

In the high-frequency region, resistances and inductances are extracted from y-intercepts of Z-parameter equations^[5] at V_{gs} =0V as a function of ω^{-2} . The drain junction capacitance is determined at V_{gs} =0V using the following low-frequency equation in Fig. 2:



그림 1. 소스와 벌크가 연결된 소신호 MOSFET 등가회 로.

Fig. 1. A small-signal MOSFET equivalent circuit with tied source and bulk.



그림 2. 측정된 $(1/\omega)Imag(Y_{22}^{\ c}+Y_{12}^{\ c})$ 대 주파수 데이 터

Fig. 2. The measured data of $(1/\omega)Imag(Y_{22}^{\ c}+Y_{12}^{\ c})$ versus frequency.

$$C_{jd} \approx \frac{1}{\omega} Imag(Y_{22}^{\ c} + Y_{12}^{\ c})$$
(5)

where Y^c -parameters are obtained by subtracting extracted R_d , R_g , L_d , and L_g from measured S-parameters.

The substrate resistance R_{sub} is determined by k_1/C_{jd}^2 at $V_{gs}=0$ where k_1 is the slope of $Real(Y_{22}^{\ c}+Y_{12}^{\ c})$ versus ω^2 at low-frequencies^[6,7]. The values of C_{gs} , g_m , and g_{ds} are extracted by the following equations:

$$C_{gs} = \frac{1}{\omega} Imag(Y_{11}^{i} + Y_{12}^{i})$$
(6)

$$g_m = \left| Y_{21}^i - Y_{12}^i \right| \tag{7}$$



그림 3. Y-파라미터 측정치(symbol)와 모델(lines)값의 비 교

Fig. 3. Comparison between and measured (symbol) and modeled (lines) Y-parameters.

Fig.



그림 4. 다양한 Vgs - Vth에서 추출된 Cgs 대 Lpoly 데 이터

Fig. 4. The extracted data of Cgs versus Lpoly at various Vgs - Vth.

$$g_{ds} = Real(Y_{22}^i) \tag{8}$$

where Y^{i} -parameters are obtained by subtracting C_{jd}, R_{sub}, R_s, and L_s from the Y^{c} -parameters sequentially.

The accuracy of the parameter extraction has been demonstrated by observing excellent agreements between measured and modeled Y-parameters up to 30 GHz in Fig. 3. The values of K at various V_{gs} are determined from the slope of the best regression lines for C_{gs} versus L_{poly} in Fig. 4.

III. RESULTS AND DISCUSSION

In Fig. 5, gate-voltage dependent data of v_{eff} at $L_{poly} = 0.065\mu$ m obtained from the conventional method of (3) using $I_{ds}(dc)$ are lower than those of the new one using $I_{ds}(rf)$ in (4). The large extraction error of the conventional method is generated by degraded $I_{ds}(dc)$ caused by the potential drop across R_s . Fig. 6 shows the current degradation effect that $I_{ds}(dc)$ is about 19% smaller than $I_{ds}(rf)$ due to the gate-source voltage reduction of $I_{ds}Rs=0.08V$ at $V_{gs}=0.9V$. This indicates the current degradation effect should be eliminated to extract an accurate value of v_{eff} in deep sub-0.1- μ m devices. It is observed that v_{eff} exceeds the bulk saturation velocity ($v_{sat} = 10^7 \text{ cm/s}$) for bulk



그림 5. 새로운 방법으로 lds(rf)를 사용하여 추출된 식(3) 의 Vgs 종속 veff곡선과 lds(dc)를 사용한 기존 방법 곡선과의 비교

5. The Vgs-dependent curve of veff extracted from the new method of (3) using Ids(rf), compared with the conventional one of (3) using Ids(dc).





Fig. 6. RF lds(rf) data of (4) and DC lds(dc) data as a function of Vgs.

N-MOSFETs with $L_{poly} = 0.065\mu m$, because of carrier acceleration due to velocity overshoot near the drain side^[1, 8].

Physically, the drain-source saturation voltage $V_{ds}(sat)$ at the drain end of the inversion channel is expressed by $V_{gs} - V_{th}$. Thus, to analyze gate-voltage dependence of velocity in the saturation region, the effect of lateral channel electric field due to the V_{gs} increase should be incorporated together with that of vertical one. In particular, in sub-0.1µm bulk N-MOSFETs, the rising rate of lateral channel electric field with $V_{gs} - V_{th}$ becomes larger due to

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very short channel length. In Fig. 5, the linear increase of v_{eff} at low $V_{gs} - V_{th}$ is primary due to the rise of lateral field, but the reduction of the increasing rate at high $V_{gs} - V_{th}$ is due to velocity saturation and the rise of vertical field. This analysis will be very helpful to understand the gate-voltage dependent behavior of the cutoff frequency f_T and the maximum oscillation frequency f_{max} for deep sub-0.1- μ m devices in the saturation region.

IV. CONCLUSIONS

A new RF method using the RF value of Ids obtained by the voltage-integral of g_{mi} and g_{ds} from measured S-parameters is proposed to extract sub-0.1*µ*m V_{gs} -dependent v_{eff} of actual bulk MOSFETs in the saturation region accurately. This new method is developed to avoid the extraction error in conventional ones due to dc Ids degradation that can't be neglected in sub-0.1µm MOSFETs. This technique based on the slope extraction of $C_{\rm gs}$ versus L_{poly} is more accurate than previous methods, because the difficult extraction of bias-dependent C_{gso} and L_{eff} is not needed. It is observed that electron velocity enhancement exceeding Veff occurs in bulk N-MOSFETs with $L_{poly} = 0.065 \mu m$.

REFERENCES

- A. Lochtefeld and D. A. Antoniadis, "On experimental determination of carrier velocity in deeply scaled NMOS: How close to the thermal limit ?," IEEE Electron Device Lett., vol. 22, no. 2, pp. 95–97, 2001.
- [2] R. Ohba and T. Mizuno, "Nonstationary electron/hole transport in sub-0.1µm MOS devices: correlation with mobility and low-power CMOS application," IEEE Trans. Electron Device, vol. 48, no. 2, pp. 338–343, 2001.
- [3] S. Lee, "A new method to extract carrier velocity in sub-0.1µm MOSFETs using RF measurements," IEEE Trans. Nanotechnology, vol. 5, no. 3, pp. 163–166, 2006.
- [4] J. Cha, J. Cha, and S. Lee, "Uncertainty analysis of two-step and three-step methods for deembedding on-wafer RF transistor measurements," IEEE

Trans. Electron Device, Vol. 55, pp. 2195–2201, 2008.

- [5] S. Lee, "An accurate RF extraction method for resistances and inductances of sub-0.1µm CMOS transistors", Electronics Letters, Vol. 41, No. 24, pp. 1325–1327, 2005.
- [6] 김종혁, 이용택, 최문성, 구자남, 이성현, "Nano-Scale MOSFET의 게이트길이 종속 차단주 파수 추출," 전자공학회 논문지 제 42권 SD편 제 12호, pp. 1-8, 2005.
- [7] 이성현, ""나노 스케일 벌크 MOSFET을 위한 새 로운 RF 엠피리컬 비선형 모델링,"전자공학회 논 문지 제 43권 SD편 제 12호, pp. 33-39, 2006.
- [8] B. Cheng, V. R. Rao, and J. C. S. Woo, "Exploration of velocity overshoot in a high-performance deep sub-0.1-mm SOI MOSFET with asymmetric channel profile," IEEE Electron Device Lett., vol. 20, pp. 538–540, Oct. 1999.



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