J Electr Eng Technol Vol. 8, No. 6: 1328-1336, 2013
http://dx.doi.org/10.5370/JEET.2013.8.6.1328

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

A New Topology of Multilevel Voltage Source Inverter to Minimize the Number of Circuit Devices and Maximize the Number of Output Voltage Levels

Ali Ajami†, Ataollah Mokhberdoran* and Mohammad Reza Jannati Oskuee*

Abstract – Nowadays multilevel inverters are developing generally due to reduced voltage stress on power switches and low total harmonic distortion (THD) in output voltage. However, for increasing the output voltage levels the number of circuit devices are increased and it results in increasing the cost of converter. In this paper, a novel multilevel inverter is proposed. The suggested topology uses less number of power switches and related gate drive circuits to generate the same level in output voltage with comparison to traditional cascaded multilevel inverter. With the proposed topology all levels in output voltage can be realized. As an illustration, a symmetric 13-level and asymmetric 29-level proposed inverters have been simulated and implemented. The total peak inverse (PIV) and power losses of presented inverter are calculated and compared with conventional cascaded multilevel inverter. The presented analyses show that the power losses in the suggested multilevel inverter are less than the traditional inverters. Presented simulation and experimental results demonstrate the feasibility and applicability of the proposed inverter to obtain the maximum number of levels with less number of switches.

Keywords: Multilevel inverter, Cascaded multilevel inverter, Reduced number of switches, Low total harmonic distortion, PIV

1. Introduction

Multilevel inverters have been attracting growing interest since introduced at early 80s [1], particularly because of the higher power rating and quality, higher efficiency, lower total harmonic distortion and lower switching losses [2] & [3]. The mentioned advantages are achieved while the multiple dc sources are used to generate the output voltage waveform [4]. In recent years, MULTILEVEL inverters are one of the most versatile and powerful components that are utilized in many industrials such as FACTS devices [5] & [6], HVDC [7] & [8], etc. Various topologies for multilevel inverters have been introduced over the past 20 years, the most popular topologies are the diode-clamped [9], flying capacitor [10] and cascaded H-bridge topologies [11]. Also, many modulation techniques such as different pulse width modulation (PWM) techniques and space-vector PWM schemes are proposed to improve the output voltage harmonic spectrum [12] & [13]. To synthesize multilevel output, voltage clamping is one of the most important concerns. The definition of clamping is to limit the switch's terminal voltage in a proper range by using clamping devices. In the three mentioned multilevel-inverter structures, voltages are clamped by diodes, by capacitors and by separated voltage sources in the diode-clamped, the flying capacitor and the cascaded multilevel structures, respectively [14]. One property that distinguishes the cascaded H-bridge from the other multilevel structures is the capability of utilizing various dc voltages on the separate H-bridge cells. This property causes to split the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters [15]. Increasing the number of DC voltage sources causes to increase the number of levels in output voltage waveform and thereby the inverter voltage output waveform reaches a nearly sinusoidal waveform while operating at a fundamental frequency switching scheme [16]. Also to provide a large number of output levels instead of increasing the number of DC sources, asymmetric topologies of multilevel inverters can be used [17] & [18]. Unfortunately, multilevel inverters have some drawbacks. One of their disadvantages is the great number of required components especially power switches and gate drivers. This increases the cost, complexity and size of inverter [3]. It is a good idea to suggest new multilevel-inverter topologies with higher performance by reducing the number of required components [19]. In new multi-level inverter topologies with reduction of switches total PIV will increase, e.g. semi cascaded inverter uses almost half number of switches compared with cascaded converter, but this reduction results that the PIV values is as much as 1.5

† Corresponding Author: Dept. of Electrical Engineering, Azarbaijan Shahid Madani University, Iran. (ajami@azaruniv.edu)
* Dept. of Electrical Engineering, Azarbaijan Shahid Madani University, Iran. ({amokhber, m.r.jannati}@azaruniv.edu)
Received: January 2, 2013; Accepted: May 27, 2013

times in semi-cascaded converter compared with cascaded converter [20]. This paper proposes a novel topology based on connected several independent units. Compared to traditional cascaded inverter, the proposed topology reduces the number of switches while uses the same number of DC sources with the same values. A new developed topology associated with a suitable method to specify the value of dc voltage sources for symmetrical and asymmetrical multilevel inverter are proposed in this paper. The rest of this paper is organized as follows: In Section II the proposed topology is detailed and the different methods are defined to utilize both symmetric and asymmetric proposed inverter. Section III provides a brief review on traditional cascade multilevel inverter and compares with proposed topology. Simulation and experimental results are given in sections IV and sections V, respectively. Presented results show the feasibility and good performance of proposed topologies and also confirm the author's accuracy.

2. Proposed Topology

The proposed topology includes several independent units which have been combined properly. Each unit consists of two DC sources with the same value and six switches and related gate drives. Fig. 1 shows the topology of basic unit and the related switching scheme for each unit is given as below.

Fig. 2 shows the topology of proposed multilevel inverter.

The proposed topology consists of 2n-DC voltage sources with 6n-switches which is able to generate zero or positive and negative polarity voltage in all levels. As shown in Fig. 2, each switch consists of an IGBT with anti-parallel diode. Both switches (H_i, $\overline{H}_i$), (S_{1i}, $\overline{S}_{1i}$) and (S_{2i}, $\overline{S}_{2i}$) are complementary turned on the whole operation cycle.

It's noted that, as mentioned in Fig. 2 the proposed topology employs n- basic units which makes it suitable to be used in photovoltaic systems. In photovoltaic system each cell has the DC voltage value which may differs from other cells. To generate all possible levels with equal output voltage steps, the voltage of cells must be same or a DC-DC chopper should be used in output of cells. In proposed inverter to generate all possible levels with equal steps in output voltage; generally two voltage sources in each unit have the same value while the values of DC sources of each unit can be different from another unit. Different values in DC voltages of a unit in proposed inverter effects on the THD value of output voltage.

The output phase voltage is clamped by DC voltage sources. The maximum output voltage ($V_{o\,max}$) of proposed topology is defined by:

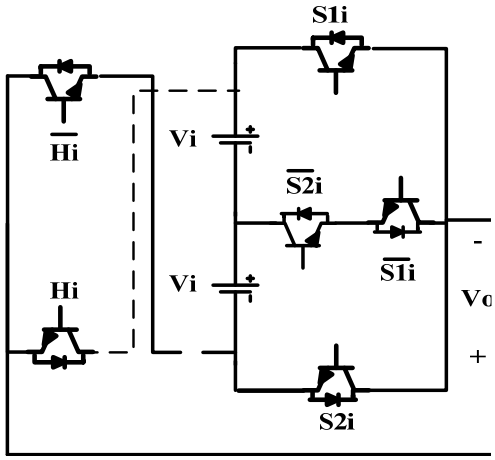


Fig.1. The overall view of basic unit

Table 1. The switching principle of unit i

Voltage level	Hi S1i S2i
0	(1 1 0) Or (0 0 1)
Vi	(1 0 0)
2Vi	(1 0 1)
-Vi	(0 0 0)
-2Vi	(0 1 0)

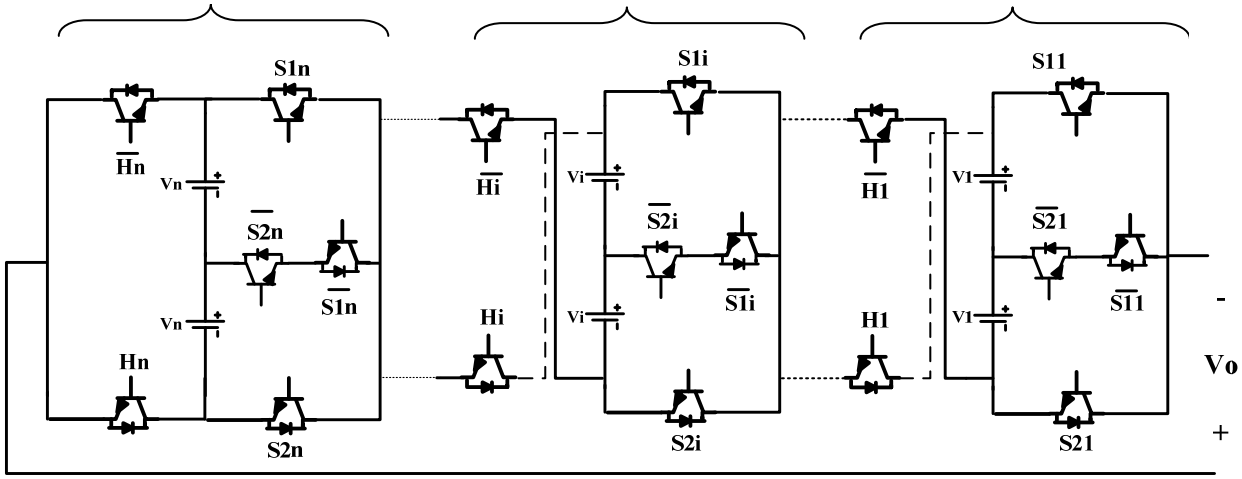


Fig. 2. The overall view of proposed inverter

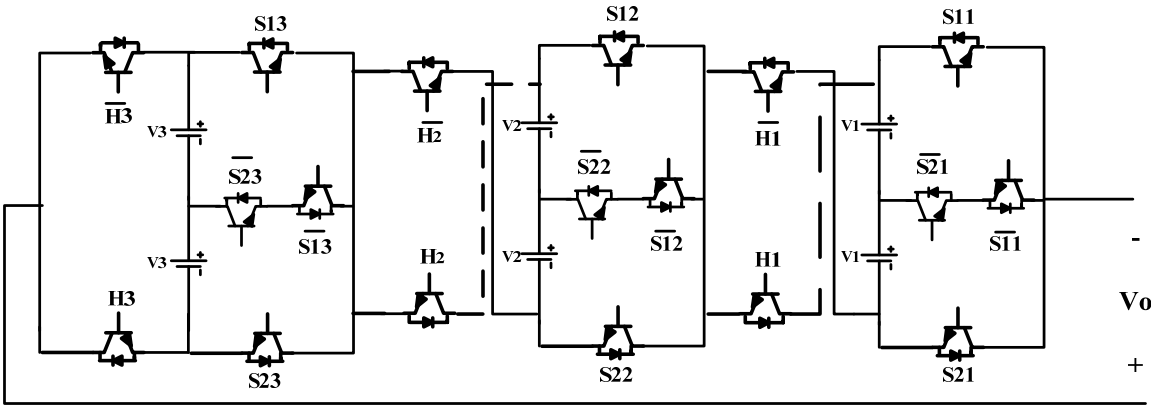


Fig. 3. The symmetric topology of 13-level proposed inverter (V_1= V_2= V_3)

$$V_{o\,max} = 2\sum_{i=1}^{n} V_i \quad (1)$$

Where 2n is the number of DC voltage sources. The maximum number of output levels in phase voltage (m) is evaluated by:

$$m = 2\frac{V_{o\,max}}{V_1} + 1 \quad (2)$$

The conduction and switching losses are two major factors of power losses in a semiconductor switch. In the suggested topology 3n-switches are turned on in different operation modes of inverter. If the on-state voltage drop of a switch points as V_d, the maximum output voltage is illustrated:

$$V_{o\,max} = 2\sum_{i=1}^{n} V_i - 3nV_d \quad (3)$$

And the total peak inverse voltage (PIV) of proposed converter can be obtained as follows:

$$PIV = \sum_{i=1}^{n} 10\,V_i \quad (4)$$

To obtain a large number of output levels, the proposed topology can be used as an asymmetric multilevel inverter, instead of increasing the number of DC- voltage sources.

For both symmetric and asymmetric operation, the mentioned Eqs. (1-3) and (4) are true. In the following, two various methods are introduced for determination of amplitude of DC voltage sources which are synthesized in the proposed topology are available. It is noticeable that in all suggested methods, each number of output voltage levels can be generated.

2.1 First method

Fig. 3 shows the symmetric topology of 13-level proposed inverter.

If the value of all DC voltage sources V_i in Fig. 3 equal to V_{dc}, the inverter is known as symmetric topology. The number of output voltage levels of the inverter with 2n-DC voltage sources with same values can be calculated as follows:

$$m = 4n+1 \quad (5)$$

Also the maximum output voltage can be evaluated by:

$$V_{o\,max} = 2n\,Vdc \quad (6)$$

2.2 Second method

In the proposed topology Vi can set to be $V_i = p^{i-1} * V_1$, Where p=2, 3… 2n+1. In other words p can be set to adjust the output voltage level to a desired value instead of manipulating the inverter circuit. In this case the proposed multilevel inverter is known as asymmetric topology, which increases the number of the output voltage levels without adding any DC voltage sources and switches. With notice to,$V_i = p^{i-1} * V_1$ the all levels can be produced in output voltage and the value of steps will be V1. In the proposed inverter with 2n-DC voltage and assumption$V_i = p^{i-1} * V_1$, the maximum output voltage ($V_{o\,max}$) and the number of output voltage levels (m) can be evaluated by (7) and (8), respectively. Table 2 compares the required power devices of proposed multilevel inverter in both methods.

$$V_{o\,max} = 2\frac{1-p^n}{1-p}V_1 \quad (7)$$

Table 2. Required components of proposed multilevel inverters

Proposed	First Method	Second Method
NO. of DC sources	2n	2n
NO. of switches	6n	6n
NO. of Output Levels	4n+1	$4\frac{1-P^n}{1-P}$+1
Maximum Voltage	2n * V_1	$2 * \frac{1-P^n}{1-P} * V_1$
PIV	$10n * V_1$	$10 * \frac{1-P^n}{1-P} * V_1$
NO. of On-State Switches	3n	3n

$$m= 4\frac{1-p^n}{1-p}+1 \quad (8)$$

3. Conventional Cascade Multilevel Inverters Configuration

Fig.4 shows a single-phase cascaded multilevel inverter with separated DC voltage sources.

The output voltage of cascaded multilevel inverter is synthesized by summing the output voltages of bridges. Each H-bridge generates a three-level square-wave voltage associated with four switches an d one DC voltage source. In a cascaded inverter with 2n DC voltage sources with n different values (a set of single phase cascaded inverter shown in Fig. 4) the maximum output voltage ($V_{o\,max}$) and the maximum number of output levels (m) can be obtained from (1) and (2), respectively. It's evident that in a cascade multilevel inverter with 2n-DC sources, always 4n switches must be turn on in various operation modes, so the maximum output voltage can be defined as:

$$V_{o\,max} = 2\sum_{i=1}^{n} V_i - 4nV_d \quad (9)$$

Where V_d is the on-state voltage drop of a switch.

To attain a large number of output levels, the asymmetrical DC sources can be employed in cascaded multilevel inverter instead of increasing the number of H-bridges.

For asymmetric cascaded multilevel inverter with 2n DC sources and n-different values, the mentioned equations (1), (2) are true. The total peak inverse voltage (PIV) of

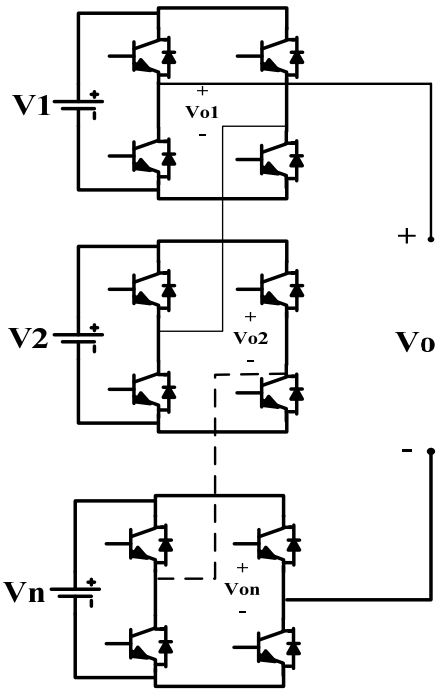


Fig. 4. A single-phase cascaded multilevel inverter

Table 3. Required power components for conventional cascaded inverter

	First Method	Second Method
NO. of DC sources	2n	2n
NO. of switches	8n	8n
NO. of Output Levels	4n+1	$4\frac{1-P^n}{1-P}+1$
Maximum Voltage	2n * V1	$2*\frac{1-P^n}{1-P}*$ V1
PIV	$8n*V_1$	$8*\frac{1-P^n}{1-P}*V_1$
NO. of On-State Switches	4n	4n

switches for both symmetric and asymmetric can be evaluated in (10) and (11), respectively:

$$PIV = \sum_{i=1}^{n} 4V_1 \quad (10)$$

$$PIV = \sum_{i=1}^{n} 4V_1 \frac{1-p^n}{1-p} \quad (11)$$

The major sufficiency of cascaded topology is the modularity of control and protection requirements of each H-bridge, but the higher amount of required switches is the major it's disadvantage. In the proposed topology the number of circuit devices is substantially reduced. For the purpose of comparison, the suggested methods for the proposed topology described in section II are employed for conventional cascaded multilevel inverter. As illustrated before, the proposed inverter and the cascaded inverter need 2n-DC sources with n-different values. Table 3 compares the required power components of the conventional cascaded inverter for both illustrated methods in section 2.

4. Comparison Study

The main goal of this paper is to present a new topology which the amount of the required components is lower than the conventional cascaded multilevel inverters.

The number of required switches and also the ratings of them are the great importance in multilevel inverter structures. It's apparent that the number of switches in proposed topology is noticeably lower than the conventional cascaded inverter in a same output level for both methods, as illustrated in Table 2 and Table 3. Also, voltage and current ratings of the power switches play important roles on the overall cost of the system and realization of the inverter. It can be seen from Table 2 and Table 3 that the total PIV of proposed inverter is lower than the traditional cascaded multilevel inverter with same number of DC voltage sources. Also the number of on-state switches is lower in the proposed topology compared to conventional cascade and so the output voltage drop is reduced. Figs. 5 and 6 represent the results of comparing the conventional cascaded multilevel inverters and the

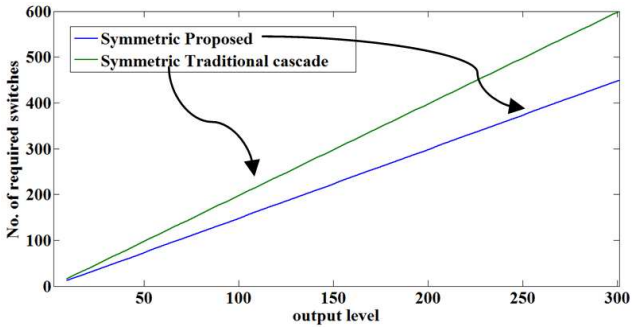


Fig. 5. The number of switches for symmetric mode of proposed topology and the conventional cascade inverter

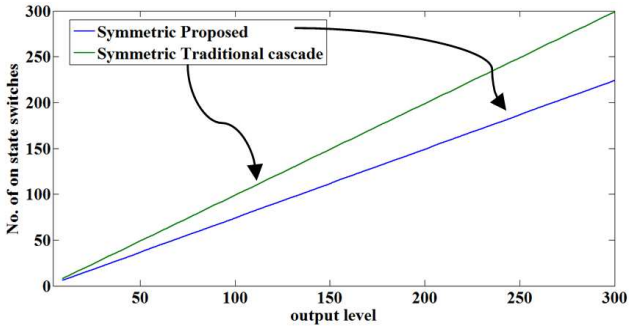


Fig. 6. The number of on-state switches versus output levels

proposed topology from different points of view. Fig. 5 shows the number of switches (IGBTs and gate drivers) versus the number of output voltage levels for symmetric mode of proposed topology and the conventional cascade inverter.

As seen in Fig. 5 the proposed topology requires less number of switches and gate driver circuits for realizing the output voltage levels. Therefore, this achievement reduces the installation area and cost of the proposed topology in comparison with the conventional cascaded inverter for realizing the same output voltage levels.

The number of on state switches results in output voltage drop and conduction losses of converter. Therefore, it is considered as a substantial factor to compare the conventional cascaded inverter and proposed topology. As presented in Fig. 6 the number of on-state switches for proposed topology is less.

5. Calculation of Power Losses

Refers to the given descriptions, the conduction and switching losses are commonly two kinds of losses that is studied in inverters. Conduction losses are due to the equivalent resistance and the on-state voltage drop of the switches. The switching losses are because of non-ideal operation of switches. The below paragraph is arranged to evaluate the losses of the proposed multilevel inverter. So as to calculating the conduction losses, firstly formulas for conduction losses of a typical power semiconductor switch is provided then they are extended to the overall proposed inverter. Each power semiconductor switch includes an IGBT and anti-parallel diode. In the following expression (12) and (13) the instantaneous conduction losses of IGBT and diode are separately formulated [21]. $P_{c.T}(t)$ is for IGBT and $P_{c.D}(t)$ is for diode.

$$P_{c.T}(t) = \left[V_T + R_T i^{\beta}(t)\right] i(t) \quad (12)$$

$$P_{c.D}(t) = [V_D + R_D i(t)] i(t) \quad (13)$$

V_T and V_D, are noted the on-state voltage of IGBT and diode respectively and β is a constant dependent to the IGBT characteristic. R_T and R_D indicate the equivalent resistance of the IGBT and diode, respectively. In the proposed inverter, the number of IGBT, $N_T(t)$, and diodes, $N_D(t)$, in the current path are varying with time. Because, the number of on state switches is dependent to the output voltage level and operating conditions (essentially direction of the current). In order to calculate the average of conduction power loss the equation (12) and (13) are used and a formula for conduction power loss is provided as follows:

$$P_c = \frac{1}{\pi}\int_0^{\pi} (N_T(t) * P_{c.T}(t) + N_D(t) * P_{c.D}(t)) \, d(\omega t) \quad (14)$$

The switching losses are formulated for a typical power semiconductor switch and then obtained formulas are developed to the overall inverter system. To evaluate switching losses, the linear approximation of the current and voltage during switching period is considered. With the assumed approximation, a formula for energy loss during the turn on period of a power semiconductor switch is provided as follows:

$$E_{on,J} = \int_0^{t_{on}} v(t) i(t)\, dt = \int_0^{t_{on}} \left[\frac{V_{sw,J}}{t_{on}} t\right] \left[\frac{-I}{t_{on}} (t - t_{on})\right] dt = \frac{1}{6} V_{sw,J}\, I\, t_{on} \quad (15)$$

Where, $E_{on,J}$ is the turn on loss of the Jth switch, t_{on} is the turn on time of the mentioned switch and I is the current through the switch after turning on. To formulate the energy loss during the turn off period is only required to substitute the "on" subtitle with "of" in the last term of (15) and I with I', which I' is the current through the switch after turning off.

$$E_{off,J} = \frac{1}{6} V_{sw,J}\, I'\, t_{off} \quad (16)$$

The switching losses are relevant with the number of switching transitions and also to the control scheme.

Commonly, the average switching power loss can be evaluated with the following expression:

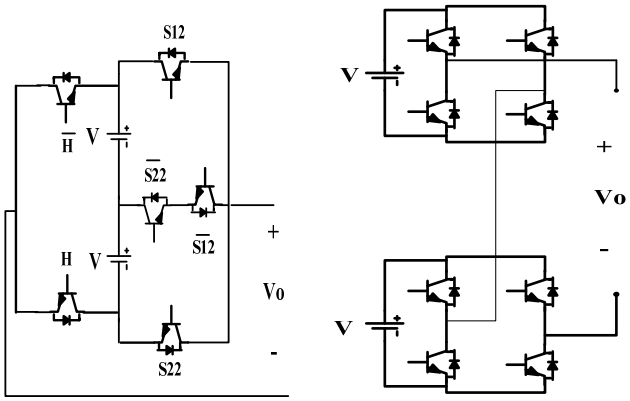
$$P_{sw} = 2f[\sum_{J=1}^{N_{switch}} \left(\sum_{i=1}^{N_{on,J}} E_{on,Ji} + \sum_{i=1}^{N_{off,J}} E_{off,Ji}\right)] \quad (17)$$

Where, f is the fundamental frequency, $N_{on,J}$ and $N_{off,J}$ are the number of turning on and off the Jth switch during a half fundamental cycle. Also, $E_{on,Ji}$, is the energy loss of the Jth switch during the ith turning-on and $E_{off,Ji}$, is the energy loss of the Jth switch during the ith turning-off. Using (14) and (17), the total losses of the overall proposed multilevel inverter is given as follows:

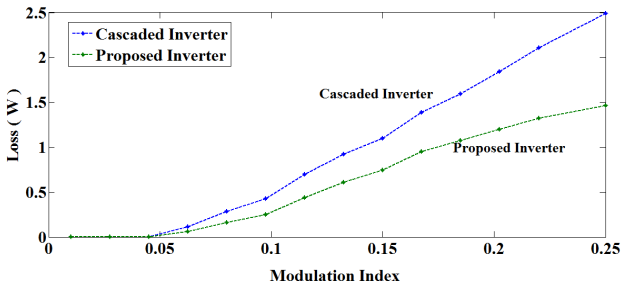
$$P_{Loss} = P_{sw} + P_c \quad (18)$$

To validate that there is a loss reduction in the proposed multi-level inverter compared with cascaded inverter, loss amount of basic units of proposed inverter and cascade inverter, shown in Fig. 7(a) and (b), are calculated for different modulation indexes and is shown in Fig. 7(c). Both cascaded inverter and proposed inverter are simulated using BUP400D switches with the given real data in [22] and 10v DC voltage sources values and load parameters of 30ohm and 20mH.

As a case study for the basic unit of proposed inverter and the given data in Table 6 for modulation index equal to 0.2 the demand power is 180W and the supply power of DC sources is 192W which defines that the power loss of proposed inverter is less than 7%.



(b)



(c)

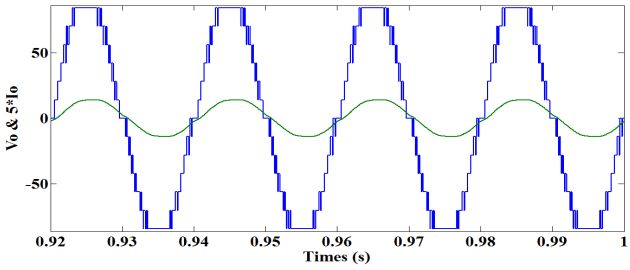
Fig. 7. (a) Basic units of proposed inverter; (b) cascaded inverter; (c) Loss comparison for proposed inverter and cascaded inverter

6. Simulation Results

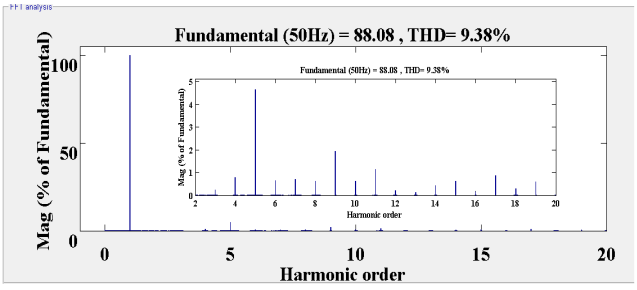
To validate the good performance of the proposed multilevel inverter, a single phase 13-level proposed topology is considered, and the simulation and experimental results are obtained. The MATLAB/Simulink software has been used for simulation. The prototype of proposed topology which includes 6-DC sources and 18 switches generating staircase waveform with the maximum 84 V in output is considered. A series R–L with R=30 ohm

Table 4. Switching states 13-level proposed symmetric inverter

Output voltage level	$H_3\ S_{13}\ S_{23}$ $H_2\ S_{12}\ S_{22}$ $H_1\ S_{11}\ S_{21}$
6E	(0 0 1 1 0 1 1 0 1)
5E	(0 0 1 1 0 1 1 0 0)
4E	(0 0 1 1 0 1 1 1 0)
3E	(0 0 1 1 0 0 1 1 0)
2E	(0 0 1 1 1 0 1 1 0)
E	(0 0 0 1 1 0 1 1 0)
0	(0 1 0 1 1 0 1 1 0)
-E	(1 0 0 1 1 0 1 1 0)
-2E	(1 1 0 1 1 0 1 1 0)
-3E	(1 1 0 0 0 0 0 0 1)
-4E	(1 1 0 0 1 0 0 0 1)
-5E	(1 1 0 0 1 0 0 0 0)
-6E	(1 1 0 0 1 0 0 1 0)

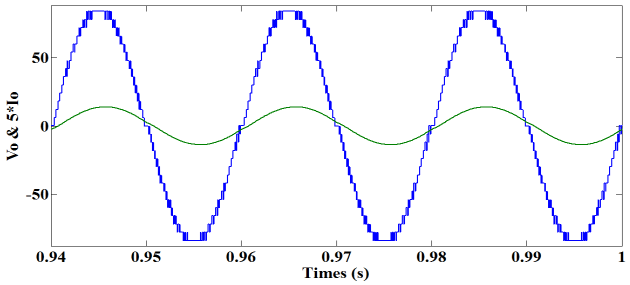


(a)

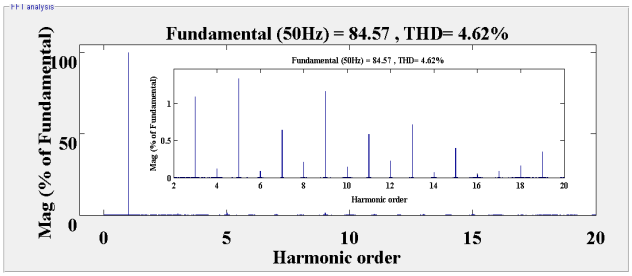


(b)

Fig. 8. (a) The voltage and current waveform (b) the harmonic spectra, of proposed symmetric 13-level inverter



(a)



(b)

Fig. 9. (a) The voltage and current waveform; (b) harmonic spectra, of proposed asymmetric 29-level inverter

and L=20 mH are used as a load. To extend the ability of proposed topologies as an asymmetric inverter, the asymmetrical DC sources are chosen to generate the 84v with the 29 steps in output voltage. Table 4 defines the switching principle of symmetric 13-level proposed inverter.

7. Experimental Results

To validate the proposed multilevel inverter topology, a 13-level symmetric proposed inverter as shown in Fig. 3 is implemented. Fig. 10 shows the implemented prototype proposed inverter. The control system of proposed inverter is implemented by DSPIC30F4011 controller. To implement the proposed symmetric 9-level inverter 4 dc voltage sources and 12 IGBTs are used. Table 6 represents the implemented circuit parameters. The experimental output voltage in the no load case are shown in Fig. 11 (a). Fig. 11 (b) shows output voltage and current under load condition. Fig. 11 validates the practicability of proposed multilevel which can generate all voltage steps for a test case 13-level symmetric inverter.

Fig. 12 validates the practicability of proposed multilevel which can generate all voltage steps for a test case 29-level asymmetric inverter with p=2 and V_1=40, V_2=80, V_3=160.

The obtained experimental results validate the practicability of proposed symmetric and asymmetric multilevel inverters which can generate all voltage steps for a test case 13-level symmetric and 29-level asymmetric inverter.

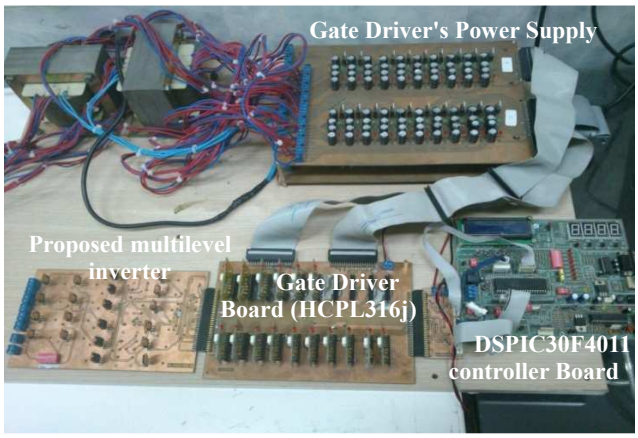
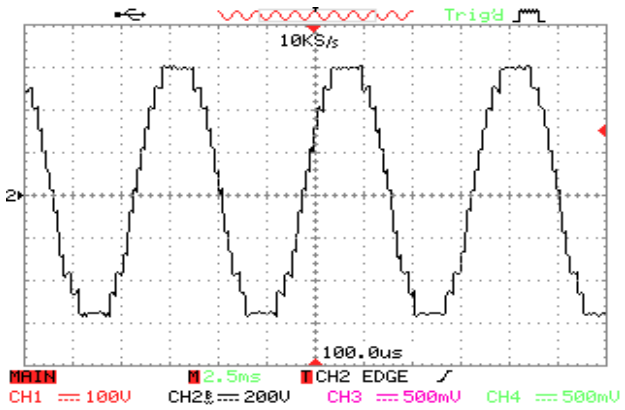


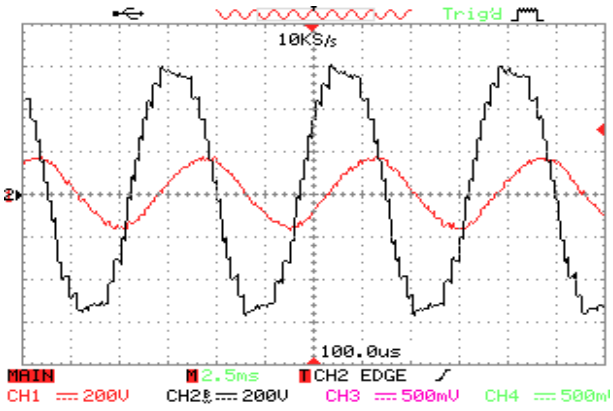
Fig. 10. The implemented prototype of proposed 13-level symmetric inverter

Table 6. Value of parameters in implemented inverter

DC voltage sources In symmetric case	V_1=V_2=V_3=100 V
Type of switch	BUP400D
Type of IGBT Driver	HCPL316j
Load Parameters	150ohm & 300mH

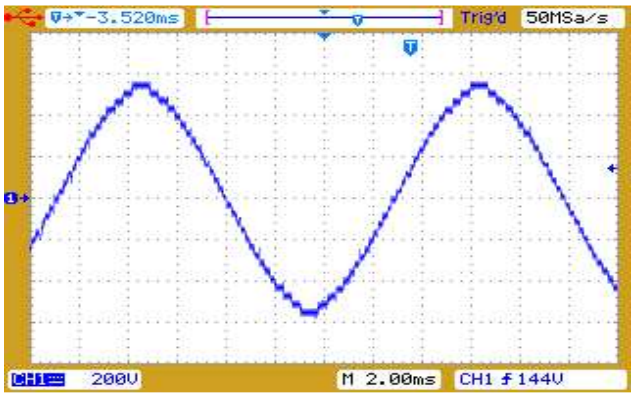


(a)

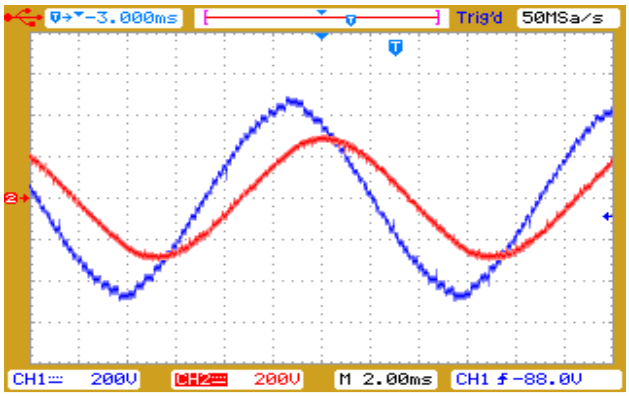


(b)

Fig. 11. (a) The voltage waveform; (b) the voltage and current waveform of 13-level proposed symmetric inverter



(a)



(b)

Fig. 12. (a) The voltage waveform; (b) the voltage and current waveform of a 29-level proposed symmetric inverter

8. Conclusion

A new multilevel inverter with a reduced number of power components has been suggested to increase the number of output voltage levels. With the suggested inverter the same level in output voltage is generated with fewer numbers of switches and related gate drive circuits compared to traditional cascaded inverter. Also the number of on-state switches is lower in the proposed topology compared to conventional cascade, so the output voltage drop is reduced and conduction power loss is decreased.

The simulation and experimental results are provided to submit the good performance and applicability of proposed inverter.

References

[1] Pablo Lezana, Roberto Aceitón, "Hybrid Multi-cell Converter: Topology and Modulation", *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, Sep. 2011.

[2] Ebrahim Babaei, "A Cascade Multilevel Converter Topology With Reduced Number of Switches," *IEEE Transactions on Power Electronics*, vol. 23, no. 6, Nov. 2008.

[3] M.R. Banaei, E. Salary, "New multilevel inverter with reduction of switches and gate driver," *Energy Conversion and Management*, vol. 52, pp. 1129-1136, 2011.

[4] M. Calais, V.G. Agelidis, M. Meinhardt, "Multilevel converters for single phase grid connected photovoltaic systems: an overview," *Elsevier J. Solar Energy*, vol. 66, no. 6, pp. 325-335, 1999.

[5] Q. Song and W. Liu, "Control of a cascade STATCOM with star configuration under unbalanced conditions," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp.45-58, Jan. 2009.

[6] B. Geethalakshmi and P. Dananjayan, "Investigation of performance of UPFC without DC link capacitor," *Elect. Power Energy Res.*, vol. 48, no. 4, pp. 736-746, 2008.

[7] Hui Ding, Yi Zhang, Aniruddha M. Gole, Dennis A. Min Xiao Han and Xiang Ning Xiao, "Analysis of Coupling Effects on Overhead VSC-HVDC Transmission Lines From AC Lines With Shared Right of Way," *IEEE Transactions on Power Delivery*, vol. 25, no. 4, Oct. 2010.

[8] Shuhui Li Timothy A. Haskew and Ling Xu, "Control of HVDC Light System Using Conventional and Direct Current Vector Control Approaches," *IEEE Transactions on Power Electronics*, vol. 25, no. 12, Dec. 2010.

[9] Changliang Xia, Xin Gu, Tingna Shi, and Yan Yan, "Neutral-Point Potential Balancing of Three-Level Inverters in Direct-Driven Wind Energy Conversion System," *IEEE Transactions on Energy Conversion*, vol. 26, no. 1, Mar. 2011.

[10] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, M. A. Perez, "Multilevel inverters: an enabling technology for high-power applications," *Proceedings of IEEE*, vol. 97, no. 11, pp. 1786-1817, Nov. 2009.

[11] F.Z. Peng, J.-S. Lai, J.W. McKeever, and J. Van Coevering, "A multilevel voltage-source inverter with separate DC sources for static var generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130-1138, Sep./ Oct. 1996.

[12] Sergio Busquets-Monge, Salvador Alepuz, Joan Rocabert and Josep Bordonau, "Pulse width Modulations for the Comprehensive Capacitor Voltage Balance of n-Level Three-Leg Diode-Clamped Converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 5, May 2009.

[13] Maryam Saeedifard, Reza Iravani, and Josep Pou, "A Space Vector Modulation Strategy for a Back-to-Back Five-Level HVDC Converter System," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2,

Feb. 2009.
[14] Alian Chen and Xiangning He, "Research on Hybrid-Clamped Multilevel-Inverter Topologies," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 6, Dec. 2006.
[15] Keith A. Corzine, Mike W. Wielebski, Fang Z. Peng and Jin Wang, "Control of Cascaded Multilevel Inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 3, May 2004.
[16] Sung Geun Song, Feel Soon Kang and Sung-Jun Park, "Cascaded Multilevel Inverter Employing Three-Phase Transformers and Single DC Input," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, Jun. 2009.
[17] Ebrahim Babaei, Mohammad Sadegh Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," *Energy Conversion and Management*, vol. 51, pp. 2272-2278, 2010.
[18] Veenstra M, Rufer A. "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives," *IEEE Transactions on Industrial Applications*, vol. 41, no. 2, pp. 655-664, 2005.
[19] Lezana P, Rodriguez J. "Mixed multi-cell cascaded multilevel inverter," *ISIE 2007 IEEE international symposium*, June, 2007.
[20] Ebrahim Babaei, Seyed Hossein Hosseini, New cascaded multilevel inverter topology with minimum number of switches, *Energy Conversion and Management,* vol. 50, pp. 2761-2767, 2009.
[21] Kangarlu, M.F., Babaei, E, "A generalized cascaded multilevel inverter using series connection of sub-multilevel inverters ," *IEEE Trans. Power Electronics*, vol. 28, no. 2, pp. 625-636, Feb 2013.
[22] Data sheet of IGBT 'BUP 400D', Available at: *www.datasheetcatalog.com* .

Ali Ajami He received his B.Sc. and M. Sc. degrees from the Electrical and Computer Engineering Faculty of Tabriz University, Iran, in Electronic Engineering and Power Engineering in 1996 and 1999, respectively, and his Ph.D. degree in 2005 from the Electrical and Computer Engineering Faculty of Tabriz University, Iran, in Power Engineering. Currently, he is associate Prof. of electrical engineering department of Azarbaijan Shahid Madani University. His main research interests are dynamic and steady state modeling and analysis of FACTS devices, harmonics and power quality compensation systems, microprocessors, DSP and computer based control systems.

Ataollah Mokhberdoran He was born in Tabriz, Iran in 1983 and received his B.Sc. and M.Sc. degrees from the Electrical Engineering Faculty of Iran University of Science and Technology and Azarbaijan Shahid Madani University, Iran, in Electrical Power Engineering in 2006 and 2010, respectively. Currently, he works as R&D manager of ASAS Company in Tabriz. In recent years, he performed numerous industrial research and development projects in power engineering fields. His research interests include multilevel inverters, power converters, renewable energies, FACTs, DSP based power electronic devices and smart grids.

Mohammad Reza Jannati Oskuee He was born in Tabriz, Iran, in 1988. He received his B.Sc. degree (2011), in electrical power engineering from University of Tabriz, Tabriz, Iran. Currently he is M.Sc. student of Power Engineering at Azarbaijan Shahid Madani University, Tabriz, Iran. His major research interests include smart grid, distribution system planning and operation, renewable energy, power electronics, application of evolutionary algorithms and intelligence computing in power systems, dynamics and FACTS devices.