J Electr Eng Technol Vol. 8, No. 6: 1352-1364, 2013
http://dx.doi.org/10.5370/JEET.2013.8.6.1352

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Control of a Single Phase Unified Power Quality Conditioner-Distributed Generation Based Input Output feedback Linearization

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Abstract – This paper describes a novel structure for single phase Unified Power Quality Conditioner-Distributed Generation (UPQC-DG) with direct grid connected DC-AC converter for low DC output DG systems which can be used not only for compensation of power quality problems but also for supplying of load power partly. This converter has been composed of one full-bridge inverter, one three winding high frequency transformer with galvanic isolation and two cycloconverters. Proper control based on Input Output feedback Linearization is used to tracking the reference signals. The simulation and experimental results are presented to confirm the validity of the proposed approach.

Keywords: UPQC-DG, Input-Output Feedback Linearization method, High Frequency Transformer.

1. Introduction

Nowadays, most of the equipments based on power electronic devices used by the industry, lead to power quality problems. These devices not only need high-quality energy to work properly but also are the major cause for decreasing of power quality. In these conditions, both electric utilities and customers are increasingly affected from the quality of electric power. Between the different technical approaches available for compensation of power quality problems, Active Power Filters (APFs) have an important alternative to compensate the power quality problems [1].

Different configurations of APFs can be found in [2] and [3]. One of the comprehensive systems for many of power quality problems, such as current harmonics, reactive power, and source voltage distortions, is Unified Power Quality Conditioner (UPQC) [4]. It consists of two back to back connected series and shunt Voltage Source Inverters (VSIs) with a common dc link [5-9]. In all of the previous contributions of series and shunt inverters DC link capacitor is a major part of compensator. Custom power devices such as UPQC by a DC link capacitor need to an external control circuit for arranging up the DC capacitor stored energy. Although limit stored energy in DC capacitor causes inability of deep voltage sags and interruptions [10].

In the last decade, Distributed Generation systems (DGs) which use Clean Energy Sources (CESs) such as wind power [10], fuel cells [11] and photo voltaic are integrated at distribution level increasingly and will have major role in future sustainable energy systems [4]. Also they can be as an active power source which affects in stability, voltage regulation and Power Quality (PQ) issues of the network. With the advancement in power electronics, the custom power devices with DG systems can now be actively controlled to enhance the system operation for improving PQ at Point of common Coupling (PCC) [12].

In this area converters not only are considered as an essential part of custom power devices such as UPQC but also have a key role in connecting of different types of DGs to the grid. So, further studying and developing of them can be an essential problem.

A high frequency link direct boost DC-AC converter accompanied by a dc link capacitor has been proposed in [13]. Existence of DC link capacitor in this converter can lead to increase in circuit degree and difficulty in dynamic analysis. In some of related schemes, converters with a galvanic isolation high frequency link can be used for elimination of the DC link capacitor and big volume power transformer [14, 15].

The previous configurations of UPQC, based on limit DC link capacitor energy storage are unable to compensation of deep and long voltage sags, and interruptions [10]. This problem could be solved by using of DG as an active source in DC side of custom power devices such as UPQC. In [4] a series of photovoltaic arrays as a DC DG, have been connected to the DC side of UPQC via a boost DC-DC converter. In [10] a wind turbine as an AC DG has been connected to the DC side of UPQC via a DC-AC converter. Also because of variable nature of wind a battery has been connected directly to the DC side of UPQC. The battery is used in low power generation condition by the wind turbine. In [16] a small AC generator has been connected to the DC side of UPQC via a rectifier which could be as an active power source for load supply and compensation of voltage interruptions. In [17] a single

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Received: February 16, 20103; Accepted: May 27, 2013

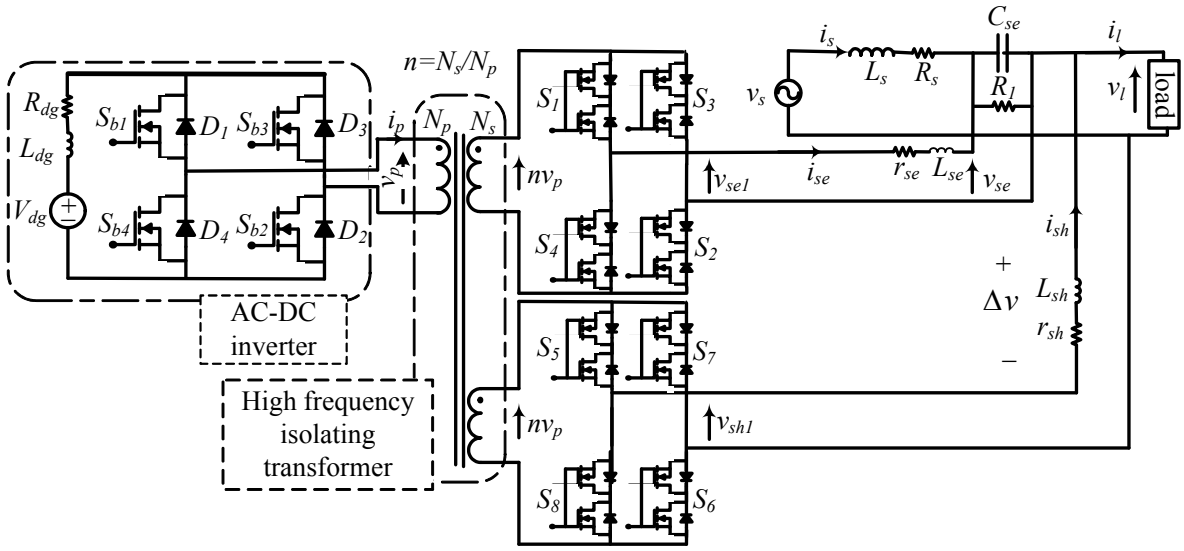

Fig. 1. The proposed direct DC-AC converter configuration (UPQC-DG)

phase combination of photovoltaic systems with UPQC for power quality compensation has been investigated too.

This paper proposes a novel configuration for the UPQC-DG which is composed from a direct DC-AC converter and a high frequency link. In the proposed configuration a DG system with low voltage DC output has been connected to the DC side of the UPQC. The proposed configuration has been composed of one full-bridge inverter, one three winding High Frequency Transformer (HFT) and two cycloconverters. One of the cycloconverters acts as a series APF and the other one act as a shunt APF which are connected to the grid directly. High frequency transformer not only steps up voltage of the primary side and reduce converters volume but also provide an electrical isolation between input DG and main grid. Also elimination of DC link capacitor not only can reduce related losses and increase conversion efficiency but also can reduce circuit degree and simple the dynamic analysis of it. State space equations of the proposed configuration is presented for dynamic analysis of the proposed configuration and providing proper control based on phase shift with nonlinear control. According to the nonlinear inherent of the proposed system, designing of the proposed configuration controller is based on the Input-Output feedback Linearization (IOFL) [18-20]. The operation of the proposed system is analyzed through simulations with power system computer-aided design/electromagnetic transient dc analysis program (PSCAD/EMTDC). The experimental results of a 220V-50Hz prototype are provided to validate the theoretical analysis.

2. Proposed UPQC Configuration

As shown in Fig. 1, in the proposed configuration UPQC has been composed of two cycloconverters which act as series and shunt APFs and have been connected back to back to a full-bridge inverter via a HFT. Each cycloconverters has been composed of eight bidirectional switches. The shunt cycloconverter can compensate load current harmonics and reactive power but the series cycloconverter can compensate voltage problems. Series cycloconverter is connected to the grid via a second order low pass LC filter. The proposed configuration not only can supply a part of load power but also can compensate power quality problems. For avoiding of saturation of transformer, the input DC port (DC-AC inverter) works with a duty cycle equal to 50%. For avoiding of short circuit, there is a dead time between switches S_1, S_2 and S_3, S_4 and similarly between switches S_5, S_6 and $S7$, S_8. Also there is an overlapping time between switches of each cycloconverter considering the continuity of inductive current. In the proposed converter which DC voltage is directly converted to an AC one, the electric isolation between input and output ports is implemented by a HFT which steps up the input voltage and, reduces the size and volume of the converter.

3. Switching Modes of the Proposed Configuration

Fig. 2, shows the simulation results of the main switching waveforms for a specific operating point. The switching period is $T_s=1/f_s$ which f_s is the switching frequency. As shown in fig. 2, there are 12 modes in the proposed converter, but the modes related to dead and overlapping times can be ignored to simplify the circuit modeling. The simplified switching modes have been listed in Table 1. The primary voltage of high frequency isolation transformer is a bipolar square wave AC voltage with high frequency and duty cycle equal to 50%. Secondary voltage

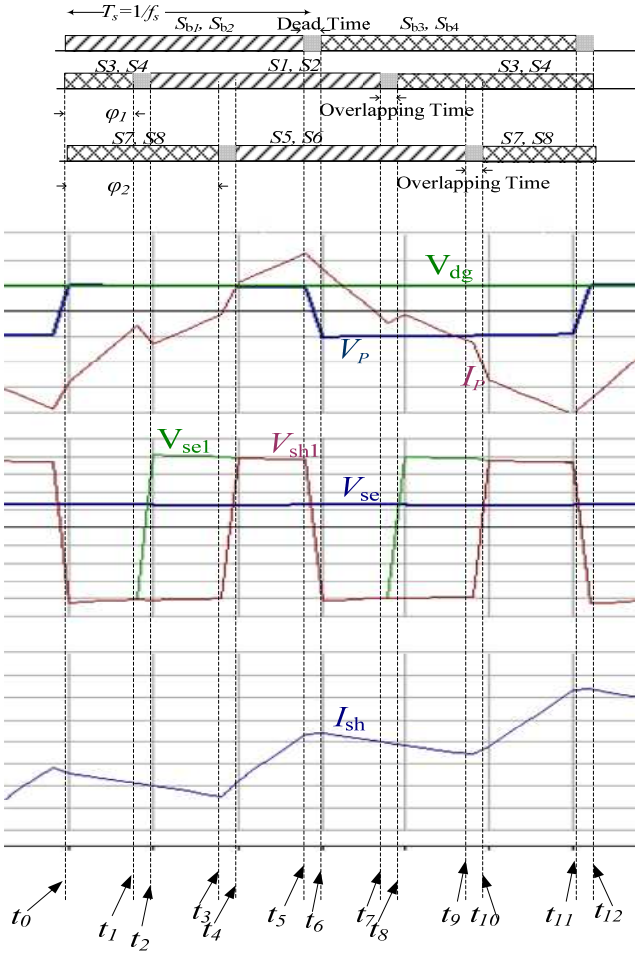

Fig. 2. Switching modes for the proposed UPQC

of transformer is v_s=nv_p. Where, n is the transformer ratio. Also v_p and v_s are the primary and secondary voltages of the transformer respectively. By the phase shift of φ_1 and φ_2 of series and shunt cycloconverters switches (respect to the primary side full-bridge switches), the output voltage/current of each cycloconverter can track the related reference signals.

As shown in Fig. 2, existence of a DC DG source in the primary side of the high frequency transformer causes a positive or negative bias in the primary side current of the transformer. This problem can be viewed based on the Kirchhoff Voltage Law on the primary side of the transformer in a special operating point as Eq. (1).

$$\begin{aligned} &R_{dg}i_p(t)+L_{dg}\frac{di_p(t)}{dt}=V_{dg}-v_p(t)\\ &i_p(s)=\frac{V_{dg}}{s(R_{dg}+L_{dg}s)}-\frac{v_p(s)}{R_{dg}+L_{dg}s}\\ &i_p(t)=\frac{V_{dg}}{R_{dg}}(1-e^{-\frac{R_{dg}}{L_{dg}}t})u(t)-L^{-1}[\frac{v_p(s)}{R_{dg}+L_{dg}s}] \end{aligned} \quad (1)$$

Table 1. Time intervals and switches states

Time interval	ON state
$0<t<\varphi_1$	S_{b1}, S_{b2}, S_3, S_4, S_7, S_8
$\varphi_1<t<\varphi_2$	S_{b1}, S_{b2}, S_1, S_2, S_7, S_8
$\varphi_2<t<\pi$	S_{b1}, S_{b2}, S_1, S_2, S_5, S_6
$\pi<t<\pi+\varphi_1$	S_{b3}, S_{b4}, S_1, S_2, S_5, S_6
$\pi+\varphi_1<t<\pi+\varphi_2$	S_{b3}, S_{b4}, S_3, S_4, S_5, S_6
$\pi+\varphi_2<t<2\pi$	S_{b3}, S_{b4}, S_3, S_4, S_7, S_8

4. Reference Signals of the Proposed UPQC

The proposed UPQC consists of two shunt and series APFs which each of controllers should have their reference outputs. Their reference signals are calculated as follows.

4.1. Reference signals of the series APF

In this paper the source voltage has been assumed to be pure sinusoidal (it has first order component only) with sag and swell. In this control approach, series APF compensates voltage sag and swell. So, the series APF arranges the load voltage at a predetermined constant voltage level. As Eqs. (2) and (3), first order components of the source voltage ($v_{r1}(t), v_{i1}(t)$), which are extracted from Fourier transform, are normalized to the nominal magnitude (V_{nom}) and set as desired load voltage ($v_{lref}(t)$) [21]. So the reference voltage of the series APF is determined as Eq. (4).

$$\begin{aligned} &v_1(t)=v_{r1}(t)+v_{i1}(t)=V_{r1}\sin(\omega t)+V_{i1}\cos(\omega t)=\\ &\sqrt{{V_{r1}}^2+{V_{i1}}^2}\sin(\omega t+\tan^{-1}\frac{V_{i1}}{V_{r1}}) \end{aligned} \quad (2)$$

$$v_{lref}(t)=\frac{V_{nom}}{\sqrt{{V_{r1}}^2+{V_{i1}}^2}}v_1(t)=V_{nom}\sin(\omega t+\tan^{-1}\frac{V_{i1}}{V_{r1}}) \quad (3)$$

$$v_{ser}(t)=v_{lref}(t)-v_s(t) \quad (4)$$

Where, v_s is the source voltage and $v_{ser}(t)$, is the series active filter reference voltage. Also V_{r1} and V_{i1} are magnitudes of the first order active and reactive components of the source voltage respectively. Fig. 3, shows block diagram of the series active filter reference signal extraction circuit.

In Fig. 3, active and reactive components of the source voltage (v_s), have been determined from Fourier transform (the first order component detector block). In this figure, PLL block is used for detection of the angular frequency.

4.2. Reference signals of parallel APF

As mentioned before, load side current high degree harmonics and load reactive power can be compensated by the shunt cycloconverter in the source side. Based on single phase pq theory [22] active and reactive components

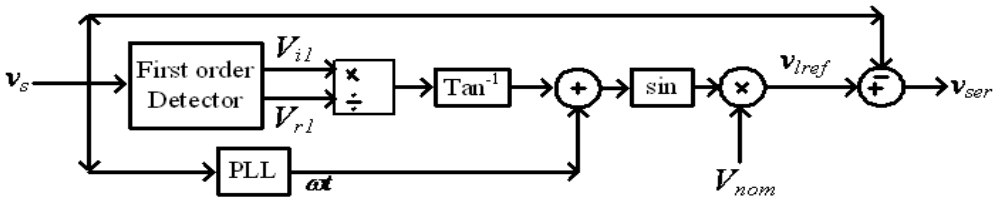

Fig. 3. Block diagram of the series active filter reference signal extraction

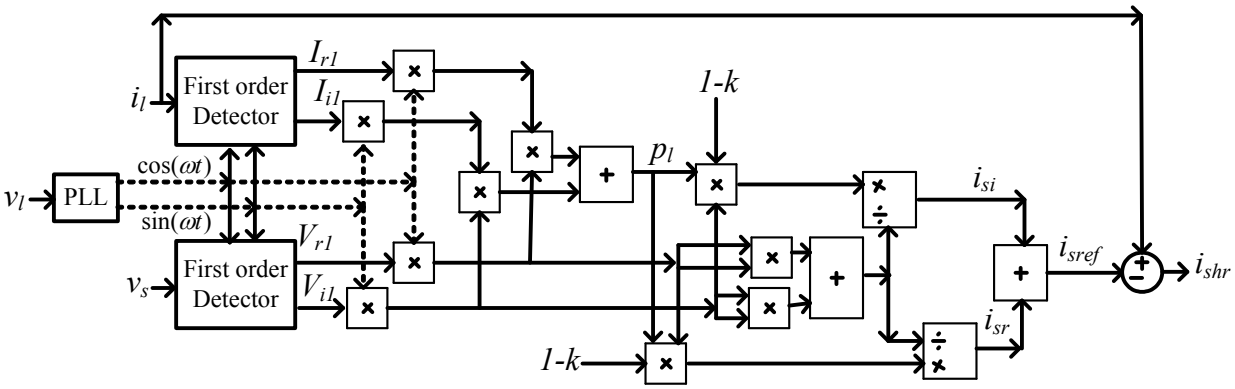

Fig. 4. Block diagram of the parallel active filter reference signal extraction

of the source side current can be determined as Eq. (5). As mentioned, the source voltage is pure sinusoidal with sag and swell. For that, first order component of the source voltage has been used in Eq. (5).

$$\begin{bmatrix} i_{sr}(t) \\ i_{si}(t) \end{bmatrix} = \frac{1}{v_{r1}^2(t)+v_{i1}^2(t)} \begin{bmatrix} v_{r1}(t) & -v_{i1}(t) \\ v_{i1}(t) & v_{r1}(t) \end{bmatrix} \begin{bmatrix} p_s(t) \\ q_s(t) \end{bmatrix} \quad (5)$$

Where, $p_s(t)$ and $q_s(t)$ are the source side active and reactive powers. Also $i_{sr}(t)$ and $i_{si}(t)$ are active and reactive components of the source side current respectively. For reactive power compensation of the source side, in Eq. (6), $q_s(t)$ has been set to zero. Also for supplying k percent of the main component of the load active power by the PAF, related active power ($P_l(t)$) in Eq. (6) has been set to (1-k)$P_l(t)$. Where, $P_l(t)$ is determined as Eq. (7). Because $P_l(t)$ is the main component of the load active power, first order component of the load current has been used in Eq. (7). So the reference currents of the source and PAF can be determined as Eqs. (8) and (9) respectively. Fig. 4, shows block diagram of the parallel active filter reference signal extraction circuit which has been designed based on Eqs. (6-9).

$$\begin{bmatrix} i_{sr}(t) \\ i_{si}(t) \end{bmatrix} = \frac{1}{v_{r1}^2(t)+v_{i1}^2(t)} \begin{bmatrix} v_{r1}(t) & -v_{i1}(t) \\ v_{i1}(t) & v_{r1}(t) \end{bmatrix} \begin{bmatrix} (1-k)p_l(t) \\ 0 \end{bmatrix} \quad (6)$$

$$\begin{aligned} p_l(t) &= v_{r1}(t)i_{r1}(t) + v_{i1}(t)i_{i1}(t) \\ i_{r1}(t) &= I_{r1}\sin(\omega t) \\ i_{i1}(t) &= I_{i1}\cos(\omega t) \end{aligned} \quad (7)$$

$$i_{sref}(t) = i_{sr}(t) + i_{si}(t) \quad (8)$$

$$i_{shr} = i_l - i_{sref} \quad (9)$$

5. Dynamic and State Space Analysis of the Proposed Configuration

For control of the proposed configuration and tracking of the reference signals of the series and shunt cycloconverters, state-space averaging method has been used in this paper [18-20], and the related equations have been obtained, as follows:

$$\begin{aligned} X^{\bullet} &= AX + BU \\ Y &= C^T X \end{aligned} \quad (10)$$

Where, X, is the state space variable vector, and U, is the input vector, which are defined as follows:

$$X = \begin{bmatrix} i_{se} \\ i_{sh} \\ v_{se} \end{bmatrix} \text{ and } U = \begin{bmatrix} v_p \\ v_l \end{bmatrix} \quad (11)$$

Where, i_{se}, i_{sh}, v_{se}, and v_l are the series APF current, shunt APF current, series APF voltage, and the load voltage respectively. So, state space equation of the proposed converter can be as Eq. (12).

$$\begin{bmatrix} i_{se}^{\bullet} \\ i_{sh}^{\bullet} \\ v_{se}^{\bullet} \end{bmatrix} = A.\begin{bmatrix} i_{se} \\ i_{sh} \\ v_{se} \end{bmatrix} + B.\begin{bmatrix} v_p \\ v_l \end{bmatrix} \tag{12}$$

Equivalent circuits of six related modes of Table 1, have been shown in Fig. 5. As mentioned before the primary voltage of the high frequency isolation transformer is a bipolar square wave AC voltage with high frequency and duty cycle equal to 50%. Mode I, II and III show equivalent circuit for its positive half period and mode IV, V and VI show equivalent circuit for its negative half period. Where, R_1 is the series capacitor snubber resistance. In Fig. 5, load has been modeled by R_2. States of switches in Table 1, determine polarity of v_{se} and v_l in the mentioned modes. State equation for each mode of Fig. 5, can be determined as Table 2.

The IOFL method uses average of A_i and B_i matrixes of Table 2 (i=1-6) as follows.

$$A = \frac{\varphi_1}{2\pi}A_1 + \frac{\varphi_2-\varphi_1}{2\pi}A_2 + \frac{\pi-\varphi_2}{2\pi}A_3 + \frac{\varphi_1}{2\pi}A_4 + \frac{\varphi_2-\varphi_1}{2\pi}A_5 + \frac{\pi-\varphi_2}{2\pi}A_6 \tag{13}$$

Table 2. State space equation for each mode

$X^{\bullet} = A_1X + B_1U$	$Y = C_1^T X$	$0 < \theta < \varphi_1$
$X^{\bullet} = A_2X + B_2U$	$Y = C_2^T X$	$\varphi_1 < \theta < \varphi_2$
$X^{\bullet} = A_3X + B_3U$	$Y = C_3^T X$	$\varphi_2 < \theta < \pi$
$X^{\bullet} = A_4X + B_4U$	$Y = C_4^T X$	$\pi < \theta < \pi + \varphi_1$
$X^{\bullet} = A_5X + B_5U$	$Y = C_5^T X$	$\pi + \varphi_1 < \theta < \pi + \varphi_2$
$X^{\bullet} = A_6X + B_6U$	$Y = C_6^T X$	$\pi + \varphi_2 < \theta < 2\pi$

And,

$$B = \frac{\varphi_1}{2\pi}B_1 + \frac{\varphi_2-\varphi_1}{2\pi}B_2 + \frac{\pi-\varphi_2}{2\pi}B_3 + \frac{\varphi_1}{2\pi}B_4 + \frac{\varphi_2-\varphi_1}{2\pi}B_5 + \frac{\pi-\varphi_2}{2\pi}B_6 \tag{14}$$

So A is:

$$A = \begin{bmatrix} \frac{-r_{se}}{L_{se}} & 0 & \frac{-1}{L_{se}} \\ 0 & \frac{-r_{sh}}{L_{sh}} & 0 \\ \frac{1}{C_{se}} & 0 & \frac{-1}{R_1C_{se}} \end{bmatrix} \tag{15}$$

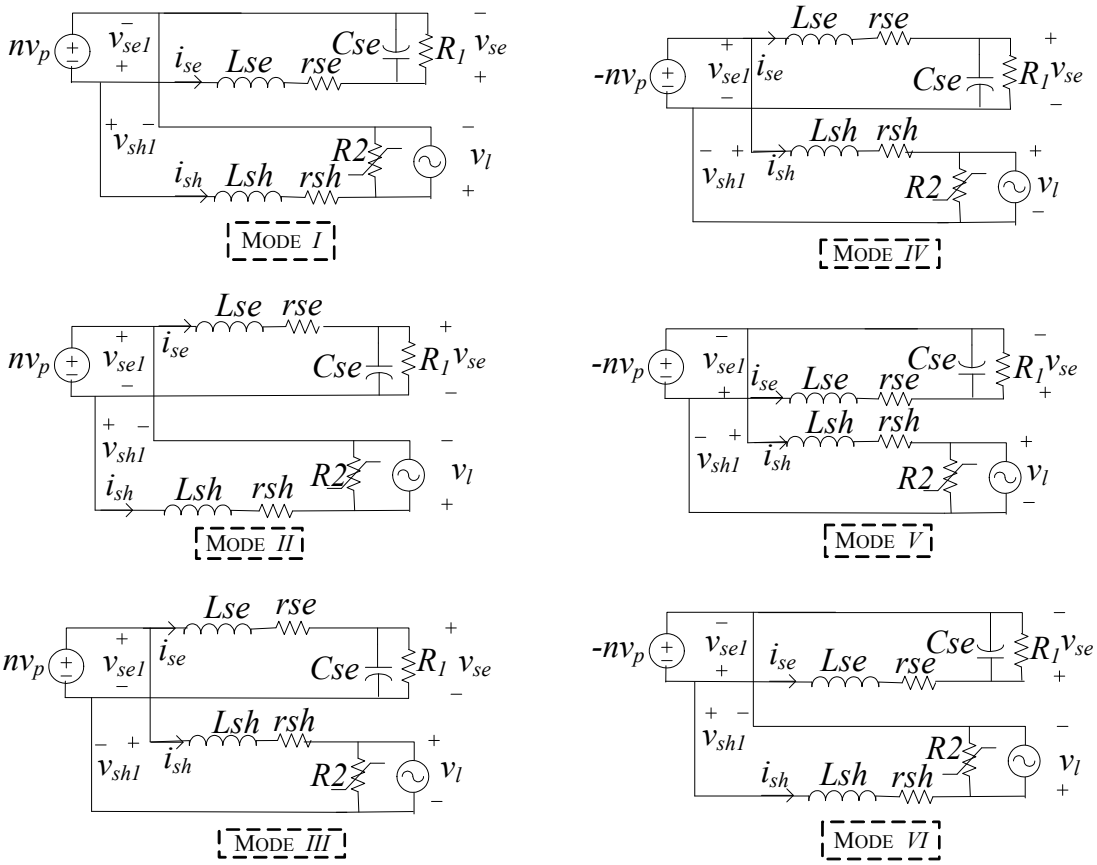

Fig. 5. Equivalent circuits of related modes

And B is:

$$B=\begin{bmatrix} \dfrac{n(\pi-2\varphi_1)}{L_{se}\pi} & 0 \\ \dfrac{n(\pi-2\varphi_2)}{L_{sh}\pi} & \dfrac{-1}{L_{sh}} \\ 0 & 0 \end{bmatrix} \tag{16}$$

5.1 Nonlinear control of the proposed UPQC based on IOFL method

The purpose of the proposed controller is the regulation of the output signals of series and shunt cycloconverters to the desired values by controlling the phase shifts of φ_1 and φ_2. By reordering the Eq. (12), the state space equation can be rewritten as follows:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \end{bmatrix} = f(x)+g(x)\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}+p(x)d \tag{17}$$

Where, *d* is disturbance vector, *x* is state-space vector, *u* is new input vector, *f(x)* is smooth vector field, *g(x)* is smooth vector field for input u and *p(x)* is smooth vector field related to the disturbance d [19].

State space and input vectors are as:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \end{bmatrix}=\begin{bmatrix} \dot{i_{se}} \\ \dot{i_{sh}} \\ \dot{v_{se}} \end{bmatrix},\quad u=\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}=\begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix} \tag{18}$$

So state space equation can be written as:

$$\begin{bmatrix} \dot{i_{se}} \\ \dot{i_{sh}} \\ \dot{v_{se}} \end{bmatrix}=\begin{bmatrix} \dfrac{-r_{se}}{L_{se}}x_1-\dfrac{1}{L_{se}}x_3+\dfrac{nv_p}{L_{se}} \\ \dfrac{-r_{sh}}{L_{sh}}x_2+\dfrac{nv_p}{L_{sh}}-\dfrac{v_l}{L_{sh}} \\ \dfrac{1}{C_{se}}x_1 \end{bmatrix}+\begin{bmatrix} \dfrac{-2nv_p}{\pi L_{se}} & 0 \\ 0 & \dfrac{-2nv_p}{\pi L_{sh}} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix}+ \tag{19}$$

$$\begin{bmatrix} 0 \\ 0 \\ -\dfrac{1}{C_{se}} \end{bmatrix}\frac{v_{se}}{R_1}$$

Where functions of *f(x)*, *g(x)*, *p(x)* and d are as:

$$f(x)=\begin{bmatrix} \dfrac{-r_{se}}{L_{se}}x_1-\dfrac{1}{L_{se}}x_3+\dfrac{nv_p}{L_{se}} \\ \dfrac{-r_{sh}}{L_{sh}}x_2+\dfrac{nv_p}{L_{sh}}-\dfrac{v_L}{L_{sh}} \\ \dfrac{1}{C_{se}}x_1 \end{bmatrix} \tag{20}$$

$$g(x)=\begin{bmatrix} \dfrac{-2nv_p}{\pi L_{se}} & 0 \\ 0 & \dfrac{-2nv_p}{\pi L_{sh}} \\ 0 & 0 \end{bmatrix} \tag{21}$$

$$p(x)=\begin{bmatrix} 0 \\ 0 \\ \dfrac{-1}{C_{se}} \end{bmatrix} \tag{22}$$

$$d=\frac{v_{se}}{R_1} \tag{23}$$

By changing equilibrium point to *x**, where $f(x)\big|_{x^*}=0$ [19], the nonlinear system is defined, as follows:

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \end{bmatrix}=\begin{bmatrix} \dfrac{-r_{se}}{L_{se}}x_1-\dfrac{1}{L_{se}}x_3 \\ \dfrac{-r_{sh}}{L_{sh}}x_2 \\ \dfrac{1}{C_{se}}x_1 \end{bmatrix}+\begin{bmatrix} \dfrac{-2nv_p}{\pi L_{se}} & 0 \\ 0 & \dfrac{-2nv_p}{\pi L_{sh}} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \varphi_1 \\ \varphi_2 \end{bmatrix}+\begin{bmatrix} 0 \\ 0 \\ -\dfrac{1}{C_{se}} \end{bmatrix}d \tag{24}$$

In IOFL method, the outputs are differentiated until appearance of inputs which the number of derivatives required for each output (r_j) is called the relative degree of *j*-th output and total degree of the system is the sum of all outputs relative degrees [19]. In the proposed system, degree of the first output ($x_2=i_{sh}$) is one but degree of the second output ($x_3=v_{se}$) is two then total degrees is equal to 3. In the proposed system, differentiated equations can be written based on *Z*. Which *Z*, is a helping parameter vector as:

$$z_1=x_2, z_2=x_3, z=\begin{bmatrix} z_1 \\ z_2 \\ z_3=\dot{z_2} \end{bmatrix} \tag{25}$$

The state-space equations in the new coordinate can be

defined at the systems equilibrium point as Eq. (26):

$$z^{\bullet}=\begin{bmatrix} x_2^{\bullet} \\ x_3^{\bullet} \\ \dfrac{1}{C_{se}}x_1^{\bullet} \end{bmatrix}=\begin{bmatrix} \dfrac{-r_{sh}}{L_{sh}}x_2-\dfrac{2nv_p}{\pi L_{sh}}\varphi_2 \\ \dfrac{1}{C_{se}}x_1 \\ \dfrac{-r_{se}}{C_{se}L_{se}}x_1-\dfrac{1}{C_{se}L_{se}}x_3-\dfrac{2nv_p}{\pi C_{se}L_{se}}\varphi_1 \end{bmatrix} \quad (26)$$

This equation will be used to define the control law. To ensure that z_1 and z_2 are adjusted respectively to the desired reference values of $Y_{r1}=i_{shr}$ and $Y_{r2}=v_{ser}$, the stabilizing controller is designed by using pole-placement linear control strategy. The new control inputs are expressed by Eqs. (27) and (28):

$$\begin{bmatrix} e_1 \\ e_2 \\ e_3=e_2^{\bullet} \end{bmatrix}=\begin{bmatrix} z_1-Y_{r1} \\ z_2-Y_{r2} \\ z_2^{\bullet}-Y_{r2}^{\bullet} \end{bmatrix}=\begin{bmatrix} z_1-Y_{r1} \\ z_2-Y_{r2} \\ z_3-Y_{r2}^{\bullet} \end{bmatrix} \quad (27)$$

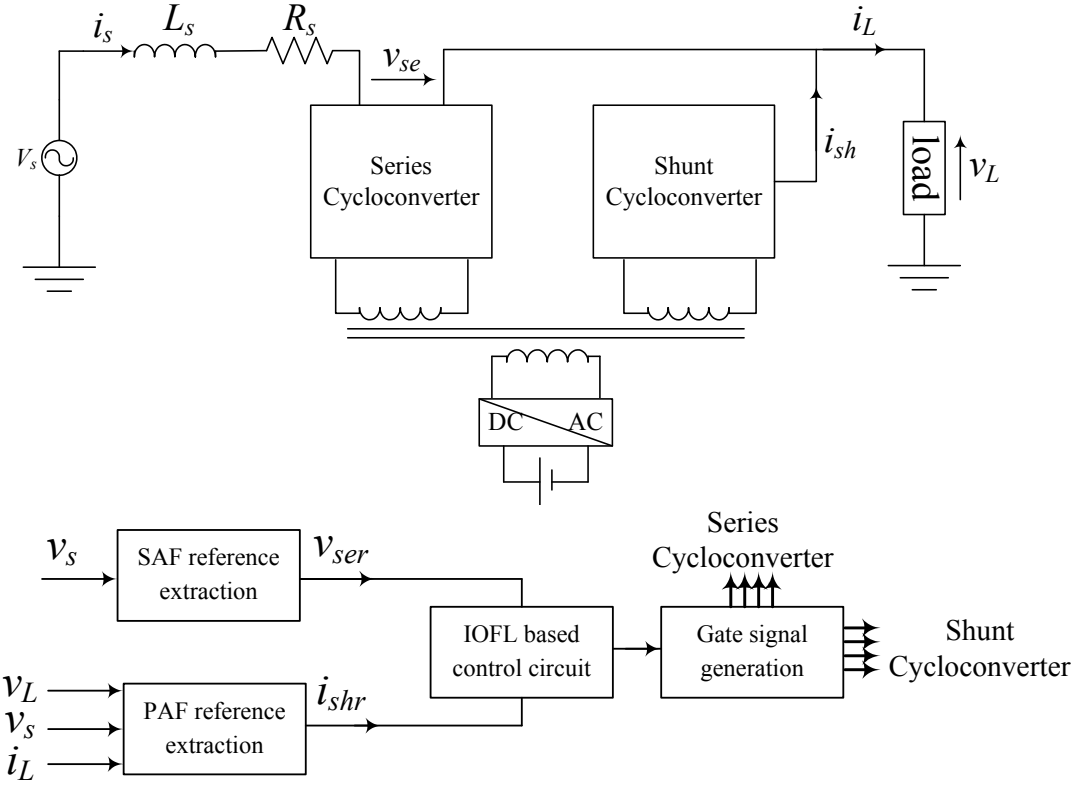

Fig. 6. Overal block diagram of power and control system

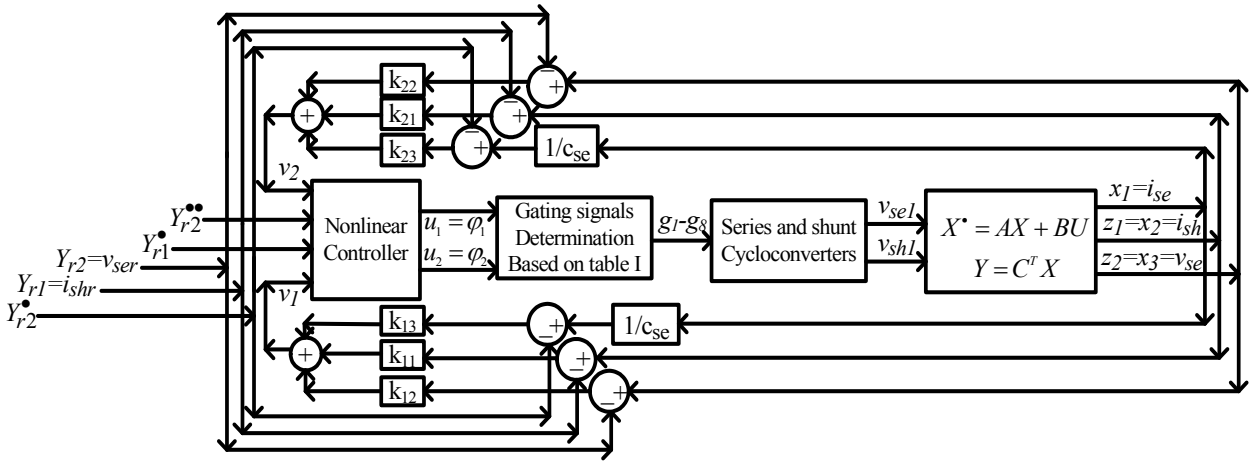

Fig. 7. State space model of the proposed system

$$\begin{bmatrix} e_1^{\bullet} \\ e_2^{\bullet} \\ e_3^{\bullet} \end{bmatrix} = \begin{bmatrix} z_1^{\bullet} - Y_{r1}^{\bullet} \\ z_2^{\bullet} - Y_{r2}^{\bullet} \\ z_3^{\bullet} - Y_{r2}^{\bullet\bullet} \end{bmatrix} = \begin{bmatrix} z_1^{\bullet} - Y_{r1}^{\bullet} \\ e_3 \\ z_3^{\bullet} - Y_{r2}^{\bullet\bullet} \end{bmatrix} \tag{28}$$

By substituting $x=x-x^*$, Eq. (28) can be written as:

$$\begin{bmatrix} e_1^{\bullet} \\ e_2^{\bullet} \\ e_3^{\bullet} \end{bmatrix} = \begin{bmatrix} -\frac{r_{sh}}{L_{sh}}(x_2 - x_2^*) - \frac{2nv_p}{\pi L_{sh}}\varphi_2 - y_{r1}^{\bullet} \\ e_3 \\ \frac{1}{C_{se}}[-\frac{r_{se}}{L_{se}}(x_1 - x_1^*) - \frac{1}{L_{se}}(x_3 - x_3^*)] - \frac{2nv_p}{\pi C_{se}L_{se}}\varphi_1 - y_{r2}^{\bullet\bullet} \end{bmatrix} =$$

$$\begin{bmatrix} v_2 \\ e_3 \\ v_1 \end{bmatrix} = \begin{bmatrix} k_{21}e_1 + k_{22}e_2 + k_{23}e_3 \\ e_3 \\ k_{11}e_1 + k_{12}e_2 + k_{13}e_3 \end{bmatrix} \tag{29}$$

Based on Eq. (29), φ_1 and φ_2 are determined as Eq. (30):

$$\varphi_1 = (-v_1 - y_{r2}^{\bullet\bullet} + \frac{1}{C_{se}}[-\frac{r_{se}}{L_{se}}(x_1 - x_1^*) - \frac{1}{L_{se}}(x_3 - x_3^*)])\frac{\pi C_{se}L_{se}}{2nv_p}$$

$$\varphi_2 = [-v_2 - y_{r1}^{\bullet} - \frac{r_{sh}}{L_{sh}}(x_2 - x_2^*)]\frac{\pi L_{sh}}{2nv_p} \tag{30}$$

Where, v_1 and v_2 (the control laws) are determined as Eq. (31) too.

$$\begin{aligned} v_1 &= k_{11}e_1 + k_{12}e_2 + k_{13}e_3 \\ v_2 &= k_{21}e_1 + k_{22}e_2 + k_{23}e_3 \end{aligned} \tag{31}$$

A stable system will be access with negative values of k_{ij}. Fig. 6 shows overall block diagram of the power and control system and Fig. 7, shows state space model of the proposed system. As shown in Fig. 7, the phase shifts of φ_1 and φ_2 can be controlled in a way for accessing the reference output signals of the series and shunt cycloconverters by using IOFL based control system. V_{ser} and i_{shr} stands for reference signals of series and shunt cycloconverters respectively but v_{se} and i_{sh} stands for real amount of them respectively.

6. Stability Analysis

Based on Eq. (29), state space equation of the control signals can be written as:

$$\begin{bmatrix} e_1^{\bullet} \\ e_2^{\bullet} \\ e_3^{\bullet} \end{bmatrix} = \begin{bmatrix} k_{21} & k_{22} & k_{23} \\ 0 & 0 & 1 \\ k_{11} & k_{12} & k_{13} \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \end{bmatrix} \tag{32}$$

For stability analysis eigenvalues of the coefficient matrix in Eq. (32) should be in left side of $j\omega$ axes. Eigenvalues can be found from Eq. (33).

$$\begin{vmatrix} s - k_{21} & -k_{22} & -k_{23} \\ 0 & s & -1 \\ -k_{11} & -k_{12} & s - k_{13} \end{vmatrix} = 0$$

$$s^3 + s^2(-k_{13} - k_{21}) + s(-k_{12} + k_{21}k_{13} - k_{11}k_{23}) + (k_{21}k_{12} - k_{11}k_{22}) = 0 \tag{33}$$

Based on routh-hurwitz theory for stability condition, Eq. (34) should be satisfied. So permissible area for k_{ij} can be found.

$$\begin{aligned} &(-k_{13} - k_{21}) > 0 \\ &(-k_{12} + k_{21}k_{13} - k_{11}k_{23}) > 0 \\ &(k_{21}k_{12} - k_{11}k_{22}) > 0 \\ &\frac{(-k_{13} - k_{21})(-k_{12} + k_{21}k_{13} - k_{11}k_{23}) - (k_{21}k_{12} - k_{11}k_{22})}{(-k_{12} + k_{21}k_{13} - k_{11}k_{23})} > 0 \end{aligned} \tag{34}$$

For stability condition, amounts of k_{ij} should satisfy related terms of Eq. (34).

7. Simulation Results

For investigation of validity of the proposed control strategy in power quality compensation of a distribution system, the parameters of the converter given in Table 3, have been used in simulations and building the prototype.

Table 3. Three-port converter parameters

Converter parameters	Value
Switching frequency, fs	15.8 kHz
L_{sh}	2 mH
L_{se}	50 mH
C_{se}	2 uF
Input voltage, v_{dg} (DC DG)	40 V
Load voltage, v_l	220 V, 50Hz
Transformer winding ratio, n	n = 10

The UPQC input port uses a 40V DC source, to model a DC DG. The AC grid voltage is 220V, 50Hz. In this simulation an RC load with nominal power of 25 VA has been selected as a consumer. Also for investigation of the proposed converter capability in load change condition, amount of the load has been reduced in time 2sec. The proposed UPQC has been simulated to investigating of its responsibility in load current harmonics reactive power and voltage sag/swell compensation too. The simulation of operating conditions has been carried out for 2.4 seconds to study of the proposed converter. Fig. 8, shows simulation results of the source voltage, SAF voltage, and load voltage

too. As shown in Fig. 8, source voltage sag and swell have been compensated by the proposed configuration. Fig. 9, shows simulation results of the load current, PAF current and source current too. In this figure parameter of i_{sh} (i_f) is related to the parallel active filter current. As shown in Fig. 9, load current harmonics have been compensated by the proposed UPQC-DG. Also Fig. 10, shows simulation results of the source, load, SAF and PAF active and reactive powers. In this figure, p_{sh} (p_f) is related to active power of shunt active filter. In this simulation, value of k has been set to 55 percent. As shown in Figs. 8, 9, and 10 the operating conditions can be divided to following six stages.

Stage one (0≤t<0.4sec):
The source voltage is normal with magnitude of 310V.

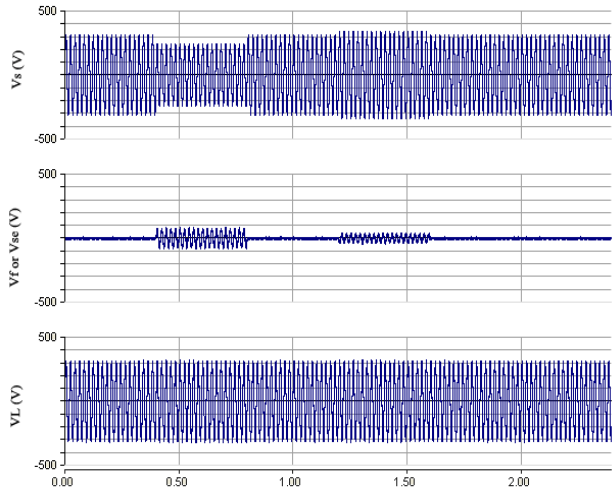

Fig. 8. Simulation result of the source voltage, SAF voltage and load voltage

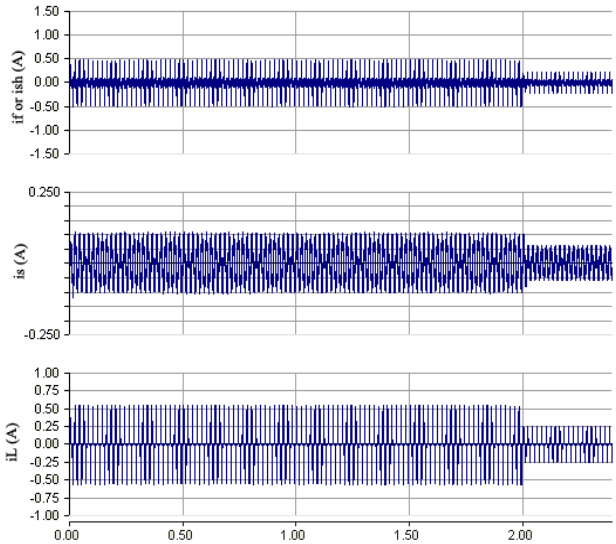

Fig. 9. Simulation result of the load current, PAF current and source current

The SAF of UPQC-DG voltage is 0V. This is for that there is no sag or swell.

The active power of the load (P_l=23W) is feed from the source (P_s=10W) and PAF of UPQC-DG (P_{sh}=13W).

The load injects reactive power to the grid (Q_l=-8Var) and UPQC absorbs all of this reactive power (Q_{sh}=-8Var). Then the reactive power of the source is about 0VAR.

Stage two (0.4≤t<0.8sec):
The source voltage has sag with magnitude of 70 V.

The SAF of UPQC-DG voltage is about 70 V. This is for compensation of voltage sag. Then the load voltage has been normal with magnitude of 310V.

The active power of the load (P_l=23W) is feed from the source (P_s=10W), PAF of UPQC (P_{sh}=10W) and SAF of UPQC (P_{se}=3W).

Like stage one, load injects reactive power to the grid (Q_l=-8Var) and UPQC absorbs all of this reactive power (Q_{sh}=-8Var). Then the reactive power of the source is about 0 VAR.

Stage three (0.8≤t≤1.2sec): This stage is like stage one.

Stage four (1.2 ≤t<1.6sec):
The source voltage has swell with magnitude of 30 V.

The SAF of UPQC compensates voltage swell. Then the load voltage is normal with magnitude of 310V.

The active power of the load (P_l=23W) is feed from the source (P_s=10W), PAF of UPQC (P_{sh}=14W) and SAF of UPQC (P_{se}=-1W). SAF of UPQC absorbs 1W in this condition.

Like stage one, load injects reactive power to the grid (Q_l=-8Var) and UPQC absorbs all of this reactive power (Q_{sh}=-8Var). Then the reactive power of the source is about 0 VAR.

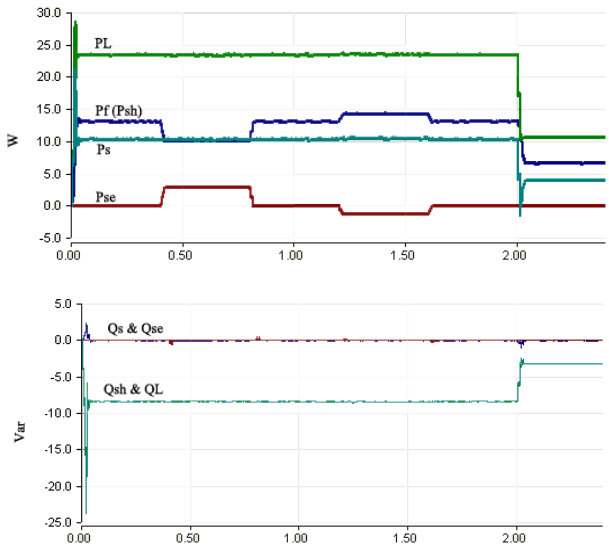

Fig. 10. Simulation results of load, source, SAF and PAF active and reactive powers

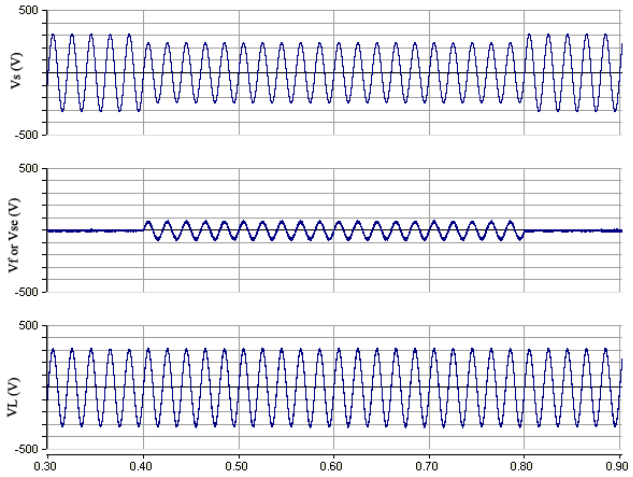

Fig. 11. Simulation of sag compensation

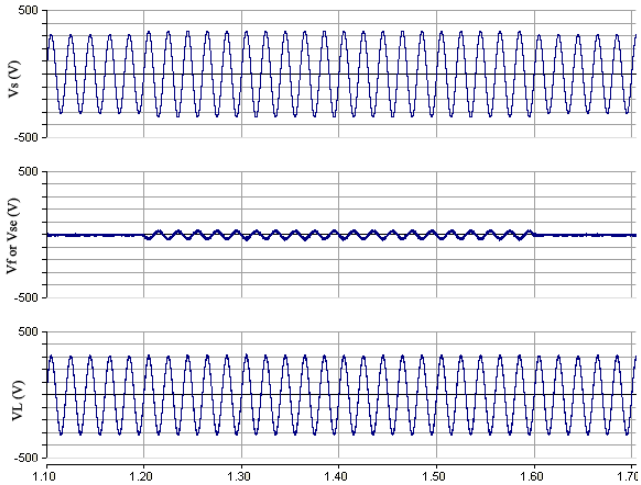

Fig. 12. Simulation of swell compensation

Stage five (1.6≤t≤2sec): This stage is like stage one.

Stage six (2≤t≤2.4sec):

The source voltage is normal with magnitude of 310 V.

The SAF of UPQC voltage is 0 V. This is for that there is no sag or swell.

The active power of the load (P_l) decrease to 10W which is feed from the source (P_s=4.5W) and UPQC (P_{sh}=5.5W).

The load injects 3VAR reactive power to the grid and UPQC absorbs that. Then the reactive power of the source is about 0 VAR.

As mentioned earlier voltage sag (70 V), has been carried between 0.4sec and 0.8sec. Fig. 11 shows the simulation results of SAF between 0.3sec and 0.9sec. This is for investigation of capability of the proposed configuration in sag compensation clearly. As shown in Fig. 11, UPQC is compensates the voltage sag so the load voltage is normal with magnitude of 310 V.

Also as mentioned before a voltage swell (30V), has been carried between 1.2sec and 1.6sec. Fig. 12 shows the simulation results of SAF between 1.1sec and 1.7sec clearly. This is for investigation of capability of the proposed configuration in swell compensation. As shown in Fig. 12, UPQC compensates the voltage swell so the load voltage is normal with magnitude of 310 V.

Fig. 13. Simulation results of compensator current (i_{sh}), source current (i_s), and load current (i_l)

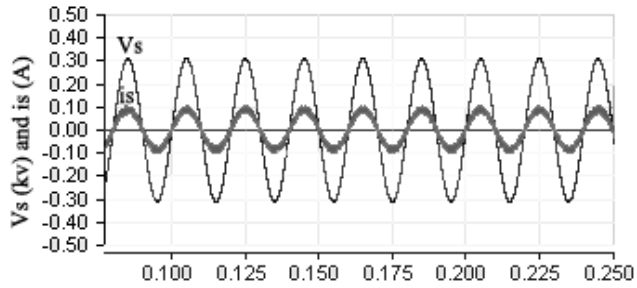

Fig. 14. Simulation results of the source current and voltage

In Fig. 13 the simulation results of the shunt part of the proposed UPQC for a few cycles has been shown clearly. The proposed UPQC has compensated the harmonics of the load current. In Figs. (8, 11) and (12) parameter of v_{se} (v_f) is related to the series active filter voltage. Also, in Figs. (9) and (13) parameter of i_{sh} (i_f) is related to the shunt active filter current. Fig. 14 represents simulation results of the source current and voltage simultaneously. Source current is sinusoidal with no phase difference with the voltage. As the other word UPQC has compensated the load reactive power.

8. Experimental results

A prototype has been built in order to test the performance of the proposed UPQC and its control strategy. The controllers have been derived by a DSP 320F28335. The UPQC and load have been connected to the grid at the point of the common coupling (PCC). The MOSFETs are

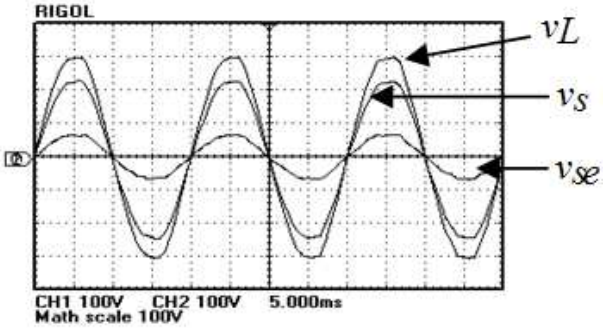

Fig. 15. Experimental results of source voltage (v_s), load voltage (v_l) and compensator voltage (v_{se})

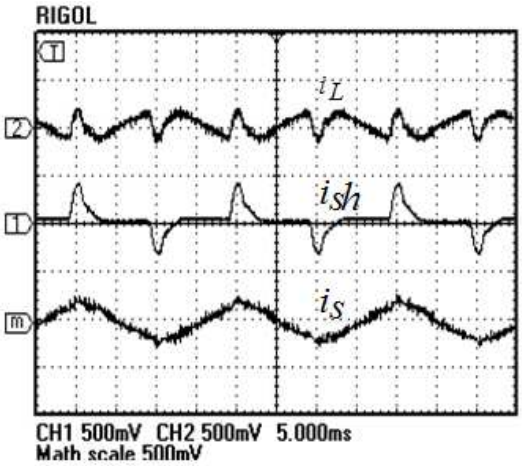

Fig. 16. Experimental results of load current (i_l), compensator current (i_{sh}), and source current (i_s)

IRFP560 and the switching frequency is 15.8 kHz.

Fig. 15, shows the experimental results of SAF for a few cycles. In this figure, there is a voltage sag (70 V) in grid side (v_s), then series part of UPQC compensates sag (v_{se}) and the load voltage is normal with magnitude of 310 V (v_l). In Fig. 16, the experimental results of the shunt part of the proposed UPQC have been shown. The load current (i_l) has harmonics and UPQC compensates the harmonics as well as reactive power. As shown in Fig 16 experimental results are satisfactory. Also Fig. 17 shows experimental results of the source, SAF and PAF active powers experimental that has good agreement with Fig. 10. Fig. 18 shows results of the source, load, SAF and PAF reactive powers that has good agreement with Fig. 10. The control board generates output current and voltage, as well as the PWM-switching orders. Fig. 19 shows the electronic circuit of the control board and PWM-switching orders. The circuit is divided into different blocks. The CSN151-100 current sensors have been used to measure the output currents of the converters, while the LEM LV25-P voltage sensors have been used to measure the output voltage of load, SAF and source. Several TL084s have been used as

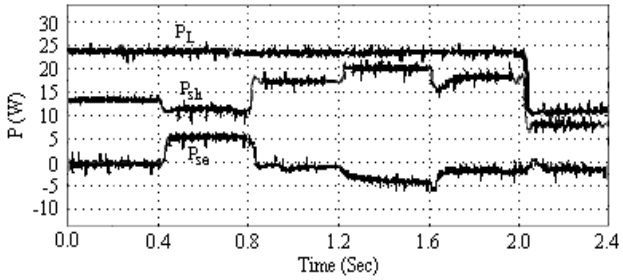

Fig. 17. Experimental results of active powers

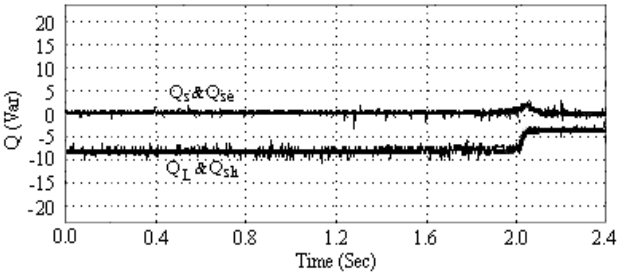

Fig. 18. Experimental results of reactive powers

operational amplifiers. The PWM switching orders have been generated by means of DSP 320F28335. TLP250 optocouplers have been used to enhance the produced voltage of DSP 320F28335.

9. Conclusions

A novel configuration of UPQC-DG for low DC output DGs has been proposed which could be used in power quality compensation of distribution networks with presence of nonlinear loads. The proposed configuration has been composed of one full-bridge inverter, one three winding high frequency transformer and two cyclo-converters. One of the cycloconverters has been as a series APF and the other one as a shunt APF connected to the grid directly. In the proposed configuration a DC capacitor has been omitted and an energy source has been provided by DGs. Proposed configuration not only could compensate power quality problems but also could supply a part of load power.

The electrical isolation between input and output ports has been provided with high frequency transformer, then the size and volume of the converter has been reduced. State space equations of the proposed configuration have been used for dynamic analysis and providing a control based on phase shift with nonlinear control. The results validate the good performance of the proposed configuration in compensation of power quality problems and as the same time supplying the load power partly.

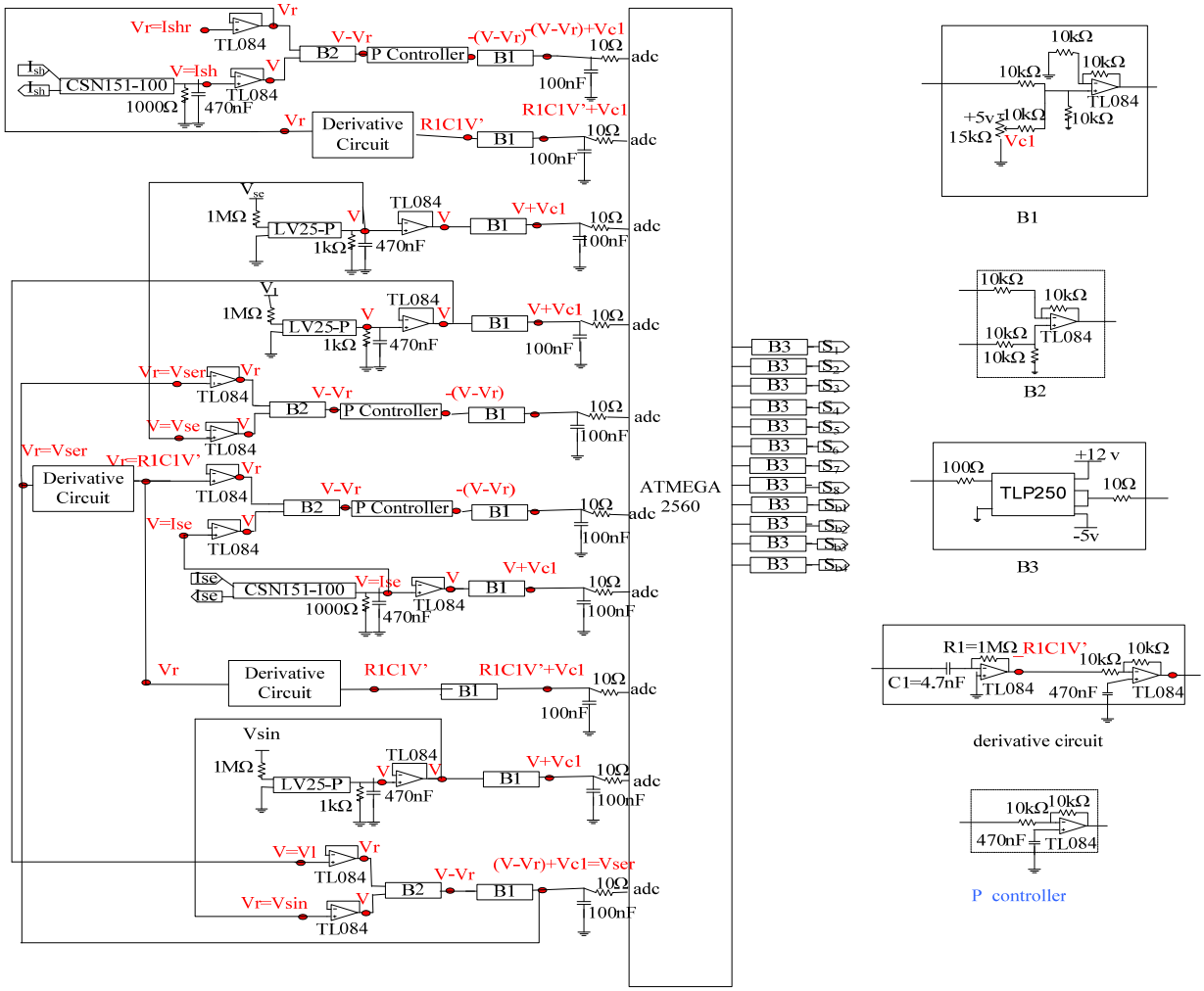

Fig. 19. Electronic circuit of control board

Acknowledgment

This research has been supported by Electrical Engineering Department, Research and Science Branch, Islamic Azad University, Tehran, Iran.

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