

Implementation of Robust Prediction Observer Controller for DC-DC Converter

R. Shenbagalakshmi[†] and T. Sree Renga Raja^{*}

Abstract – A discrete controller is designed for low power dc-dc switched mode power supplies. The approach is based on time domain and the control loop continuously and concurrently tunes the compensator parameters to meet the converter specifications. A digital state feedback control combined with the load estimator provides a complete compensation, which further improves the dynamic performance of the closed loop system. Simulation of digitally controlled Buck converter is performed with MATLAB/Simulink. Experimental results are given to demonstrate the effectiveness of the controller using LabVIEW with a data acquisition card (model DAQ Pad – 6009).

Keywords: DC-DC converters, Digital state feedback, Pole placement, Prediction observer, Separation principle

1. Introduction

The dc-dc converters are widely used in many applications such as distributed power supply systems, power factor improvement, harmonic elimination, fuel cell applications and photo voltaic arrays. In power electronic systems, the switched mode dc-dc converters are very popular due to their light weight, compact, more power density, fast dynamics, higher efficiency and smaller size [1-4]. Therefore they are extensively used in personal computers, computer peripherals, communication, medical electronics and adapters of consumer electronic devices to provide different level of voltages [1].

Especially in portable consumer electronics Buck converters play a vital role. Buck converter is very simple in construction and highly efficient. The main challenge in the field of Power Electronics is emphasized more on the control aspects of the dc-dc converters. The control approach requires effective modelling and a thorough analysis of the converters. The switching power converters in general are non-linear and time invariant. The major disadvantage of the Buck converter is its dependence on large passive components. In conventional analog design approaches, control problems are more complex and topology dependent [2]. The major disadvantages include: (i) difficulty in adjusting (ii) System alteration and higher functions are difficult (iii) Low reliability and (iv) sensitivity to noise. Thus Buck converters cannot be analyzed by directly applying the conventional method which in turn leads to the implementation of digital compensators. In low power dc-dc converters, the overload

protection, increased efficiency and improved dynamic response are obtained by current sensing or measurement. The measurement methods are generally voltage drop method and observer based method. In voltage drop method the major drawback is that it decreases the efficiency and requires a wide bandwidth amplifier which is very difficult to realize [3]. Hence the observer plays a vital role in current sensing thereby leading to the design of Observer controller for the dc-dc converters.

In recent years digital controller for power switching converters are being popular due to several advantages such as advanced control strategies, low sensitivity to variations, robustness to ageing and environmental changes, noise immunity and ease of programming. In digital approach the two areas which find significance in the research are, (i) The DPWM (Digital Pulse Width Modulation) signals are generated with highest resolution in order to obtain high accuracy in required output voltage (ii) The digital control algorithms are being developed to fully utilize the features of the controller [4].

In this paper, high resolution DPWM signals are generated keeping the system switching frequency low to provide the state feedback control. The main control objective in the design of controller for the dc-dc converters is to drive the semiconductor switch with a duty cycle so that the dc component of the output voltage is equal to the reference. The regulation should be maintained constant despite variations in the load or in the input voltage. Furthermore, the constraints in the design of controller results due to the duty cycle which is bounded between zero and one. This problem can be solved by modelling the dc-dc converters using state space averaging technique [5]. By using this technique, the converter can be described by a single equation approximately over a number of switching cycles. The averaged model makes the simulation and control design much faster [1].

[†] Corresponding Author: Dept. of Electrical and Electronics Engineering, Mookambigai College of Engineering, Pudukkottai, India. (lakshmi_amrith@yahoo.com)

^{*} Dept. of Electrical and Electronic Engineering, BIT Campus, Anna University, Chennai, India. (renga_raja@rediffmail.com)

Received: October 4, 2012; Accepted: June 5, 2013

The foremost objective of this work is to design a robust compensator based on prediction observer, which overcomes the above mentioned problems. The design is based on time domain in which the converter specifications such as rise time, settling time, maximum peak overshoot and steady state error are met. The dc-dc converters are modelled using state space averaging technique and the discrete observer controller is designed using pole placement technique and separation principle. MATLAB/Simulink is used to perform simulation. The experimental set up has been carried out using LabVIEW program with portable USB DAQ device whose results are illustrated. The sections are organized as follows: Section II discusses the overall block diagram, Section III gives the design of Buck converter, Section IV discusses the modeling, Sections V and VI explain the design of digital state feedback matrix and the prediction observer controller, Sections VII and VIII give the simulation and experimental results, Hardware implementation and conclusion are given in sections IX and X respectively. References and Appendix are included at the end.

2. Overall Block Diagram

The overall block diagram of the dc-dc converter with the entire set up is shown in Fig. 1

The prediction observer controller is designed for the Buck converter using pole placement technique and separation principle. The output voltage of the converter is compared against the desired value of reference voltage using a comparator 1 circuit designed by using operational Amplifier (IC 741). The error output thus obtained is fed in to the in built Block diagram section of the LabVIEW through the data acquisition card, DAQ pad 6009. Inside the Block diagram of the LabVIEW section, the analog to digital conversion takes place and thus the processed signal is fed into the discrete transfer function block in which the designed controller values are entered. The output of this controller thus obtained is acquired back to the hardware set up and fed into comparator 2. Comparator 2 is also

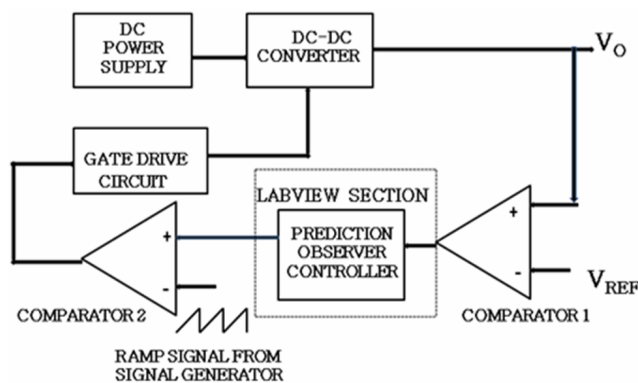


Fig. 1. Overall Block diagram

designed using Operational Amplifier (IC 741). This signal is compared against the ramp signal with desired switching frequency obtained from signal generator. The resulting switching pulses are fed to the MOSFET of the dc-dc converter through the gate drive circuit.

3. Design of Buck Converter

The schematic of Buck converter is shown in Fig. 2.

The dc-dc converters convert an unregulated dc supply into regulated dc voltage to a variable load. The buck converter comprises of an inductor L, a capacitor C, a semiconductor switch and a diode. In the diagram, V_S denotes the input voltage and R denotes the Load resistance. The coil non linearities and the noise which are caused mainly due to the oscillations of stray inductors and parasitic capacitors at each switching instants are neglected. The switch is assumed as ideal [6]. The design of the converter is discussed now.

The output voltage of the Buck converter is always less than the input voltage and is given by,

$$V_o = dV_s \tag{1}$$

where $d = \frac{T_{on}}{T}$ is the duty cycle ratio, T_{on} is the on time of the semiconductor switch and T is the switching period. To ensure the continuous current mode of conduction the selected value of inductance should be greater than the critical value of the inductance L_C which acts as a boundary condition for continuous and discontinuous current mode of operations [1].

The critical value of inductance is given by,

$$L_c = (1-d) \frac{R}{2f_s} \tag{2}$$

where f_s is the switching frequency.

The inductor value must be chosen by considering the fact that the magnitude of the ripple current in the output capacitor as well as the load current is determined by the appropriate inductor value. Hence, normally a ripple current of 10% to 20% of the average output current is assumed for the design to achieve good performance of the

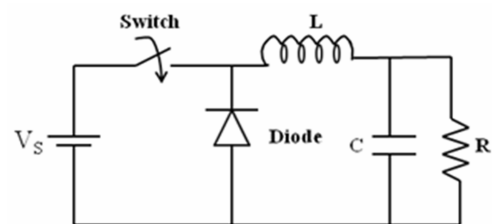


Fig. 2. Schematic diagram of Buck converter

converter. The value of inductor is determined by,

$$\Delta I_L = \frac{V_s T d (1-d)}{L} \quad (3)$$

where T is the time period.

The capacitor value is determined by assuming the output voltage ripple as 1% to 2% of the output voltage. The capacitor value is determined by,

$$\Delta V = \Delta I_L \times \frac{1}{8 f_s C} \quad (4)$$

The following are the parameters considered for the design: $V_s = 48V$, $V_o = 12V$, $f_s = 100 \text{ kHz}$, $L = 720\mu H$, $C = 8.667 \times 10^{-7} F$ and $R = 14.4\Omega$

4. Modelling of Buck Converter

The DC-DC converter is modelled using state space averaging technique. The unique feature of this method is that the design can be carried out for a class of inputs such as impulse, step or sinusoidal function in which the initial conditions are also incorporated. This technique is convenient to use but it offers a low frequency approximation of the true dynamics where the discontinuous effect introduced by the switching is ignored [6]. The state space analysis is discussed now.

The switch is driven by a pulse sequence with a constant switching frequency, f_s . The state vector for this converter is defined as $x(t) = \begin{bmatrix} i_l(t) \\ V_c(t) \end{bmatrix}$, where $i_l(t)$ is the inductor current and $V_c(t)$ is the capacitor voltage. For the given duty cycle $d(k)$ for the k^{th} period, the system is described by the following set of affine continuous time state space equations:

$$\left. \begin{aligned} x(t) &= A_1 x(t) + B_1 V_s(t), s = 1 \\ x(t) &= A_2 x(t) + B_2 V_s(t), s = 0 \end{aligned} \right\} \quad (5)$$

where $s = 1$ represents the condition at which the switch is conducting and $s = 0$ represents the off condition of the switch. The matrices A_1 , A_2 , B_1 and B_2 for the buck converter are given by,

$$A_1 = A_2 = \begin{bmatrix} 0 & -1 \\ 1 & -1 \\ C & RC \end{bmatrix} \quad (6)$$

$$B_1 = \begin{bmatrix} 1 \\ L \\ 0 \end{bmatrix} \quad (7)$$

and

$$B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad (8)$$

The output voltage $V_o(t)$ across the load is expressed as

$$V_o(t) = [0 \ 1] x(t) \quad (9)$$

The continuous state equations are discretized in order that the prediction observer controller has to be designed. It is considered that the discrete system is same as that of the continuous system except that the system is sampled with a sampling time, which is assumed as $1\mu s$. The state space solution is transformed into a sampled system by using the relation $t = kT_s$, where T_s is the sampling time. The equation is described as,

$$x(kT_s) = e^{AKT_s} x(0) + \int_0^{KT_s} e^{A(KT_s-\tau)} Bu(\tau) d\tau \quad (10)$$

where τ is a variable.

With the analog coefficient matrices, discrete counter parts are obtained by using the following relationship,

$$G = e^{AT_s} \quad (11)$$

$$H = \int_{\tau=0}^{T_s} e^{A\tau} d\tau B \quad (12)$$

$$C_d = C \quad (13)$$

$$D_d = D \quad (14)$$

where G , H , C_d and D_d are the coefficient matrices for discrete systems.

The dynamics of the Buck converter for discrete time system is obtained as follows,

$$G = \begin{bmatrix} 0.999 & -0.00138 \\ 0.1148 & 0.9919 \end{bmatrix} \quad (15)$$

$$H = \begin{bmatrix} 3.473 \times 10^{-4} \\ 1.995 \times 10^{-5} \end{bmatrix} \quad (16)$$

5. Closed Loop Control using Digital State Feedback

The digital control objective is to derive the discrete state feedback control and the observer based controller similar to the kalman like filter using pole placement technique. The main intention of the state feedback control is to make the system to track the reference signal which is considered as a step input. Prediction Observer acts as a load estimator and measures the unmeasurable variables. It

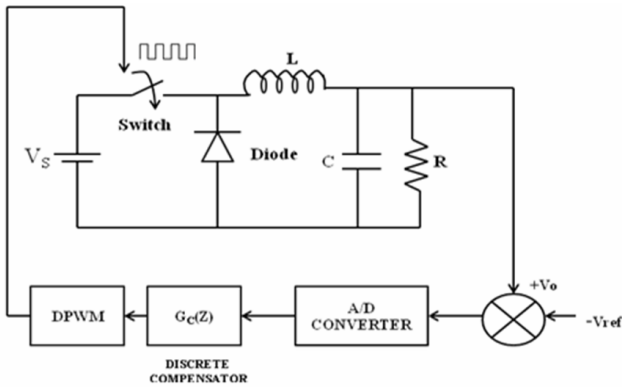


Fig. 3. Closed loop control of Buck Converter

effectively ensures the robustness of the control law. By separation principle, digital state feedback control and Observer poles are combined to provide a dynamic compensation. The closed loop control is illustrated in Fig. 3.

The output voltage is regulated by using the feedback. The feedback ensures that the output must be insensitive to load disturbances, stable and provides good transient response thereby improving the dynamic performances. The error voltage is fed to A/D Converter which samples them at a sampling rate equal to twice the switching frequency. The function of the discrete time compensator is to process the error signals. The output samples control the switch by generating gating pulses when it is processed through DPWM (Digital Pulse Width Modulation) block. The DPWM block includes a sample and hold and it acts as a demodulator. The delay time (t_d) is included in the feedback loop. It includes the A/D conversion time, computational delay, modulator delay and the switch transition time which is taken equal to the switching period. The additional advantages of digital state feedback control include: (i) Implementation of discrete time systems is very easy including Prediction (ii) Effective utilization of observed state variables instead of measured ones and (iii) synchronization of controller operation and pulse width modulation can be achieved effectively.

Fig. 4 shows the Analog to digital converter block. It is an effective device that converts a continuous time signal to a discrete time signal by using sampling. The converter block includes a delay, zero order hold and a quantizer.

The total time between sampling the error signal and updating the duty cycle command at the beginning of the next switching period is carried out by the delay block. The zero order hold is added mainly for modelling the sampling

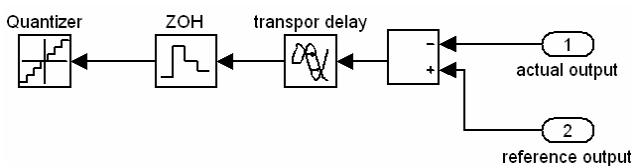


Fig. 4. Analog to Digital Converter

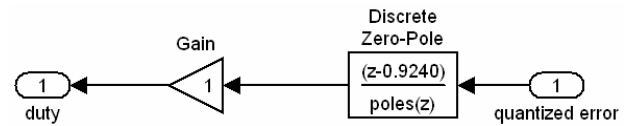


Fig. 5. Discrete time compensation

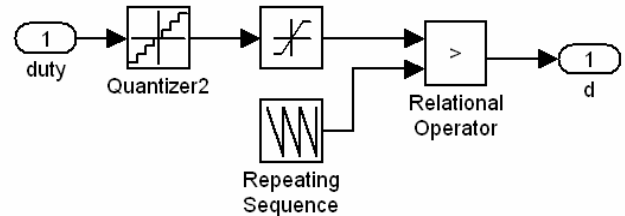


Fig. 6. Digital Pulse width modulation

effect. It reconstructs the continuous time signal by holding the sample one by one for each sampling interval.

Quantizer is mainly used to map a larger set of input values to a smaller set such as rounding values to some unit of precision. The discrete time Compensation block is shown in Fig. 5.

The output of the A/D converter called quantized error is fed to the discrete zero - pole block which in turn is converted into Pulse using DPWM block shown in Fig. 6. The compensator thus designed minimizes the error and send the command signal to the switch in form of pulses in order that the output tracks the reference signal.

The output of the compensator is compared against the ramp signal in order that the duty cycle command for the semiconductor switch is obtained.

6. Design of Robust Digital State Feedback Control Using Pole Placement Technique

The main objective is to choose the state feedback gain matrix based on control law given by $u = -kx(k)$ for the systems under consideration defined by their respective state equations. The desired steady state value of the controlled variable 'y' is a constant reference input 'r', which is taken as a unit step input. The root locus of Buck converter under consideration is drawn from which the desired closed loop poles are chosen for the design of the state feedback gain matrix of the converter. The necessary and sufficient condition for arbitrary pole placement of the system is that the system should be completely controllable and it will be very much simpler to find the state feedback gain matrix when the state equations are in the controllable canonical form [7].

Pole placement technique is an effective one through which it is possible to stabilize a completely controllable system by arbitrarily choosing the closed loop poles. The main objective is to place the closed loop poles arbitrarily in z-plane of the Buck converter in such a way that $y(k)$

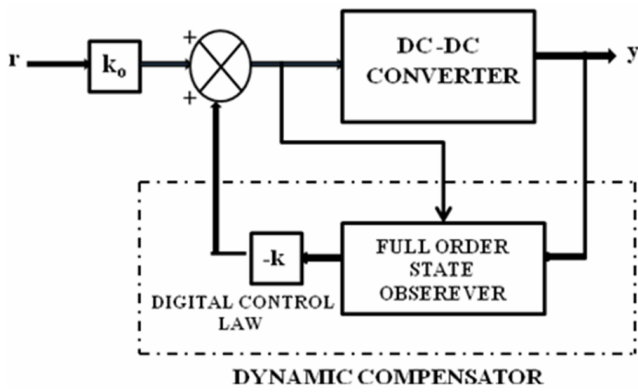


Fig. 7. Control scheme with digital state feedback matrix

track any of the references $r(k)$, which is considered as a step function in this case. The control scheme with digital state feedback is shown in Fig.7.

Here k_0 represents the adjustable gain.

For the state equations under consideration, if we assume that all the n state variables are accurately measured at all times, a linear control law is possible to be implemented which takes the form as $u = -kx(k)$ for the discrete time systems. The dynamic equation of the discrete system with control law is defined as,

$$x(k) = (G - Hk)x(k) \tag{17}$$

With the necessary and sufficient condition that the system should be completely state controllable, if all the Eigen values of $(G-Hk)$ are placed in the left half plane, the closed loop system thus considered is asymptotically stable. The Buck converter under consideration is of second order and the desired poles can be easily placed by assuming the following converter specifications,

$$\left. \begin{aligned} \text{settlingtime} &\approx \frac{4}{\zeta\omega_n} \leq 1\text{ms} \\ \text{Max.PeakOvershoot} &\approx 100e^{-\zeta\pi\sqrt{1-\zeta^2}} \leq 1\% \end{aligned} \right\} \tag{18}$$

$$\left. \begin{aligned} |z| &= e^{-T\zeta\omega_n} \\ \angle z &= \frac{2\pi\omega d}{\omega s} \\ \text{samplingtime} &\approx 1 \times 10^{-6} \text{ s} \end{aligned} \right\} \tag{19}$$

where ζ is the damping ratio and ω_n is the natural frequency of oscillation of the system.

From the desired pole locations the characteristic equation of the converter is given by,

$$\Delta = z^2 + 2\zeta\omega_n z + \omega_n^2 \tag{20}$$

By using the above mentioned assumptions the digital state feedback gain matrix is designed and the values are

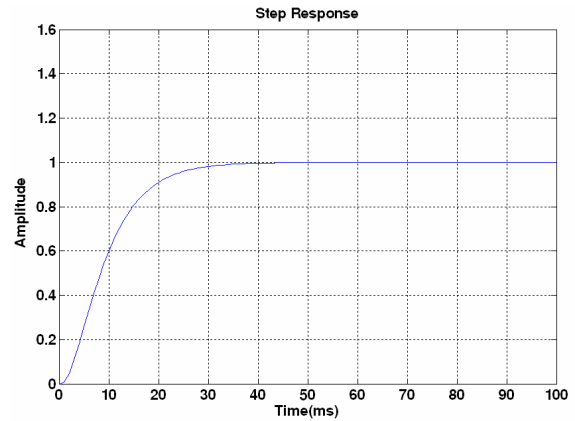


Fig. 8. Step response of the buck converter

obtained as $k_1 = 1079$ and $k_2 = 861$.

Fig. 8 shows the step response tracked by the converter and hence the required dynamics are achieved for the given time domain specifications.

7. Design and Implementation of Full Order Prediction Observer Controller

The control law thus designed is based on the assumption that all the state variables are available for feedback. Since all the states cannot be measured at all times, an estimation scheme employing full order observer is designed in order to replace the true states by their estimates in the control law. If the measurement of the portion of the states is given then all the state variables can be reconstructed by the Prediction Observer. The dynamic equation describing the state estimation is defined as,

$$\hat{x}(k+1) = G\hat{x}(k) + Hu(k) + m(y(k) - C\hat{x}(k)) \tag{21}$$

where \hat{x} is the estimate and m is an $n \times 1$ real constant gain matrix. It is called Prediction Observer since the estimate $\hat{x}(k+1)$ is one sampling period ahead of the measurement $y(k)$. The estimation scheme employing the full order observer is shown in the Fig. 9.

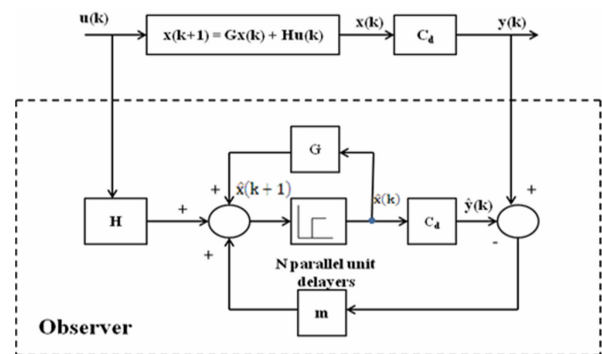


Fig. 9. Load estimator based on prediction observer

The difference equation describing the behaviour of the error is defined as,

$$\tilde{x}(k+1) = (G - mC_d)\tilde{x}(k) \tag{22}$$

Where $x = \tilde{x}$. The characteristic equation of the error is defined as,

$$|zI - (G - mC_d)| = 0 \tag{23}$$

The desired characteristic equation is assumed as,

$$(z - a_1) (z - a_2) \dots (z - a_n) \tag{24}$$

The required elements of m are obtained by matching the coefficients of the Eqs. (23) and (24).

The dynamic compensation can thus be provided to the discrete system under consideration by implementing the state feedback control law using an estimated state vector thereby completing the design of Observer controller with the help of separation principle. The equation describing the Prediction Observer Controller is obtained by including the state feedback control in the Observer equation and is given by,

$$\hat{x}(k+1) = (G - Hk - mC_d)\hat{x}(k) + my(k) \tag{25}$$

$$u(k) = -k\hat{x}(k) \tag{26}$$

The Prediction Observer Controller thus designed for the Buck converter is obtained as,

$$G(z) = \frac{1772z - 16327}{z^2 - 1.118z + 0.4533} \tag{27}$$

Thus by separation principle the digital control law and the state Observer can be designed separately and yet used together to provide a robust dynamic compensation for the second order system under consideration. Since the Observer is mainly designed to check the robustness of the control law, it is essential that the estimated error variables should converge at zero from any non zero initial value. This ensures the asymptotic stability of the system under consideration with the desired pole locations. It is expressed in the Figs.10(a) and Fig.10(b). The error variables for the designed system thus converge at zero thereby ensuring the stability of the system.

8. Simulation Results

The design and performance of Buck converter is accomplished in continuous conduction mode and simulated using MATLAB / Simulink. Simulation has been carried out using the values same as that of the experimental values. The ultimate aim is to achieve a robust controller in spite of uncertainty and large load disturbances. It is evident from Table 1 that the output voltage obtained using digital controller settles down at 0.01s with a rise time of 0.005s. The converter specifications under consideration are rise time, settling time, maximum peak overshoot and steady state errors which are shown compared against its analog counterpart in Table 1.

No overshoots or undershoots are evident and the steady state error observed for load variations is much lesser than 5%. The performance specifications for the Buck converter with digital controller are better than with the analog controller. The results thus obtained with digital controller are in concurrence with the mathematical calculations. It is obvious that the digital system shows improved results than the analog system. The simulation of the Buck converter with digital controller is also carried out by

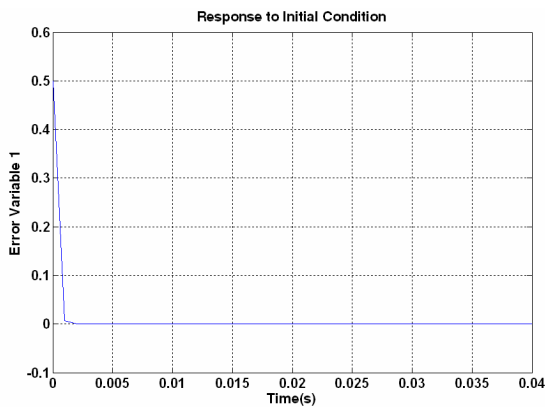


Fig. 10(a). Estimation of Error variable 1

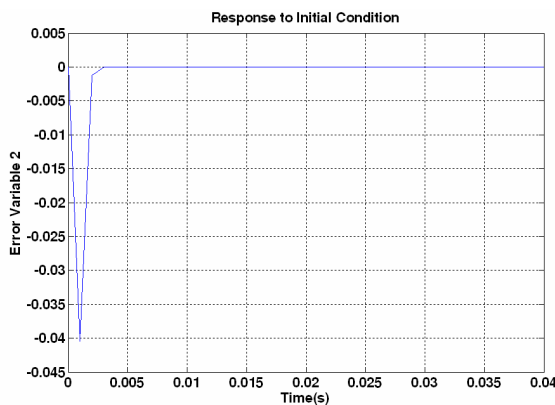


Fig. 10(b). Estimation of Error Variable 2

Table 1. Performance of Buck Converter

Specifications	Digital Controller	Analog Controller
Settling Time(s)	0.01	0.06
Peak Overshoot (%)	0	0
Steady state error(V)	0	0.2
Rise Time(s)	0.0050	0.0420
Output Ripple voltage(V)	0	0

Table 2. Output response for load variations

R(Ω)	L(μ H)	E(V)	Reference voltage(V)	Output Voltage(V)
1.44	-	-	5	5.000
2	-	-	5	5.017
5	-	-	5	5.063
1.44	10×10^{-6}	-	5	5.009
14.44	100×10^{-6}	-	5	5.048
2	100×10^{-6}	3	5	5.041

varying the load not limiting to R load and it is illustrated in Table 2.

It is evident from Table 2 that the controller tracks the reference voltage inspite of the load variations. When the load resistance is varied as 1.44 Ω , 2 Ω and 5 Ω , the Prediction Observer is efficient enough to track the output Voltages as 5.000V, 5.017V and 5.063V respectively for the reference Voltage of about 5V. Again when the inductance of 10 μ H and 100 μ H are added to the load resistance of 1.44 Ω and 14.44 Ω , the output voltage thus obtained is 5.009V and 5.048V respectively. The steady state error thus observed is of the order of 0.1% and 0.2% respectively. The simulation is also carried out again using RLE load with a resistance of 2 Ω , inductance of 100 μ H and an ideal dc voltage source of 3V. The response of the converter is such that the controller is capable to work under all the load transients thereby tracking the voltage as 5.041V.

The simulation is also carried out by varying the input voltage and load resistance and the corresponding, input voltage, output voltage, error, inductor current and load current are shown in Fig. 11 respectively. The input Voltage is first set as 12V until 0.01s and then varied from 12V to 10V and again at 0.02s 10V is varied to 12V. From 12V it is again changed to 14V at 0.03s and finally 12V is set at

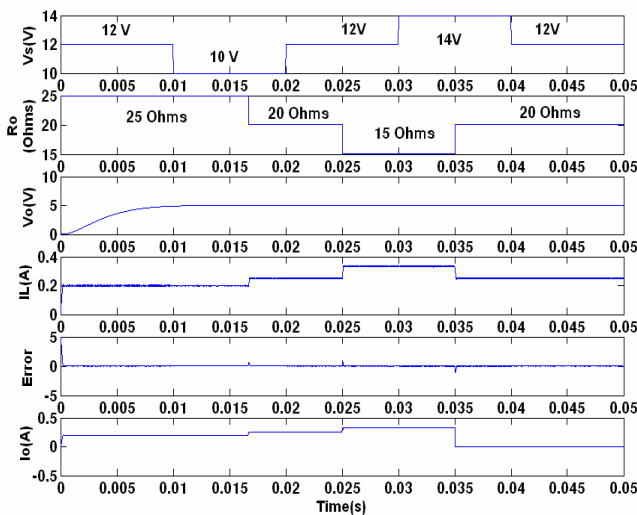


Fig. 11. Output Response of the Buck Converter (V_s – Input Voltage, R_o - Load resistance, V_o – Output Voltage, I_L – Inductor Current, I_o – Load Current)

Table 3. Output Response with Variable Converter Parameters

Sl. No	Inductance (L)	Capacitance (C)	Reference voltage(V)	Output Voltage(V)
1	720.28 μ H	0.8677 μ F	5	5.009
2	600 μ H	1 μ F	5	5.011
3	500 μ H	5 μ F	5	4.992
4	100mH	6 μ F	5	4.981
5	10mH	1 μ F	5	4.981
6	1mH	1mF	5	4.982

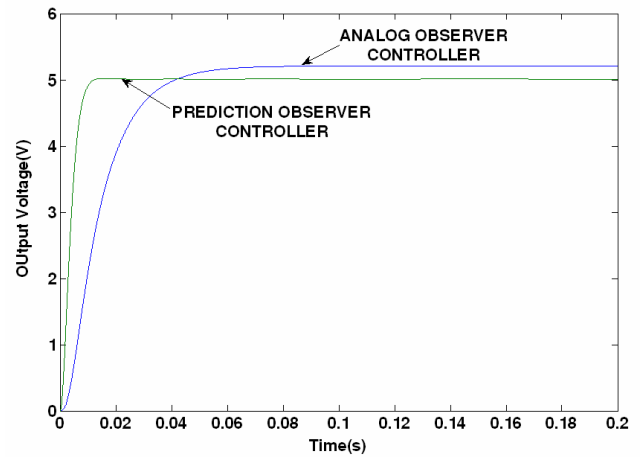


Fig. 12. Comparison between Digital and Analog Controller responses

0.04s. The corresponding output response of the Buck converter shows fixed output regulation. Undershoots and overshoots are not seen and the steady state error is also not apparent. The error signal which is the difference between the output voltage and the reference voltage is almost zero and hence the controller is very much emphatic in tracking exactly the reference voltage of 5V. The inductor current and the load current are also shown in Fig. 11, which shows no sign of current ripples. In order to check the dynamic performance of the system, the L and C values are varied and the output response of the system is shown in Table 3.

It is evident from Table 3 that the system is very much dynamic in tracking the reference voltages in spite of the variations in the inductance and capacitance values. The system does not show any overshoots or undershoots and it settles down fast with a settling time of about 0.014 seconds for all the values. The steady state error thus apparent is within the tolerable limits. In order to confirm the dominance of the digital controller over its analog counter parts, the output response of the dc-dc converter is compared against the response produced by the analog Observer controller and its graph is shown in Fig.12. It is noticeable that the digital controller demonstrates much better performance than the analog controller.

9. Hardware Implementation

9.1 LabVIEW package

The Buck converter with prediction observer controller has been implemented using LabVIEW as a controller platform. LabVIEW (Laboratory Virtual Instrumentation Engineering Work Bench) is a system design platform and development environment for a visual programming language from National Instruments. It is a widely used software to implement the projects with a shorter duration due to its programming flexibility combined with built in tools designed especially for testing, measurements and control. The key feature of LabVIEW is that it extensively supports accessing the instrumentation hardware. It is provided with drivers and abstraction layers for almost all types of instruments. The buses are also available for inclusion. The abstraction layers and drivers act as graphical nodes and enable to communicate effectively with the hardware devices thereby offering standard software interfaces [8].

The LabVIEW software is used to develop virtual instrumentation which comprises of the front panel and a functional block diagram. The front panel shown in Fig. 13 is mainly used for user interactions. It is through the front

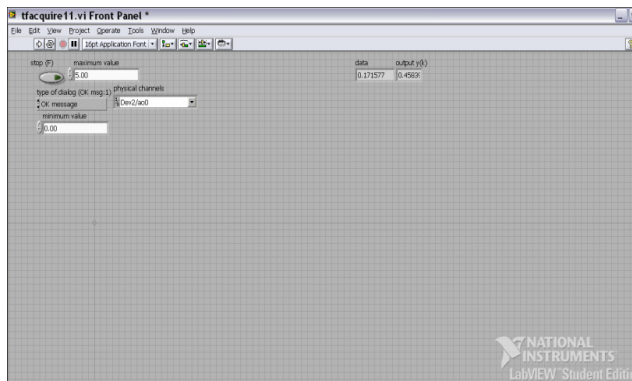


Fig. 13. Front Panel

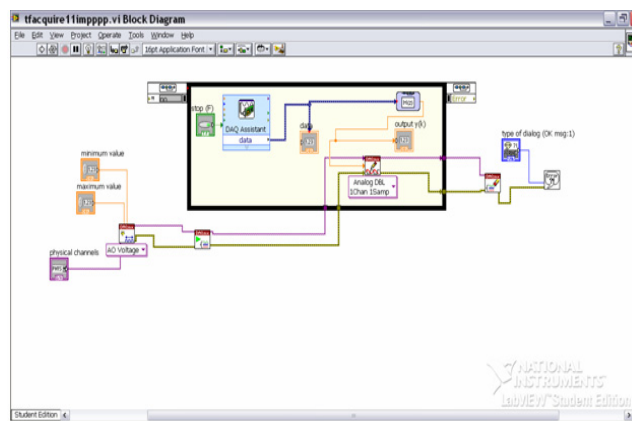


Fig. 14. Block Diagram

panel the desired transfer function of the observer controller is entered and the corresponding parameters of the controlled process and hence the updated status of the system is obtained. The block diagram, data acquisition, transfer function and signal generation are built using the functional block diagram as shown in Fig. 14. The analog signal from the external circuit is acquired by the DAQ Assistant block and it gets converted into the digital signal before being fed into to the discrete prediction observer controller block. As per the Nyquist criterion which states that the sampling frequency of the analog signal should be atleast twice the maximum signal frequency, the sampling frequency is set as 40 kHz. Since this type of DAQ card supports a maximum sampling rate of about 48 k samples/sec, such low frequency is assumed.

9.2 Interfacing circuit

The NI DAQ Pad-6009 multifunction data acquisition (DAQ) devices provide plug and play connectivity via USB for acquiring, generating and data logging in a variety of portable applications. It comprises of 8 analog inputs with referenced single ended signal coupling or 4 inputs with differential coupling, 2 analog outputs, 12 bits A/D and D/A converters and 32 bits counters. There are 12 channels of digital Input/output lines which can be used either as input or output. It eventually provides an excellent platform for the proposed observer controller. The prototype model of the Buck converter with prediction observer controller is shown in Fig. 15. It is obviously understood that the Observer controller works well and the LabVIEW provides the most feasible solution for the controller platform. To evaluate the performance, the reference values of 5V and 7V are set for which the output is obtained as 5.02V and 7.19V respectively. The output obtained with 5V reference value is illustrated in Fig. 16. The steady state error thus observed is very minimum of the order of 0.02V and the system settles down fast. The acquisition of the error signal from the hardware takes place instantaneous as and when the program is run and at the same time the controlled signal from the LabVIEW package is also generated within a very shorter duration of time without any delay or time lag. The experimental results thus obtained are in concurrence with the simulation results and mathematical calculations. Prototype model is developed using the values shown in Table 4.

Table 4. Experimental Values

Description	Experimental values
L	15mH
C	1 μ F
R	20 Ω
V _s	10V
f _s	20kHz
D	1N4007
M	IRF840

The input voltage has been varied as 10V, 12V and 14V and the corresponding output voltage is measured as 5.02V, 5.03V and 5.01V for the reference of 5V and it is illustrated in the Figs. 17, 18 and 19 respectively. In these figures orange coloured lines indicate the input voltages such as 10V, 12V and 14V respectively and the green coloured lines represent the corresponding output voltages. It can be observed that there are no undershoots or overshoots and steady state error is of very minimum order. Similarly the output voltage for the references of 5V and 7V are shown along with their switching pulses in the Fig. 20 and 21. It can be very well understood that the output thus observed shows better performance thereby proving that the controller is efficient enough to track the references inspite of the input voltage changes.

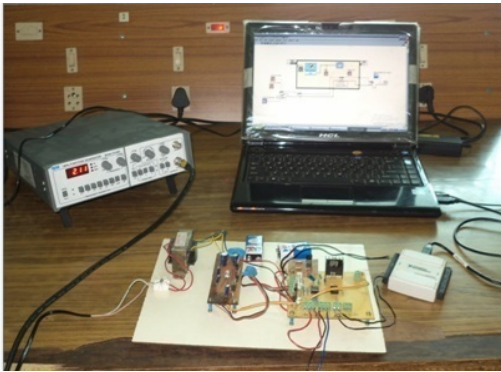


Fig. 15. Experimental set up

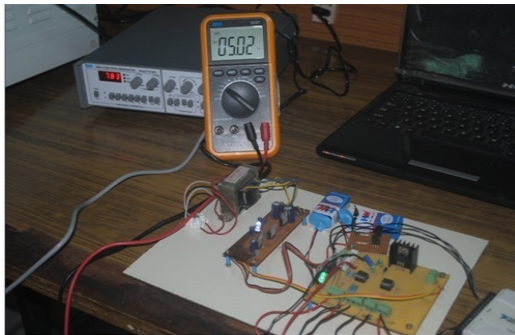


Fig. 16. Output Obtained for the reference of 5V

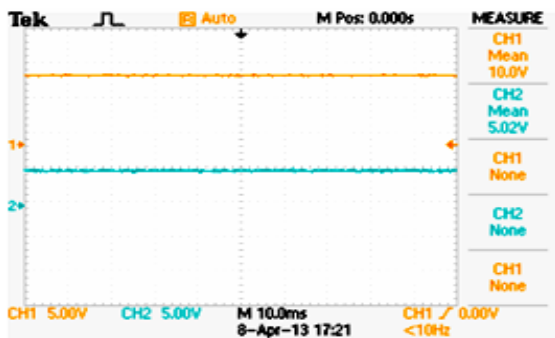


Fig. 17. Output Voltage Obtained for 10V input

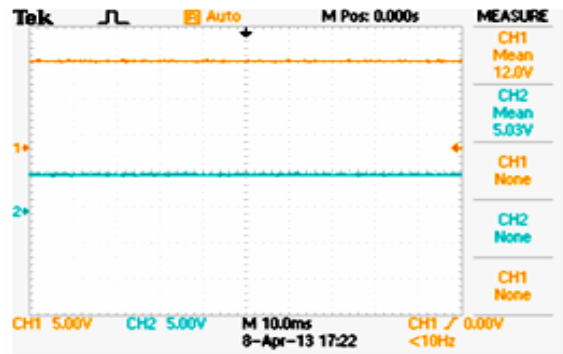


Fig. 18. Output Voltage Obtained for 12V input

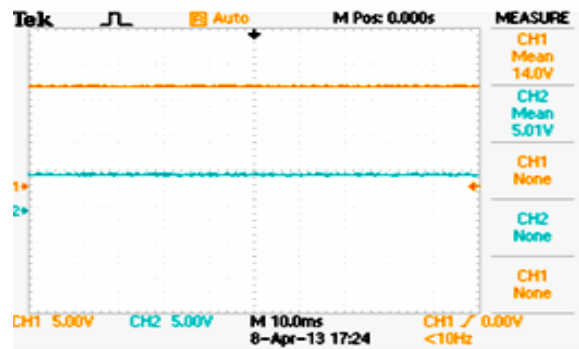


Fig. 19. Output Voltage Obtained for 14V input

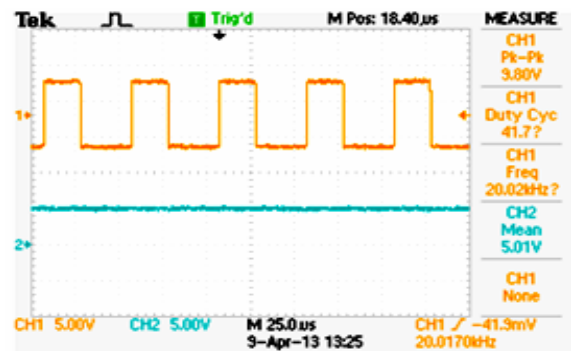


Fig. 20. Duty Cycle and Output voltage Obtained for 5V reference

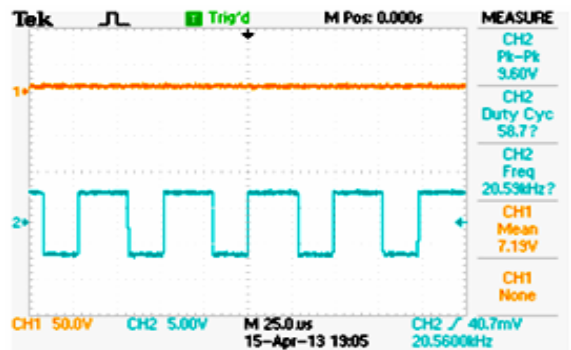


Fig. 21. Duty Cycle and Output voltage Obtained for 7V reference

10. Conclusion

A digital state feedback control approach has been designed for the Buck converter in discrete time domain using pole placement technique and separation principle. The load estimator has been designed by deriving full order state prediction observer to ensure robust control for the converter. The separation principle allows designing a dynamic compensator which very much looks like a classical compensator since the design is carried out using simple root locus technique. The prediction observer controller thus designed for the Buck converter is implemented using LabVIEW as a control platform and the results are illustrated. The mathematical analysis, simulation study and the experimental study show that the controller thus designed achieves tight output voltage regulation, good dynamic performances and higher efficiency. This method is topology independent and also can be extended for any of the applications such as power factor preregulation, photovoltaic cell and speed control applications.

Appendix

State equations of the discrete time system under consideration are same as that shown in the Eqs. (15) and (16) respectively. The derivation of the transfer function of the prediction observer controller is discussed now.

Root locus of the Buck converter is drawn and the desired poles are chosen arbitrarily by pole placement technique. Now the corresponding desired poles are chosen as 0.85 and 0.75. The desired characteristic polynomial is defined as,

$$(z - 0.85)(z - 0.75) = 0 \quad (1a)$$

Again this equation can be written as,

$$z^2 - 1.6z + 0.6375 = 0 \quad (2a)$$

The dynamic polynomial equation of the system with control law is defined as,

$$|ZI - G + HK| = \left[\begin{array}{c|c} z & 0 \\ \hline 0 & z \end{array} - \left[\begin{array}{cc} 0.9999 & -0.001383 \\ 0.1148 & 0.9919 \end{array} \right] + \left[\begin{array}{c} 0.0003471 \\ 1.995 \times 10^{-5} \end{array} \right] \left[\begin{array}{cc} k_1 & k_2 \end{array} \right] \right| \quad (3a)$$

The above equation is simplified as,

$$z^2 + (3.471 \times 10^{-4} k_1 + 1.995 \times 10^{-5} k_2 - 1.9917)z + (-3.442815 \times 10^{-4} k_1 + 3.98469 k_2 + 0.98351) = 0 \quad (4a)$$

Comparing Eqs. (2a) and (4a), k_1 and k_2 values are obtained as 1.0179×10^3 and 861.6 respectively.

Further to derive the Observer gain matrix the following assumptions are made.

The natural frequency of oscillation,

$$\omega_n = 424.2641 \times 10^3 \text{ rad/sec} \quad (5a)$$

The damping ratio (ζ) and the sampling time (T_s) are assumed as, 0.5 and $1 \mu\text{s}$ respectively.

Thus the desired characteristic equation for finding out the digital observer matrix is defined as,

$$z = e^{-\zeta \omega_n T_s} e^{\pm j \omega_n T_s \sqrt{1 - \zeta^2}} \quad (6a)$$

$$z = e^{-(0.5 \times 424.2641 \times 10^3 \times 1 \times 10^{-6})} e^{(\pm j 424.2641 \times 10^3 \times 1 \times 10^{-6} \sqrt{1 - 0.5^2})}$$

The above equation is simplified as follows,

$$z^2 - 1.5097z + 0.65425 = 0 \quad (7a)$$

The system dynamics with the unknown values of prediction observer gain matrix is given by,

$$|ZI - G + mC_d| = 0 \quad (8a)$$

Substitution of all the values in the above equation yields the following,

$$\left[\begin{array}{c|c} z & 0 \\ \hline 0 & z \end{array} - \left[\begin{array}{cc} 0.9999 & -0.001383 \\ 0.1148 & 0.9919 \end{array} \right] + \left[\begin{array}{c} m_1 \\ m_2 \end{array} \right] \left[\begin{array}{cc} 0 & 1 \end{array} \right] \right| = 0 \quad (9a)$$

Further simplification of the above equation gives the following,

$$z^2 + (m_2 - 1.9918)z + (0.1148m_1 - 0.9999m_2 + 0.991959) = 0 \quad (10a)$$

On comparison of the Eqs. (7a) and (10a) the observer gain matrices are obtained as $m_1 = 0.42135$ and $m_2 = 0.27032$.

Discrete Compensator is designed using separation principle using the following formula,

$$\frac{-U(z)}{Y(z)} = D(z) = k [ZI - G + HK + mC_d]^{-1} m \quad (11a)$$

On substitution of the required values in the above equation the transfer function of the prediction observer controller is obtained as,

$$\frac{-U(z)}{Y(z)} = \frac{1772z - 1637}{z^2 - 1.118z + 0.4533} \quad (12a)$$

References

- [1] Subhash Chander, Pramod Agarwal and Indra Gupta, "Auto-tuned, Discrete PID Controller or DC-DC Converter for fast transient response", in *proceedings of International Conference on Power Electronics*, pp. 1-7, March 2011.
- [2] Frank H.F. Leung, Peter K.S. Tam, C.K.Li, "The Control of Switching dc-dc Converters-A General LQR Problem", *IEEE Transactions on Industrial Electronics*, Vol. 38, No. 1, pp. 65-71, Feb. 1991.
- [3] Zdravko Lukic et. al., "Self – Tuning Digital Current Estimator for Low-Power Switching Converters", in *Proceedings of Applied Power Electronics Conference and Exposition*, pp. 529-534, Feb. 2008.
- [4] Shuibao Guo et. al., "Digital PWM Controller for High-Frequency Low-Power DC-DC Switching Mode Power Supply", in *Proceedings of Power Electronics and Motion control Conference*, pp. 1340-1346, May 2009.
- [5] Tobias Geyer et. al., "Constrained Optimal Control of the Step-Down DC-DC Converter", *IEEE Transactions on Power Electronics*, Vol. 23, No. 5, pp. 2454-2464, Sep. 2008.
- [6] Sebastien Mariethoz et.al., "Comparison of Hybrid Control Techniques for Buck and Boost DC-DC Converters", *IEEE Transactions on Control systems Technology*, Vol. 18, No. 5, pp. 1126-1145, Sep. 2010.
- [7] Jong-Won Shin et.al., "Digital Average Current Mode Control of Boost Converter using Diode Current Sensing Technique", in *Proceedings of Power Electronics Annual Conference, KIPE*, pp. 305-307, Feb. 2009.
- [8] Chien-Ming Lee et.al. , "LabVIEW Implementation of an Auto-Tuning PID Regulator via Grey-predictor", *IEEE Conference on Cybernetics and Intelligent Systems*, pp.1-5, June 2006
- [9] Jonathan W, Kimball, Philip T. Krein, "A Current-Sensorless Digital Controller for Active Power Factor Correction Control Based on Kalman Filters", in *Proceedings of Applied Power Electronics Conference and Exposition*, pp.1328-1333, 2008.
- [10] Jeffrey Morroni, Regan Zane and Dragan Maksimovic, "Design and Implementation of an adaptive Tuning System Based on Desired Phase Margin for Digitally Controlled DC-DC Converters", *IEEE Transactions of Power Electronics*, Vol. 24, No. 2, pp. 559-564, Feb. 2009.
- [11] N.Gonzalez – Fonseca, J. de Leon – Morales, J. Leyva – Ramos, "Observer- Based Controller for Switch Mode DC-DC Converters", in *Proceedings of the 44th IEEE Conference on Decision and Control, and European Control Conference* , pp. 4773-4777, Dec. 2005.
- [12] Hyun-Su Bae, Jeong – Hwan Yang, Jae-Ho Lee, Bo-Hyung Cho," Digital State Feedback Current Control using the Pole Placement Technique", *Journal of Power Electronics*, Vol. 7, pp. 213-221, July 2007.



dc-dc converters.

R. Shenbagalakshmi She received B.E degree in Electrical and Electronics Engineering from Bharathidasan University, Tiruchirapalli in 2001 and Master degree in Power Electronics and Drives from Vinayaga Mission's University, Salem in 2007. Her research interests are robust control of



Dr. T. Sree Renga Raja He is working as an Assistant Professor in the Department of Electrical and Electronics Engineering, Anna University, BIT Campus, Tiruchirapalli, Tamil Nadu, India. He obtained B.E (Electrical and Electronics Engineering) degree from Manonmaniam Sundaranar University, Tirunelveli in 1998, M. E (Power Systems) from Annamalai University, Chidambaram in 1999 and Ph.D from Anna University, Chennai in 2007. He has published many papers in the field of Power System Engineering. His area of interest includes Power system optimization, Renewable Energy Applications, Energy Conservation Management and Insulation Engineering.