J Electr Eng Technol Vol. 8, No. 6: 1481-1486, 2013
http://dx.doi.org/10.5370/JEET.2013.8.6.1481

ISSN(Print) 1975-0102
ISSN(Online) 2093-7423

Analytical Modeling and Simulation of Dual Material Gate Tunnel Field Effect Transistors

T.S.Arun Samuel†, N.B.Balamurugan*, S.Sibitha*, R.Saranya* and D.Vanisri*

Abstract - In this paper, a new two dimensional (2D) analytical model of a Dual Material Gate tunnel field effect transistor (DMG TFET) is presented. The parabolic approximation technique is used to solve the 2-D Poisson equation with suitable boundary conditions. The simple and accurate analytical expressions for surface potential and electric field are derived. The electric field distribution can be used to calculate the tunneling generation rate and numerically extract tunneling current. The results show a significant improvement of on-current and reduction in short channel effects. Effectiveness of the proposed method has been confirmed by comparing the analytical results with the TCAD simulation results.

Keywords: Tunnel field effect transistor (TFET), Band to band Tunneling, Analytical model, Poisson equation, Parabolic approximation, Surface potential

1. Introduction

The primary challenges faced in scaling a complementary metal oxide semiconductor (CMOS) device are to ensure the increased functionality per unit cost and improvement in the performance of device. Several technologies are proposed to keep up the scaling law proposed by Gordon Moore. In order to fulfill the scaling law, various device structures are required for maintaining the device characteristics accurately. These device structures include double gate (DG) MOSFETs, dual material gate (DMG) MOSFETs, surrounding gate (SG) MOSFETs, and dual material surrounding gate (DMSG) MOSFETs device. The key factors that limit the performance of MOS devices are increased short channel effects (SCE) and very high leakage current. In recent years, a number of non-classical MOS device structures have been proposed to overcome the SCEs of CMOS technology in the nanoscale region. But in these non classical devices, the supply voltage cannot be reduced further because of the Subthreshold Swing (SS) being limited to 60 mV/decade [1, 2] at the room temperature.

Tunnel field-effect transistor has been considered as a best alternative device in the standard CMOS for low-power applications. Due to the built-in tunnel barrier, the TFET device does not suffer from short channel effects, when compared to the conventional planar MOSFET device.

TFET has several superior properties such as, the subthreshold swing is smaller than 60 mV/decade at room temperature [3], which is the physical limit of the MOSFET. In addition, tunnel field effect transistors (TFETs) show a very small leakage current, in the range of femto amperes (fA) [4] when the device is turned off. Also TFET offers much smaller Vt roll-off while scaling because threshold voltage depends on the band bending in small tunnel region, but not the whole channel region. Apart from all these merits, TFETs suffer from a low ON-current (I_{ON}). Therefore various techniques to improve the I_{ON} in the TFET have been suggested [5], [6]. In order to enhance the ON current (I_{ON}), various design improvements in terms of band gap engineering [6], hetero junction TFETs [7] strained silicon [8], novel architectures like carbon nanotube TFETs [9], DG TFET [10] and DMG DGTFETs [11] have been proposed. The above models deal only with simulation and only a few analytical models were proposed. [12-14]. The analytical model provides better understanding of the physical design of the TFETs. Lee [12] proposed a model for potential and electric field for Single Material Gate (SMG) TFET using superposition method. Despite accuracy of this model, it involves a lot of mathematical complexity and makes its understanding difficult. Bardon [14] proposed potential and electric field model for DG TFET using pseudo 2-D solution. 1-D poisson's equation based modeling of TFET was devised by Verhulst [15]. In this paper, we have proposed a new novel DMG TFET structure which enhances the I_{ON} current during device operation

The aim of this work is, to study the potential benefits offered by the DMG TFET by using parabolic approximation technique for the first time, which is simple and accurate. The analytical model is developed using two dimensional solution of Poisson equation. This model is used to calculate the surface potential and electric field

† Corresponding Author: Dept. of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India. (arunsamuel@tce.edu)
* Dept. of Electronics and Communication Engineering, Thiagarajar College of Engineering, Madurai, India. (nbbalamurugan@tce.edu, {emailtosibi, rsaranya154, svanisri17}@ gmail.com)
Received: April 27, 2013; Accepted: June 5, 2013

distribution in the device under the two metal gates and the drain current I_{DS} is derived from the electric field using Kane's model. This paper is ordered as follows: Section 2 shows model derivation of this work. The result and discussions are analyzed in Section 3 and Section 4 contains a summary of the conclusions.

2. Model Derivation

The cross section view of a Dual Material Gate TFET is shown in Fig. 1. The source and drain is made of highly doped p-type and n-type regions respectively. The intermediate channel region is made of a moderately doped n-type layer. Silicon-di-oxide (SiO_2) is used as the gate dielectric. The gate consists of two materials M_1 and M_2 with gate lengths L_1 and L_2 with two different work function ϕ_{m1} and ϕ_{m2}. Based on the positive or negative potential applied to the gate terminal, the device behaves as n type TFET and p type TFET respectively. If a positive gate voltage is applied, the transistor behaves as a n-TFET and a negative gate voltage is applied, the transistor behaves as a p-TFET. The device physical parameters are summarized in Table 1. Increasing the positive voltage on the gate narrows the energy barrier between the source and intrinsic region. Then electrons tunnel from the valence band of the p-doped source to the conduction band in the intrinsic body and then move toward the n-doped drain by drift diffusion. The bottom of the buried oxide (BOX) layer is grounded. The thickness of the BOX layer (t_{BOX}) is very small, hence the voltage drop across BOX region is negligible.

2.1 Surface potential

The potential distribution in the gate oxide region is distinguished by two dimensional Poisson's equation [12],

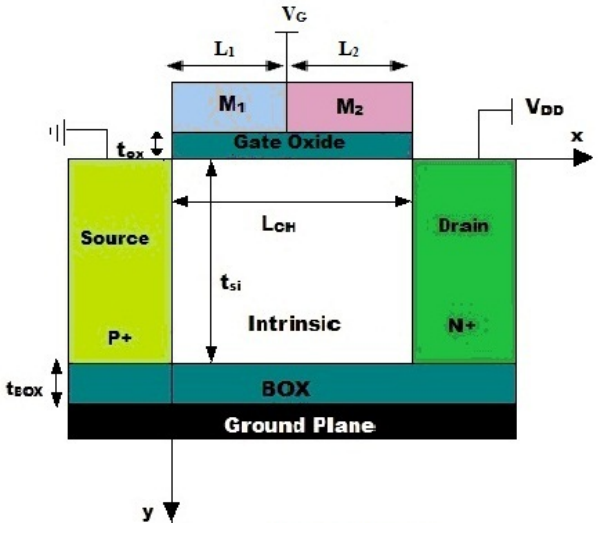


Fig. 1. Schematic diagram of a DMG TFET

$$\frac{\partial^2\phi(x,y)}{\partial x^2}+\frac{\partial^2\phi(x,y)}{\partial y^2}=0 \tag{1}$$

The potential profile in the vertical direction is assumed to be a second-order polynomial, i.e.,

$$\phi(x,y)=c_0(x)+c_1(x)y+c_2(x)y^2 \tag{2}$$

The boundary conditions in the channel region are:

(a) Electric flux at the front-oxide gate interface is continuous for DMG TFET, therefore

$$\frac{d\phi_1(x,y)}{dy}=\frac{\in_{ox}}{\in_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}} \quad \text{Under } M_1 \text{ at y=0} \tag{3}$$

$$\frac{d\phi_2(x,y)}{dx}=\frac{\in_{ox}}{\in_{si}}\frac{\phi_{s_2}(x)-\psi_{g_2}}{t_{ox}} \quad \text{Under } M_2 \text{ at y=0} \tag{4}$$

(b) Electric flux at the back gate-oxide and the back channel interface is continuous for both the material

$$\frac{d\phi_1(x,y)}{dx}=0 \quad \text{Under } M_1 \text{ at y=}t_{si} \tag{5}$$

$$\frac{d\phi_2(x,y)}{dx}=0 \quad \text{Under } M_2 \text{ at y=}t_{si} \tag{6}$$

(c) The potential at the source and drain end is

$$\phi_1(x,y)=\phi_{s_1}(0)=V_{bi}$$
$$\phi_2(L_1+L_2,0)=\phi_{s_2}(L_1+L_2)=V_{bi}+V_{DS} \tag{7}$$

Where V_{bi} is the built in potential, E_g is Band gap energy, q is elementary charge, V_{GS} is Gate to Source voltage, V_{DS} is Drain to Source voltage, ε_{si} is relative permittivity of silicon and ε_{ox} is relative permittivity of silicon dioxide.

Since we have two materials in the gate, the potential under Material1 (M_1) and Material2 (M_2) can be written as

$$\phi_1(x,y)=\phi_{s1}(x)+C_{11}(x)y+C_{12}(x)y^2 \tag{8}$$
$$0 \le x \le L_1$$

$$\phi_2(x,y)=\phi_{s2}(x)+C_{21}(x)y+C_{22}(x)y^2 \tag{9}$$
$$L_1 \le x \le L_1+L_2$$

The values of $C_{11}(x)$, $C_{12}(x)$, $C_{21}(x)$, and $C_{22}(x)$ are arbitrary constants which is obtained from the boundary conditions (3-5) and (6).

$$C_{11}(x)=\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}} \tag{10}$$

$$C_{12}(x)=-\frac{1}{2t_{si}}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\frac{\phi_{s_1}(x)-\psi_{g_1}}{t_{ox}} \tag{11}$$

$$C_{21}(x) = \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s_2}(x) - \psi_{g_2}}{t_{ox}} \tag{12}$$

$$C_{22}(x) = -\frac{1}{2t_{si}} \frac{\varepsilon_{ox}}{\varepsilon_{si}} \frac{\phi_{s2}(x) - \psi_{g_2}}{t_{ox}} \tag{13}$$

potential $\phi_{s_1}(x)$ and $\phi_{s_2}(x)$ under M_1 and M_2 can be obtained by solving the Poisson's equation (1) using boundary conditions (7), (8) and (9), therefore,

$$\phi_{s1}(x) = Ae^{\lambda x} + Be^{-\lambda x} - \psi_{g_1} \tag{14}$$

$$\phi_{s2}(x) = Ce^{\lambda x} + De^{-\lambda x} - \psi_{g_2} \tag{15}$$

Where $\lambda = \sqrt{\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox} t_{si}}}$

$$\psi_{g1} = V_{gs} - \phi_{m1} + \chi + E_g/2$$

$$\psi_{g2} = V_{gs} - \phi_{m2} + \chi + E_g/2$$

Where the gate work function of metal1 (ϕ_{m1}) is 4eV and metal2 (ϕ_{m2}) is 4.6eV. χ is the electron affinity. The coefficients of A, B, C and D can be expressed as

$$A = \frac{[(V_{bi} - \psi_{g1})e^{(\lambda(L_1 - L_2)}] - [V_{bi} + V_{DS} - \psi_{g2}] + [(\psi_{g_1} - \psi_{g2})\cosh(\lambda L_2)]}{e^{\lambda(L_1 - L_2)} - e^{\lambda(L_1 + L_2)}}$$

$$B = \frac{[V_{bi1} + V_{ds} - \psi_{g2}] - [(V_{bi} - \psi_{g1})e^{\lambda(L_1 + L_2)}] - [(\psi_{g1} - \psi_{g2})\cosh(\lambda L_2)]}{e^{\lambda(L_1 - L_2)} - e^{\lambda(L_1 + L_2)}}$$

$$C = Ae^{(\lambda L_1)} + \frac{\psi_{g_1} - \psi_{g_2}}{2} \tag{16}$$

$$D = Be^{-(\lambda L_1)} + \frac{\psi_{g_1} - \psi_{g_2}}{2}$$

2.2 Electric field

The electric-field distribution along the channel length can be obtained by differentiating the surface potential. The lateral electric field can be written as,

$$E_1(x) = -\frac{d\phi_{s1}(x)}{dx} = -(A\lambda e^{\lambda x} - B\lambda e^{-\lambda x}) \tag{17}$$

$$0 \le x \le L_1$$

$$E_2(x) = -\frac{d\phi_{s2}(x)}{dx} = -(C\lambda e^{\lambda x} - D\lambda e^{-\lambda x}) \tag{18}$$

$$L_1 \le x \le L_1 + L_2$$

The vertical electric field can be written as

$$E_{y1}(x) = \frac{d\phi_{s1}(x,y)}{dy} = -C_{11}(x) - 2yC_{12}(x) \tag{19}$$

$$0 \le x \le L_1$$

$$E_{y2}(x) = \frac{d\phi_{s2}(x,y)}{dy} = -C_{21}(x) - 2yC_{22}(x) \tag{20}$$

$$L_1 \le x \le L_1 + L_2$$

2.3 Drain current

The mechanism of flow of current I_{DS} in DMG TFET is based on Band-to-Band Tunneling (BTBT) of electrons from the valance band of the source to the conduction band of the channel region. The tunneling generation rate (G) can be calculated using Kane's model. The total drain current is computed by integrating the band to band generation rate over the volume of the device. Therefore,

$$I_{DS} = q\iint G dx dy \tag{21}$$

For the calculation of tunneling Generation rate (G), Kane's Model has been employed [14, 16, 17].

$$G(E) = A\frac{|E|^2}{\sqrt{E_g}} e^{\left[-B\frac{E_g^{3/2}}{|E|}\right]} \tag{22}$$

Where, $|E|$ is the magnitude of the electric field which is defined as $|E| = \sqrt{E_x^{\,2} + E_y^{\,2}}$ and E_g is the energy band gap. The parameters used for TCAD simulation are $A = 8.1 \times 10^{17} eV^{1/2}/cm.s.V^2$ and $B = 3.057 \times 10^7 V/cm\text{-}(eV)^{3/2}$.

3. Result and Discussion

In order to verify the analytical model, two-dimensional device simulation has been performed by using TCAD Sentaurus. In the simulator Band-to-Band Tunneling is an important parameter considered for analyzing the working of Tunnel FETs. The models available in TCAD to simulate band-to-band tunneling are Kane's Band-to-Band model, Hurkx's Band-to-Band model, Schenk's Band-to-Band model and the dynamic Non Local Band-to-Band model. In our work the Kane's model is used to evaluate the band-to-band generation rate. It is also compared with the superposition model proposed by M.J.Lee [12] for SMG TFET. At low values of V_{DS} (approximately 0 to 0.5 V), the gate bias induces an accumulation of electronics in the channel region. This leads to reduce the channel resistance. Hence the tunnel width is decreased which in turn increases the electric field across the tunneling junction, leading to a rapid increase in the drain current I_{DS}.

Fig. 2 shows the calculated surface potential profile for different gate voltage of the DMG TFET structure along with the simulated potential profile. As the gate voltage increases, the potential in the lightly doped region increases. There is a step-change of potential along the

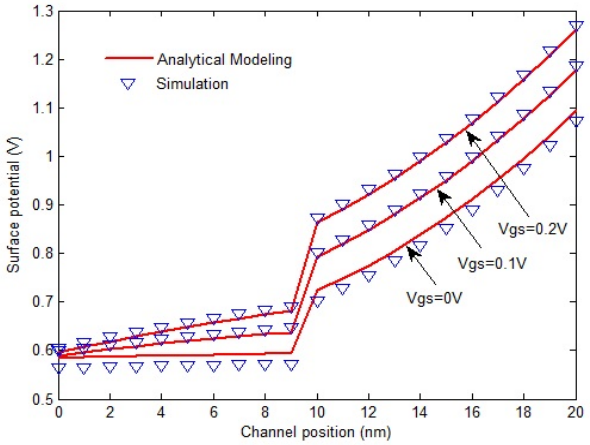


Fig. 2. Surface potential profiles of DMG-TFET for Channel length L=20nm and V_{DS}=0.1V with different gate biases.

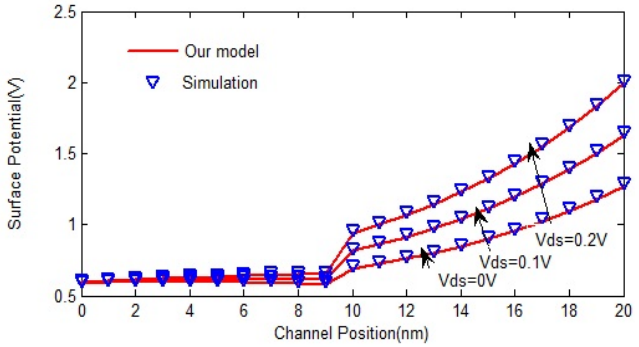


Fig. 3. Surface potential profiles of DMG-TFET for channel length L=20nm and V_{GS}=0.1V with different V_{DS}

channel at the interface of Metal1 and Metal2.It is clearly seen from the figure that due to the presence of gate bias, there is momentous change in the potential under the gate metal 1. As a result the gate bias has high influence on tunneling current at source side.

Fig. 3 shows the calculated surface potential profile for different drain voltage of the DMG TFET structure along with the simulated potential profile. As the drain voltage increases, the potential in the region under metal2 increases. But there is no significance change in potential under Metal1. Hence Metal1 is screened from the effect of drain voltage. Analytical results are in excellent agreement with simulation results.

Fig. 4 shows the calculated and simulated values of the surface potential at V_{GS}=0.3V and V_{DS}=0.1V along the channel length for the DMG TFET and it is also compared with Lee model. Fig. 5 shows the variation of vertical electric field distribution with the channel position for different values of gate voltage. It is evident from the figure that peak of the vertical electric field appears near the tunneling junction. ie., region under metal 1. Due to this effect the tunneling current gets increased. The electric

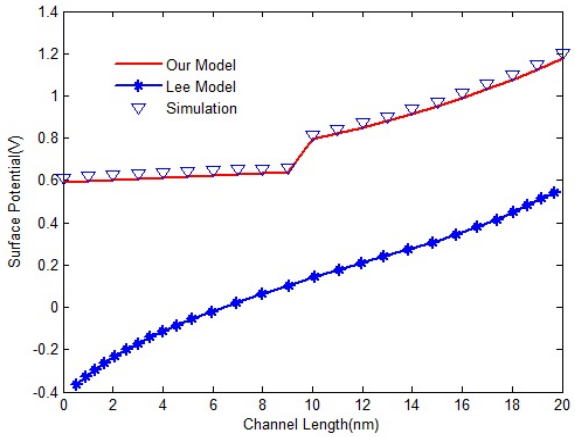


Fig. 4. Surface potential profiles of DMG-TFET and SMG TFET for Channel length L=20nm, V_{DS}=0.1V and V_{GS}=0.3V

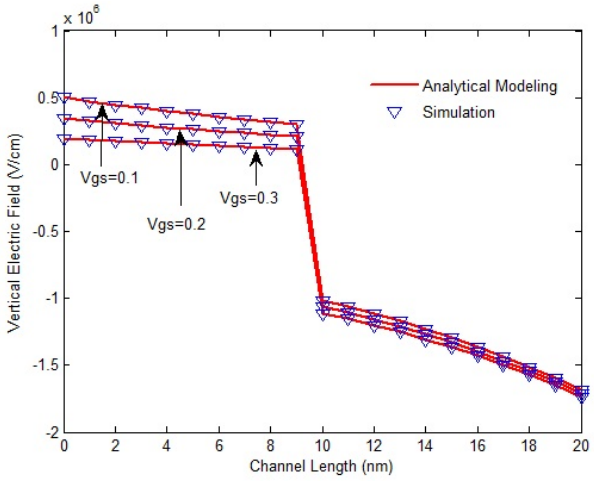


Fig. 5. Vertical electric field of DMG-TFET for Channel length L=20nm and V_{DS}=0.1V with different gate biases.

field near the drain decreases with the change in the work function. ie., region under metal 2. The simulation results proved the validity of the model proposed. Fig. 6 shows the modeled and simulated values of the lateral electric field distribution at V_{GS}=0.3V and V_{DS}=0.1V along the channel length for the DMG TFET and it is also compared with the model proposed by Lee for SMG TFET considering the same channel length. The lateral electric field is present on the device at any gate voltage. Analytical results are in excellent agreement with simulation results.

Fig. 7 shows the I_D-V_{GS} characteristics of DMG TFET with modeled and simulated values and it is compared with the model proposed by Lee. The positive values of V_{GS}, electrons tunnel from valence band in p+ source region to conduction band in channel region and the tunneling current gets increased. The device behaves as a N type DMG TFET. The negative values of V_{GS}, electrons tunnel from valence band in channel region to conduction band in

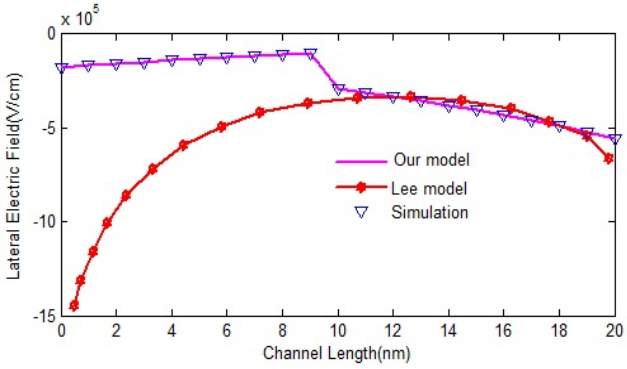


Fig. 6. Lateral electric field of DMG-TFET and SMG TFET for Channel length L=20nm, V_{DS}=0.1V and V_{GS}=0.3V

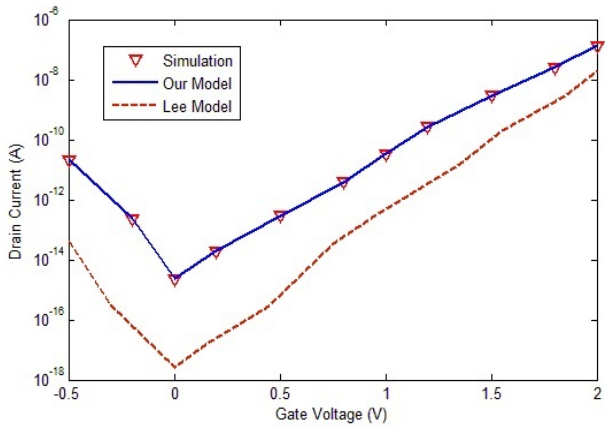


Fig.7. I_D-V_{GS} characteristics of DMG-TFET for channel length L=20nm and V_{DS}=0.1V

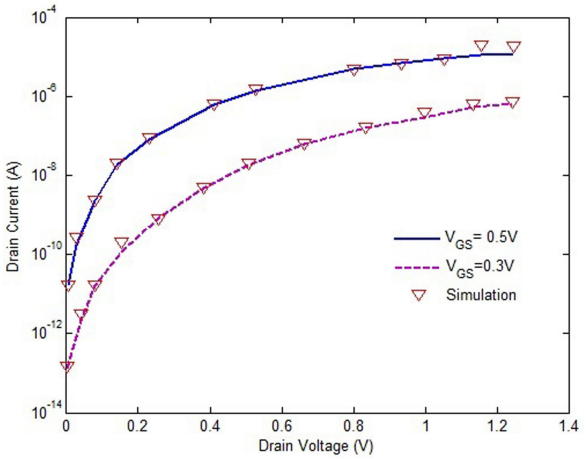


Fig.8. I_D-V_{DS} characteristics of DMG-TFET for channel length L=20nm with varies gate voltage V_{GS}.

n+ drain region and the tunneling current gets increased. The device is behaves as a P type DMG TFET. It is inferred from the figure that our model has higher drive current than SMG TFET. Fig. 8 shows the I_D-V_{DS} characteristics of DMG TFET with modeled and simulated values with gate voltages 0.3V and 0.5V respectively. Analytical results are in excellent agreement with simulation results.

4. Conclusion

In this work the DMG-TFET structure has been analyzed and their performance improvements over different parameters are discussed. The analytical model is based on two-dimensional Poisson's equation which is solved by using parabolic approximation. The analytical expressions of surface potential, lateral electric field and vertical electric field have been calculated. In this model, components of lateral electric field and vertical electric field can also be used to analytically calculate distribution of tunneling generation rate and numerically extract tunneling current. Based on the generation rate and electric fields, we obtained the I_{DS}-V_{GS} characteristics. From the presented results, it can be concluded that the DMG structure provides wide range of benefits to the TFET performance. The results clearly demonstrate the excellent immunity against SCE offered by the DMG structure while decreasing channel length.

Table 1. The values of parameters used in simulations

Gate Oxide Thickness	2nm
Silicon Body Thickness	10nm
P^+ Source Doping	$10^{20}/cm^3$
N^+ Drain Doping	$10^{20}/cm^3$
Channel Doping	$10^{17}/cm^3$
Channel Length (L_1+L_2)	10nm+10nm=20nm

References

[1] P. K.Tiwari and S. Jit, "A Subthreshold Swing Model for Symmetric Double Gate (DG) MOSFETs with Vertical Gaussian Doping", *Journal of Semiconductor Technology and Science*, Vol.10, No.2, pp.107-16, Jun. 2010.

[2] Z. Ding, G. Hu, J. Gu, R. Liu, and L.Wang "An analytical model for the subthreshold swing of double-gate MOSFETs," *International Workshop on IWJT*, 2010, pp.1-4.

[3] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, Vol. 27, No. 4, pp. 297-300, Apr. 2006.

[4] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, Vol.93, No.19, pp.196805, Nov. 2004.

[5] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-K gate dielectric," *IEEE Trans. Electron Devices*, Vol. 54, No. 7, pp. 1725-1733, Jul.

2007.

[6] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel band gap modulation and gate work function engineering," *IEEE Trans. Electron Devices*, Vol. 52, No. 5, pp. 909-917, May. 2005.

[7] L. Wang, E. Yu, Y. Taur and P. Asbeck, "Design of tunneling field effect transistors based on staggered hetero junctions for ultra low power applications," *IEEE Electron Device Lett*., Vol. 31, No. 5, pp. 431-433, May. 2010.

[8] O. M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt and D. A. Antoniadis, "Design of Tunneling Field-Effect Transisitors Using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunctions," *IEEE Electron Device Lett.,* Vol. 29, No. 9, pp- 1074-1077, Sep. 2008.

[9] J. Appenzeller, Y. M. Lin, J. Knoch, Z. H. Chen, and P. Avouris, "Comparing carbon nanotube transistors - The ideal choice: A novel tunneling device design," *IEEE Trans. Electron Devices*, Vol. 52, No. 12, pp. 2568-2576,Dec. 2005.

[10] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high- k gate dielectric," *IEEE Trans. Electron Devices*, Vol. 54, No. 7, pp. 1725-1733, Jul. 2007.

[11] S. Saurabh and M. Jagadesh Kumar, "Novel Attributes of a Dual Material Gate Nanoscale Tunnel Field-Effect Transistor," *IEEE Trans. on Electron Devices*, Vol. 58, No. 2, pp. 404-410, Feb. 2011.

[12] M.J.Lee and W.Y.Choi, "Analytical Model of a single-gate silicon-on-insulator (SOI) tunneling field-effect transistors (TFETs)," *Solid-State Elec.*, Vol. 63, pp.110-114, Sep. 2011.

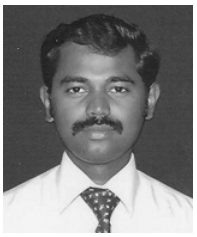
[13] C. Shen, S.-L. Ong, C.-H. Heng, G. Samudra, and Y.-C. Yeo. "A variational approach to the two-dimensional nonlinear Poisson's equation for the modeling of tunneling transistors," *IEEE Electron Device Lett.*, Vol. 29, No. 11, pp. 1252-1255, Oct. 2008.

[14] M.G. Bardon, H.P.Neves, R.Puers, and C.V.Hoof, "Pseudo-two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions", *IEEE Trans., Electron Devices*, Vol.57, No.4, pp. 827-34, Apr. 2010.

[15] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization," *J. Appl. Phys.*, Vol. 104, No. 6 pp. 064 514-1,Sep. 2008.

[16] E.O.Kane, "Zener tunneling in semiconductors," *J.Phys. Chem.Solides,* Vol. 12, No. 2, pp.181-188, Jan. 1960.

[17] E.O. Kane, "Theory of tunneling," *J. Appl. Phys.,* Vol. 32, No. 1, pp. 83-91, Jan.1961.



T.S.Arun Samuel He received B.E degree in Electronics and Communication engineering from Madurai Kamaraj University and M.E degree from Anna University, India. His research interests includes multi gate TFETs.

N. B. Balamurugan He received B.E and M.E degree in Electronics and Communication engineering from Madurai Kamaraj University and Ph.D degree from Anna University, India. His research interests includes multi gate TFETs and Nanowire transistors

S.Sibitha She received B.E degree in Electronics and Communication engineering from Anna University, India. Her research interests includes multi gate TFETs.

R.Saranya She received B.E degree in Electronics and Communication engineering from Anna University, India. Her research interests includes multi gate TFETs.

D.Vanisri She received B.E degree in Electronics and Communication engineering from Anna University, India. Her research interests includes multi gate TFETs.