Fabrication of Superjunction Trench Gate Power MOSFETs Using BSG-Doped Deep Trench of p-Pillar

Sang Gi Kim, Hoon Soo Park, Kyoung Il Na, Seong Wook Yoo, Jongil Won, Jin Gun Koo, Sang Hoon Chai, Hyung-Moo Park, Yil Suk Yang, and Jin Ho Lee

In this paper, we propose a superjunction trench gate MOSFET (SJ TGMOSFET) fabricated through a simple p-pillar forming process using deep trench and boron silicate glass doping process technology to reduce the process complexity. Throughout the various boron doping experiments, as well as the process simulations, we optimize the process conditions related with the p-pillar depth, lateral boron doping concentration, and diffusion temperature. Compared with a conventional TGMOSFET, the potential of the SJ TGMOSFET is more uniformly distributed and widely spread in the bulk region of the n-drift layer due to the trenched p-pillar. The measured breakdown voltage of the SJ TGMOSFET is at least 28% more than that of a conventional device.

Keywords: Superjunction MOSFET, trench p-pillar formation, trench gate.

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I. Introduction

A power MOSFET is an essential component in switching mode power supply circuits and inverter systems. The power MOSFETs used in power converters operate as switching devices, and their associated dissipation loss consists of conduction loss while the power MOSFET is in an on state and switching loss when it turns on and off. To reduce the dissipation loss of a power MOSFET, a minimization of the on-resistance per unit area (R_{ON}•A) and gate-to-drain charge is normalized to the on-resistance (R_{ON}•Q_{GD}) [1], [2]. However, for a conventional power MOSFET, there is a fundamental tradeoff between the breakdown voltage and specific R_{ON}, and it is not thought to be possible to obtain an R_{ON}•A value that exceeds the silicon limit. A superjunction (SJ) structure is an innovative breakthrough that overcomes this limitation and is a fitting way to achieve both a low R_{ON} and high breakdown voltage of above 400 V [3]-[5]. An SJ requires the formation of multiple p-pillars and n-pillars in the drift region, and its concept is based on the charge compensation principle. The excess charge in an n-pillar is counter balanced by the adjacent charges in the p-pillar, and a uniform field distribution can thus be achieved [6]. These alternating p- and n-pillars make it possible to achieve a charge balance. SJ trench gate MOSFETs (SJ TGMOSFETs) are typically manufactured by creating multiple columns of p-pillars within a low-impurity n-type epitaxial layer, which is grown on a heavily doped n+ substrate. A multistep epitaxial growth process builds up the columns layer by layer, thereby increasing the total implanted layer thickness until the required voltage tolerance is obtained. Therefore, the low throughput of the epitaxial growth and the complicated production steps of this process make it difficult to

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enhance the productivity or cut the cost [7]-[9].

In this paper, we propose a simple p-pillar formation process to overcome the process complexity inherent to a multilevel epitaxial growth approach that creates a p-pillar region through multiple high-energy ion implantations. The p-pillar region is built from the lateral boron diffusion from the boron silicate glass (BSG) film and annealing after the deep etching process of the silicon. Considering the required breakdown voltage, process optimization, such as regarding p-pillar depth and BSG doping concentration, is conducted using a two-dimensional SILVACO process and device simulations.

II. Experiments

SJ TGMOSFETs with a BSG doping process technology are fabricated on an n-type epitaxial layer grown on a heavily doped n+ (100) substrate. The resistivity of the epitaxial layer is 0.6 Ω•cm to 1.0 Ω•cm, and its thickness is 10 μm. First, a p-body region is formed with a boron ion implantation. The trench gate etching process is done after local dry oxidation of silicon and n+ source formation in the p-body layer. The post trench etching treatment carried by the SC1 cleaning and high-temperature sacrificial oxidation is done to reduce the roughness of the trench sidewall and eliminate the damaged layer of the trench surface. The resulting width of the trench gate is 0.8 μm, and its depth is 1.6 μm. To improve the gate oxide integrity, we use a stacked gate oxide that combines the thermal and chemical vapor deposition oxides. The polysilicon gate electrode is formed through polysilicon deposition and doping processes. To overcome the disadvantages inherent to the multilevel epitaxial growth method, we create an SJ structure with the deep trench etching and lateral boron doping techniques. A high aspect ratio trench is built through reactive ion etching, while the deposited TEOS oxide is used for the deep trench etching mask layer. After the formation of a deep trench under a p+ source region, a boron-doped BSG film 1,000 Å thick is deposited under a processing temperature of 730°C. The removal of the BSG film and a thermal annealing are then conducted to form a p-pillar. Finally, deep trench filling and metallization processes are carried out. Figure 1 shows the cross-sectional structure of the SJ TGMOSFET. Owing to the use of a high aspect ratio trench and lateral boron doping techniques for this device, the processing steps can be simplified, and the manufacturing throughput can be boosted and the cost reduced. Detailed scanning electron microscopy (SEM) images after boron lateral diffusion and oxide filling inside the deep trench region are shown in Fig. 2. Figure 2(a) illustrates the conventional TGMOSFET fabricated using the high density trench etching process described in our previous study [10], whereas Fig. 2(b) shows an SJ TGMOSFET fabricated with a deep trench and BSG lateral doping technologies for the p-pillar. In Fig. 2(b), the dashed line represents an estimated p-pillar from the process simulation and the secondary ion mass spectroscopy (SIMS) data. The

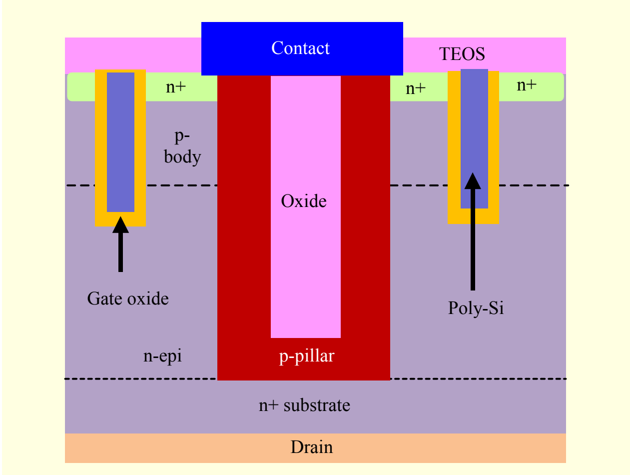

Fig. 1. Cross-sectional structure of SJ TGMOSFET fabricated with deep trench and BSG doping process technologies.

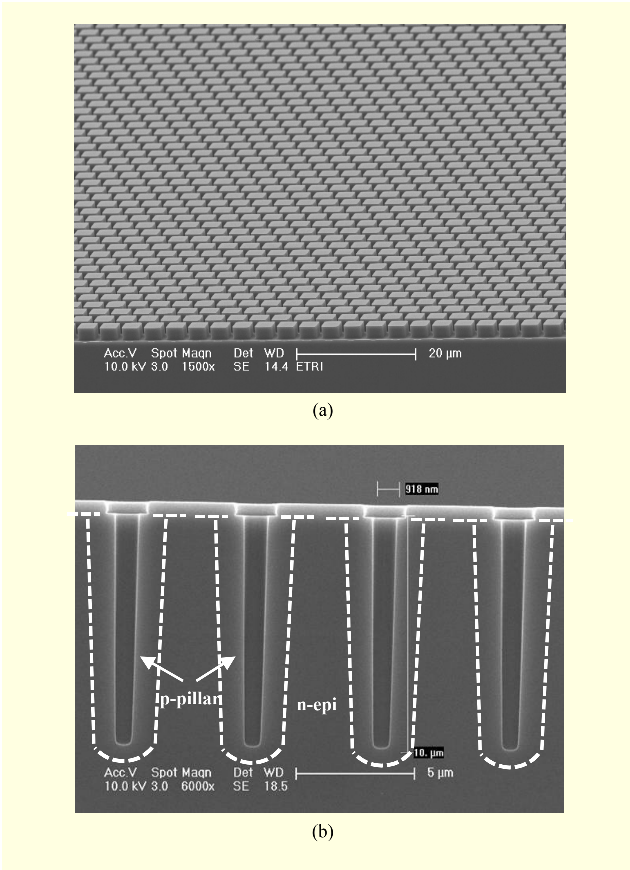

Fig. 2. SEM photograpies of (a) conventional TGMOSFET and (b) SJ TGMOSFET with deep trench and lateral boron diffused p-pillar regions.

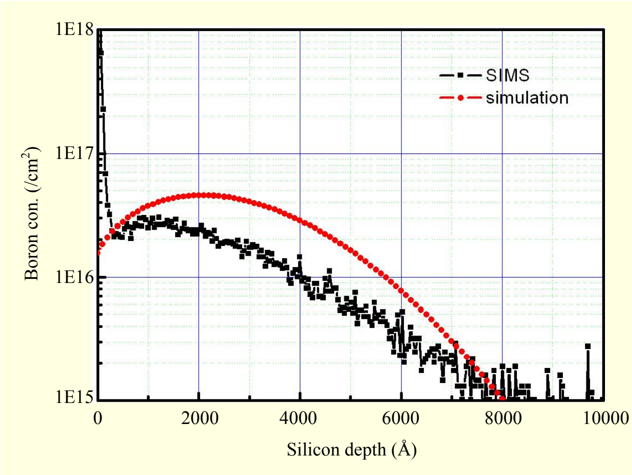

Fig. 3. Boron concentration and depth profile simulated and measured using SIMS for p-pillar region.

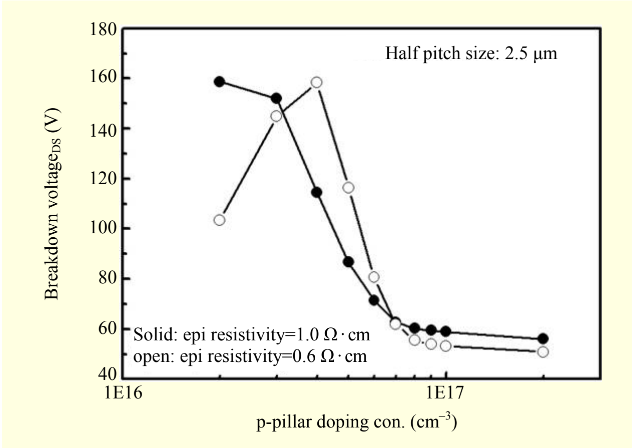

Fig. 4. Breakdown voltage variation depending on doping concentration of p-pillar.

depth and width of the trench are evaluated to be 10 μm and 0.85 μm, respectively, and have a high aspect ratio of about 11.8. Despite the trench having a high aspect ratio, as shown in Fig. 2(b), we obtain a desirable trench profile by means of the optimized combination of etching gas chemistries. The rounded corner of the trench, which effectively reduces electric field crowding, results from the hydrogen annealing technique [9].

Due to the moderately positive profile of the trench, the BSG film is deposited more uniformly inside the trench. The p-pillar doping is accomplished through this BSG film deposition and thermal annealing. For the purpose of avoiding excessive boron diffusion, the BSG film is removed before the thermal annealing. To achieve the desired breakdown voltage, the total doping concentration between the p-pillar and n-epi columns should be balanced. In the manufacturing field, it is difficult to make the doping concentrations of the p-pillar and n-pillar exactly equal, and the impact of the imbalance results in a breakdown voltage fluctuation. Particularly for an SJ TGMOSFET fabricated through lateral boron diffusion, the control of the boron concentration and profile is most critical. Throughout the various boron doping experiments, as well as the process simulations, we confirm the optimal boron concentration and the diffusion temperature for a better charge balance condition. Figure 3 shows the boron profile and concentration, which are analyzed using SIMS, and compares them with the process simulation results. The peak boron concentration diffused from the BSG film is approximately 5.0×10^{16} cm^{-3}. The p-pillar junction is located at 0.8 μm from the side wall of the trench. The slight discrepancy of doping concentration between the simulation and SIMS data results from the different diffusion coefficients due to the different silicon orientations. Moreover, the relationships between the diffusion depth depending on various process conditions and a variation in breakdown voltage are investigated.

III. Results and Discussion

To determine the optimum doping concentration of the p-pillar for the desired breakdown voltage, we simulate the breakdown voltage depending on the different doping concentrations of the p-pillars. When increasing the doping concentration of the p-pillar, the breakdown voltage is decreased, as shown in Fig. 4. However, for the SJ TGMOSFET fabricated with 0.6 Ω•cm epi resistivity, the maximum breakdown voltage is observed to be at a p-pillar concentration of 4.0×10^{16} cm^{-3}. This proves that an equal charge balance between the p-pillar and n-pillar occurs at that concentration. Investigating the effects of the trenched p-pillar on the electric field distribution and breakdown voltage of the MOSFET, a two-dimensional electric field and current flow simulations are conducted.

Figure 5(a) shows the simulated potential distribution of a conventional MOSFET with high density. In Fig. 5(b), the simulated potential distribution of the SJ TGMOSFET fabricated using a lateral boron diffusion method is presented and compared with that of a conventional TGMOSFET. The potential distribution of the conventional TGMOSFET is concentrated at the drain near the channel region, as shown in Fig. 5(a).

On the other hand, the potential of the SJ TGMOSFET is more uniformly distributed and widely spread in the bulk region of the n-drift layer under an applied drain voltage of 140 V. It is considered that these potential distributions of the SJ TGMOSFET reflect the influence of the proper charge balance between the p- and n-pillar regions.

Figure 6 illustrates the simulated current flows for

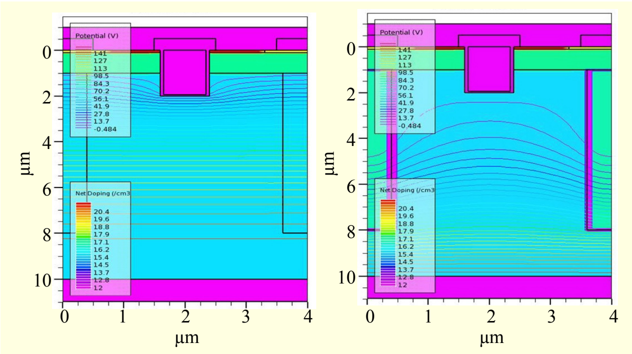

Fig. 5. Potential distribution of SJ TGMOSFET in this simulation: (a) conventional TGMOSFET and (b) SJ TGMOSFET.

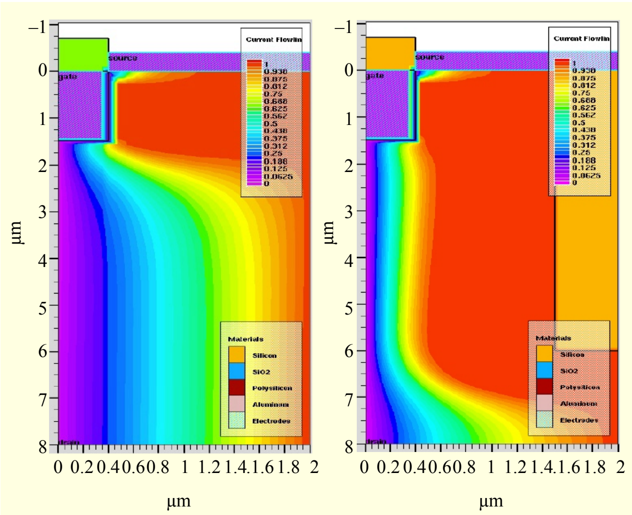

Fig. 6. Current flow simulations: (a) conventional TGMOSFET and (b) SJ TGMOSFET.

conventional and SJ TGMOSFETs. The current flow in the SJ TGMOSFET comparatively spreads uniformly through the entire n-drift region, as shown in Fig. 6(b). However, the current flow of the conventional TGMOSFET in Fig. 6(a) tends to crowd in the upper channel region and concentrate into the center of the n-drift region. This phenomenon can lead to a lower breakdown voltage for the conventional TGMOSFET. We also simulate a breakdown voltage of an SJ TGMOSFET to evaluate the effect of a boron-doped p-pillar on the breakdown voltage. As shown in Fig. 7, the breakdown voltage of an SJ TGMOSFET is higher than that of a conventional TGMOSFET. We also measure the breakdown voltages of the conventional and SJ TGMOSFET. As shown in Fig. 8, the breakdown voltage of the SJ trench gate devices is approximately 28% higher than that of conventional trench gate devices owing to the effect of the charge balance between the boron-doped p-pillar and n-drift region. However, based on the device simulation results, the R_{ON} of the SJ TGMOSFET is

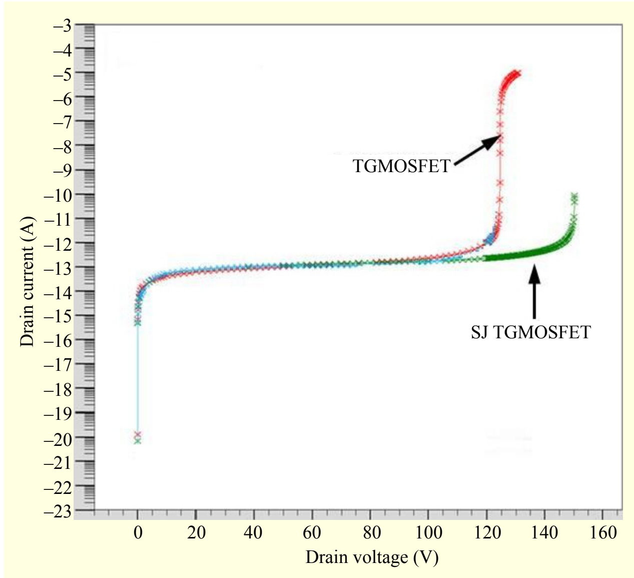

Fig. 7. Breakdown voltage simulations of conventional TGMOSFET and SJ TGMOSFET.

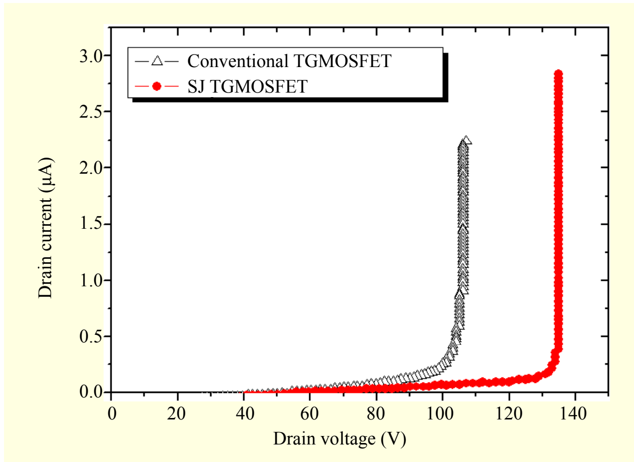

Fig. 8. Measured breakdown voltages of conventional and BSG-doped SJ TGMOSFET.

approximately 16% higher than that of the conventional TGMOSFET.

IV. Conclusion

This paper described an SJ TGMOSFET manufactured using a p-pillar forming process through the use of a deep trench and BSG doping technology to reduce the complexity of the process. The p-pillar region was built from the lateral boron diffusion from the BSG film and the annealing after the silicon deep etching process. The effects of the lateral boron doping concentration in the deep trenches on the breakdown voltages were investigated both theoretically and experimentally. Through various boron doping experiments and device simulations, we optimized the process conditions related with the p-pillar depth, boron doping concentration, and diffusion temperature. Compared to a conventional TGMOSFET, the potential distribution of the SJ TGMOSFET is more uniform and widely spread in the bulk region in the n-drift layer. As a result, the measured breakdown voltage of an SJ TGMOSFET increases over 28% compared to the conventional TGMOSFET owing to the effect of an excellent charge balance between the boron-doped p-pillar and n-drift region. However, from the device simulation results, the on-resistance of the SJ TGMOSFET is approximately 16% higher than that of the conventional TGMOSFET.

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