

# Novel Punch-through Diode Triggered SCR for Low Voltage ESD Protection Applications

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**Abstract**—This research presented the concept of employing the punch-through diode triggered SCRs (PTTSCR) for low voltage ESD applications such as transient voltage suppression (TVS) devices. In order to demonstrate the better electrical properties, various traditional ESD protection devices, including a silicon controlled rectifier (SCR) and Zener diode, were simulated and analyzed by using the TCAD simulation software. The simulation result demonstrates that the novel PTTSCR device has better performance in responding to ESD properties, including DC dynamic resistance and capacitance, compared to SCR and Zener diode. Furthermore, the proposed PTTSCR device has a low reverse leakage current that is below  $10^{-12}$  A, a low capacitance of  $0.07 \text{ fF}/\mu\text{m}^2$ , and low triggering voltage of 8.5 V at  $5.6 \times 10^{-5}$  A. The typical properties couple with the holding voltage of 4.8 V, while the novel PTTSCR device is compatible for protecting the low voltage, high speed ESD protection applications. It proves to be good candidates as ultra-low capacitance TVS devices.

**Index Terms**—ESD, Punch-through diode, SCR, Zener diode, PTTSCR

## I. INTRODUCTION

Electrostatic discharge (ESD) is a well known transient threat to sensitive electronic component and products, especially nanometer-scale electronic components and the integrated circuit (IC) chips [1]. Typical ESD damage are burnout of insulators, junctions, metal interconnects of electronic components, and the integrated circuits (ICs). Higher integration density, faster operation speed, and lower power consumption were realized as the electronic component dimension was adjusted to the nanometer scale. So the low voltage ESD protection device is required to maintain the reliability of such electronic components against ESD damages. The non-snapback transient suppressor (TVS) diode, operated in avalanche breakdown condition, is recognized to be close to the ideal ESD protection device that offer desirable electrical and ESD characteristics, including fast response time, low operating and clamping voltage, and no device degradation [2, 3]. On the other hand, TVS diodes with low breakdown voltage, less than 5 V, requires heavy doping of the base layer and operation in tunneling mechanism that is known as a Zener diode [4]. This results in high leakage current and capacitance, which is insufficient for high reliability protection with advanced technologies [5-7]. Silicon controlled rectifier (SCR) has low clamping voltage and small turn-on resistance and high current handle capably [8-10]. However, the SCR requires several modifications to decrease its triggering voltage while maintaining a high holding voltage in order to avoid latch-up.

This proposed work is to address the design of a new SCR device, punch-through diode triggered SCR

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Manuscript received Jul. 29, 2014; accepted Sep. 21, 2014

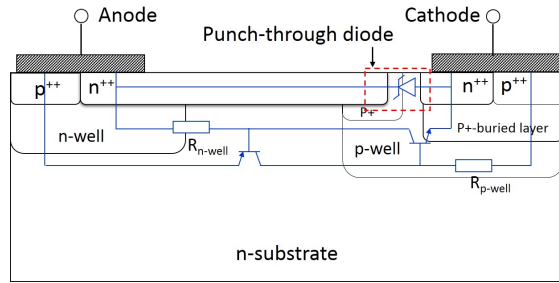
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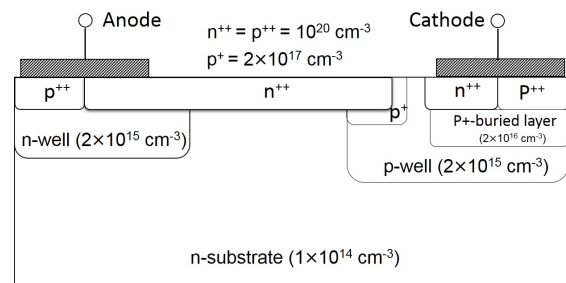
**Fig. 1.** Cross-sectional of the proposed PTTSCR.

(PTTSCR). The punch thought diode was employed to reduce the triggering voltage of SCR when it achieved the breakdown voltage below 2 V while conserving the leakage current below 1 nA [6, 11]. Then, its electrical properties were compared to the conventional TVS device through TCAD simulation software technology

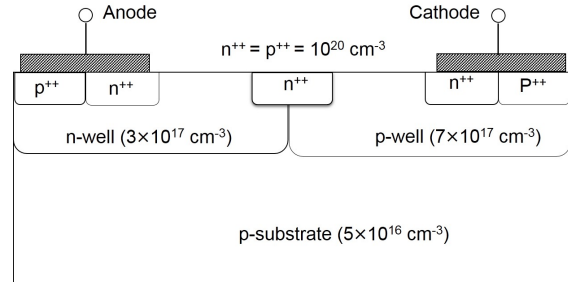
## II. DEVICE STRUCTURE

Fig. 1 shows the cross-section schematic of the navel PTTSCR structure, and the punch-through device is placed to p-well. The PTTSCR is triggered on by punch-through mechanism between  $n^{++}$ -anode and  $n^{++}$ -cathode rather than an avalanche breakdown of the well-substrate junction in a traditional SCR device that usually require heavy doping n- or p-well for low triggering voltage, which results in high leakage current and capacitance. The punch-through voltage is controlled by controlling the doping concentrate  $p^{+}$  diffusion and the space between  $n^{++}$ -anode and  $n^{++}$ -cathode. Meanwhile, the  $p^{+}$ -buried in the p-well is used to control the holding voltage, which acts as the barrier for blocking the injected carrier from the emitter to the base of an npn transistor as well as current gain controlling. Heavy doped  $p^{+}$ -buried corresponds with low emitter carrier injection and current gain. In this case, the base resistance is weakness dependent with increasing emitter- base voltage of the parasitic npn transistor as well as a applying voltage when compare with light doping, which results in high holding voltage.

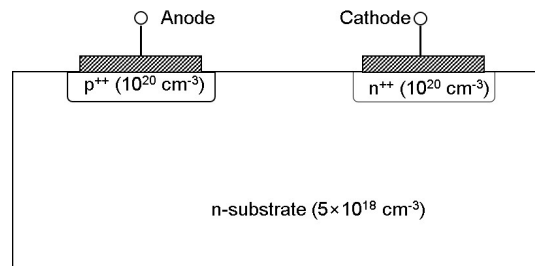
The working principle is followed. It is known that the SCR device is conducted when both parasitic npn and pnp transistors are turned-on. When the positive voltage is applied to anode pin, while the cathode is relative as the ground, the current is injected into the base region of an npn transistor by punch-through current between  $n^{++}$



(a)



(b)



(c)

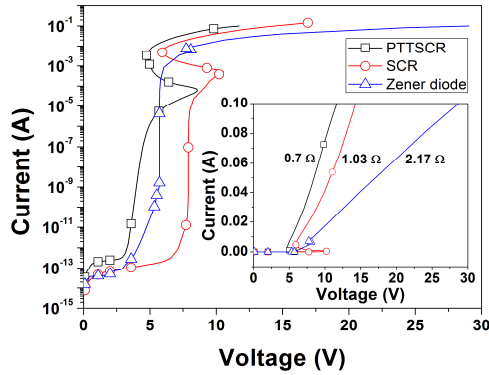
**Fig. 2.** Cross-section of analyzing ESD protection device structure (a) PTTSCR, (b) SCR, (c) Zener diode.

cathode and  $n^{++}$  anode. The injection current triggers the npn transistor of voltage across its emitter-base equal to 0.7 V. The turning on of an npn transistor also inject the electron current to bias pnp transistor turn on. Finally, SCR is in full conduction.

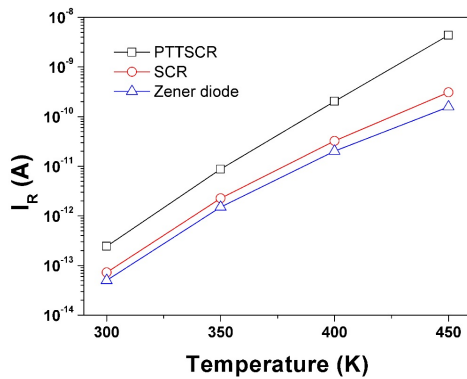
## III. DEVICE SIMULATION AND RESULTS

The ESD protection devices used in this investigation and comparison include a novel PTTSCR, Zener diode, convention SCR device (See Fig. 2). The electrical properties such as I-V and C-V characteristics were performed through TCAD Athena and Atlas Silvaco simulation.

Fig. 3 shows the I-V characteristics of three device structures. It is notable that the PTTSCR was triggered



**Fig. 3.** Comparing I-V characteristics of three device structures.

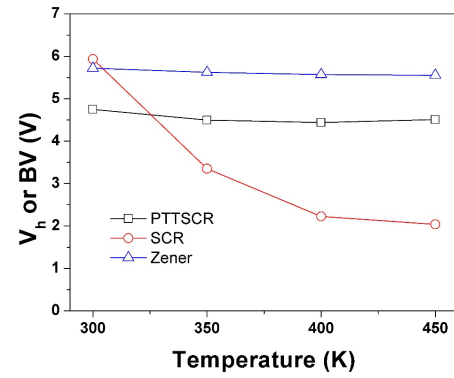


**Fig. 4.** Temperature dependent of leakage current simulated from three device structures.

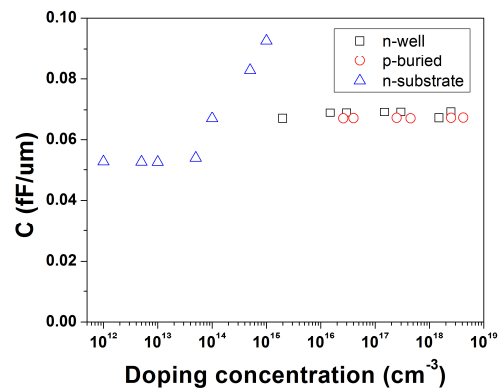
on at 8.5 V with current of  $5.6 \times 10^{-5}$  A, which is lower compared to the conventional SCR structure of 10.5 V and  $5.4 \times 10^{-4}$  A. Moreover, the holding voltage ( $V_h$ ) of the PTTSCR is about 4.8 V, which is compatible for low voltage applications.

The temperature dependent of reverse leakage current is given in Fig. 4, demonstrated that the SCR and Zener diode were beneficial in achieving low leakage current levels at all temperature ranges. Even through the PTTSCR is strongly temperature-dependent in terms of reverse leakage current, it has a negligible smaller temperature coefficient of holding voltage compared to an SCR device as shown in Fig. 5. This indicates that the new PTTSCR device is operating in a high temperature environment as 400 K when its reverse leakage current and holding voltage were maintained below  $10^{-8}$  A and closed to the original value (see Figs. 4 and 5).

Furthermore, among all device structures, the PTTSCR shows a lower DC dynamic resistance ( $R_D$ ) value. The  $R_D$  calculated from the linear region of Fig. 3



**Fig. 5.** Temperature dependent of BV or  $V_h$  simulated from three device structures.



**Fig. 6.** Capacitance at zero bias plotted as a function of the doping concentration of n-well, p-buried and n-substrate (for each case, another parameters were set as default value (see Fig. 2(a))).

was  $0.70 \Omega$ , meanwhile the SCR was  $1.03 \Omega$  and  $2.17 \Omega$  for the Zener diode at the active area of  $100 \mu\text{m}^2$  (see inset of Fig. 3). Typical smaller dynamic is a strong point in terms of minimizing the energy absorption of the device as well as Joule heating and improved ESD performance as found in previous works [2, 3]. The heating problem is known to be the major cause of degradation and failure in devices.

Finally, the capacitance was analyzed. The capacitance is known as an important parameter of the ESD protection device that represents a speedy response time in absorbing transient energy like ESD events. Therefore, for the fast device, the capacitance should be smaller as much as possible, in order to minimize the RC time constant that known as the limiting speed parameter of device [12]. Fig. 6 plots the capacitance as a function of various doping parameters that simulated from the

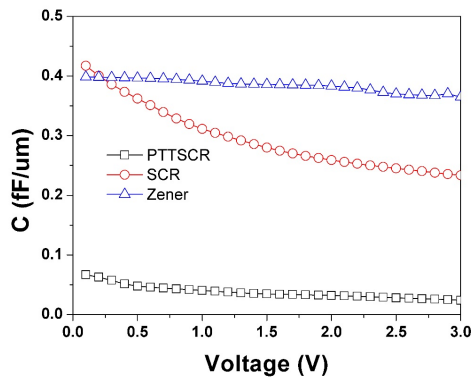


Fig. 7. C-V characteristic curve simulated from three device structures at the frequency of 1 MHz.

PTTSCR structure. It is found that the capacitance is independent on the doping concentration of the n-well and p-buried, but it dominated by the n-substrate layer. Since the original PTTSCR structure used a low substrate and well-doping concentration, a smaller capacitance value would be an expected achievement. The capacitance value simulated from all device structures were plotted in Fig. 7. The PTTSCR shows an extremely small capacitance value that is lower than other devices by about 6 times. Typically the smaller capacitance value not only behaviors as a high speed device, but it is also advantageous in high speed data applications in terms of minimizing signal attenuated at high frequency and increase cut off frequency [13].

## V. CONCLUSIONS

The performance of the novel punch-through device triggered SCR was performed through the TCAD simulation. The result showed that the novel PTTSCR device has a low leakage current below  $10^{-12}$  A, a low triggering voltage of 8.5 V, a high holding voltage of 4.8 V, a small capacitance of  $0.07 \text{ fF}/\mu\text{m}^2$ , and a small dynamic resistance. In comparison, the novel PTTSCR device shows better and higher ESD performance than the SCR and Zener diode in accordance with the DC dynamic resistance and capacitance. This guarantees that the novel PTTSCR is capable of protecting low-voltage high-speed applications and good candidates, such as a ULC-TVS device.

## ACKNOWLEDGMENTS

This work was supported by a Basic Research Laboratory Program (2011-0027956) through the Ministry of Education of the Republic of Korea, and by a Converging Research Center Program (2013K000404) through the Ministry of Science, ICT & Future Planning of the Republic of Korea. It was also supported by supported by the Future Semiconductor Device Technology Development Program (Grant No. 10044651), funded by the Ministry of Trade, Industry & Energy of the Republic of Korea, and by the Korea Semiconductor Research Consortium.

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