V_T-Modulation of Planar Tunnel Field-Effect Transistors with Ground-Plane under Ultrathin Body and Bottom Oxide

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***Abstract*—Control of threshold voltage (V_T) by ground-plane (GP) technique for planar tunnel field-effect transistor (TFET) is studied for the first time using TCAD simulation method. Although GP technique appears to be similarly useful for the TFET as for the metal-oxide-semiconductor field-effect transistor (MOSFET), some unique behaviors such as the small controllability under weak ground doping and dependence on the dopant polarity are also observed. For V_T-modulation larger than 100 mV, heavy ground doping over 1×10^{20} cm^{-3} or back biasing scheme is preferred in case of TFETs. Polarity dependence is explained with a mechanism similar to the punch-through of MOSFETs. In spite of some minor differences, this result shows that both MOSFETs and TFETs can share common V_T-control scheme when these devices are co-integrated.**

***Index Terms*—Threshold voltage, Tunnel field-effect Transistor (TFET), ground-plane, ultrathin body and bottom oxide (UTBB), TCAD simulation**

I. INTRODUCTION

Recently various tunneling-injection floating-body devices, so called tunnel field-effect transistors (TFETs), have been massively studied as a single device due to the extraordinary subthreshold characteristics and capability of low-voltage operation [1-4]. However, there is a lack of studies on practical V_T-control schemes compatible with existing low power circuit design techniques [5, 6]. Although a device design with the V_T-control doping region was recently proposed from this perspective, needs of asymmetric angled doping process and restriction in the direction of gate lines can limit the practical usefulness [7].

A similar problem in a fully-depleted silicon-on-insulator metal-oxide-semiconductor field-effect transistor (FDSOI-MOSFET) is studied with the ground-plane (GP) or back-gate technique proposed by Xiong *et al.* (Fig. 1) [8]. Recently this scheme was successfully demonstrated to implement multi-V_T options for metal-gate/high- MOSFETs using ultrathin body and bottom oxide (UTBB) SOI substrate [9].

In this work, we verify the extendibility of GP

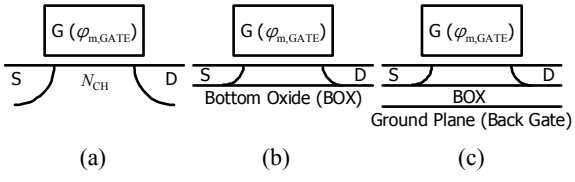

Fig. 1. V_T-control schemes of (a) bulk device, (b) ultra-thin-body silicon-on-insulator (UTB-SOI) device, (c) ultra-thin-body-and-box silicon-on-insulator (UTBB-SOI) device.

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technique to TFETs with the commercial device simulator SILVACO ATLAS™ [10]. For the accurate calculation, the built-in non-local tunneling model and the Fermi-Dirac statistics are used with 0.15-nm interval of quantum mesh defined near the tunneling region.

II. Model Device and Definition of Parameters

Fig. 2 and Table 1 summarize the model structure used in this study. Based on the recent studies on UTBB-SOI MOSFETs, the baseline device is defined with 6 nm of SOI and 10 nm of BOX with the raised source/drain [9, 11]. To maximize the current drivability, the source junction is designed within a narrow bandgap material [12]. The drain-side sidewall is formed thicker than the other to suppress the unwanted drain-side tunneling current at off-state.

Fig. 3 shows the typical transfer characteristics of the model device with V_{DS} = 1 V. Since the definitions of V_T for the MOSFET based on the strong inversion of the channel are not applicable to TFET, the simple constant current method with a threshold current I_T of 0.1 A/μm is used to define V_T. Change in the energy band diagram at the defined V_T is shown in Fig. 4. As for subthreshold swing (*SS*), the slope of I_D-V_{GS} curve in Fig. 3 continuously changes below V_T unlike those of MOSFETs. This is because the subthreshold current of a TFET is governed by the band-to-band tunneling mechanism, not by the statistical diffusion. Therefore, the *SS* is defined as the average swing between V_T and V_T - 0.3×V_{DD}. Calculating the average *SS* within a fixed interval makes it possible to compare the steepnesses of different subthreshold curves regardless of the V_Ts. The value of 0.3×V_{DD} is used because the V_Ts of MOSFETs in logic CMOS technology have been scaled to be

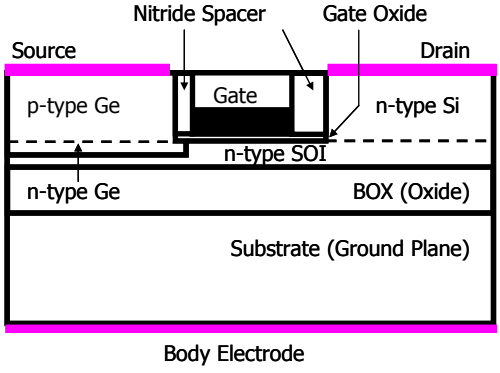

Fig. 2. Structure of model device: The doped substrate region under bottom oxide acts as the GP layer.

Table 1. Parameters of baseline device

Design Parameters	Value
Gate length	24 nm
Gate oxide thickness (T_{gox})	1 nm
SOI thickness	6 nm
BOX thickness (T_{box})	10 nm
Left-sidewall length	4 nm
Right-sidewall length	8 nm
Thickness of raised S/D	15 nm
n-type Ge thickness	3 nm
p-type Ge doping	1×10^{20} cm^{-3}
n-type Ge doping	1×10^{13} cm^{-3}
Doping of SOI	1×10^{15} cm^{-3}
n-type Si doping	1×10^{15} cm^{-3}
Gate work function	4.61 eV

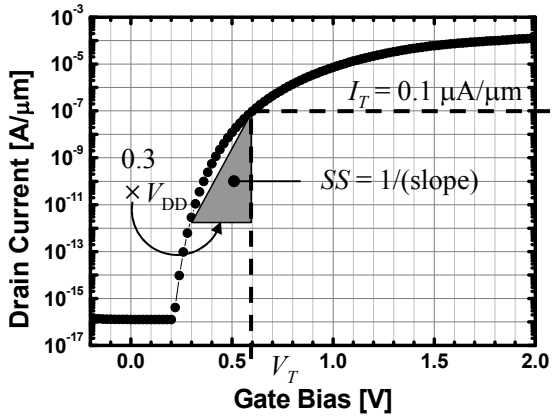

Fig. 3. Definitions of threshold voltage (V_T) and subthreshold swing (*SS*) in this study: Here V_T is defined by the threshold current method with I_T = 0.1 μA/μm. Here V_{DS} = 1 V.

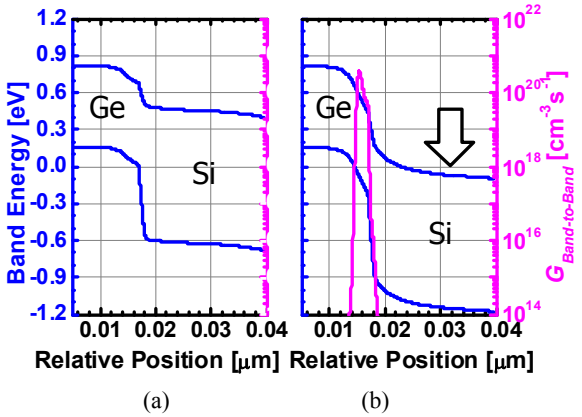

Fig. 4. Energy band diagrams and band-to-band tunneling rate at 0.5 nm below the gate oxide with (a) V_G = 0 V, (b) V_G = V_T. Here V_{DS} = 1 V.

approximately this value in order to keep both a large drive-current and small off-current.

III. RESULTS AND DISCUSSION

First, the V_T-modulation of the baseline device and that of MOSFET are compared with variation of the GP doping from 1×10^{14} to 1×10^{21} cm^{-3} with V_{DS} = 1 V (Fig. 5). The smaller modulation under light doping conditions and with thicker BOX designs is attributed to higher field-sensitivity of the carrier injection of TFET devices. It also shows that the GP technique for the FDSOI-MOSFET is similarly useful for TFETs if heavy GP doping is used.

Next, the asymetric sensitivity to the polarity of GP doping is investigated using energy band contours in Fig. 6. While p-type GP blocks the field penetration from the drain and influences on the potential at the tunneling point, n-type GP lets the drain field into the channel region and loses its controllability over the potential at the point. Therefore, p-type doping modulates V_T more efficiently than n-type does. Meanwhile, since the *SS* in this work is defined as the average swing between V_T and V_T - 0.3×V_{DD} and the change of GP doping does not mean the change of doping in the SOI region, the *SS* remains unchanged regardless of the GP doping (Fig. 7).

Finally, the effectiveness of GP technique in the devices with a change of gate dielectric is studied in Figs. 8 and 9. Although smaller T_{gox} helps to reduce V_T, it also narrows down the window within which GP doping can modulate V_T. As the BOX gets thinner, GP doping exerts more influence over V_T to the contrary. These are understood from the simple capacitance network model described in Fig. 10. Since the potential at the tunneling point is determined by the capacitive coupling ratios in the network, tighter coupling to the top gate potential leads to reduced modulation window with GP. The

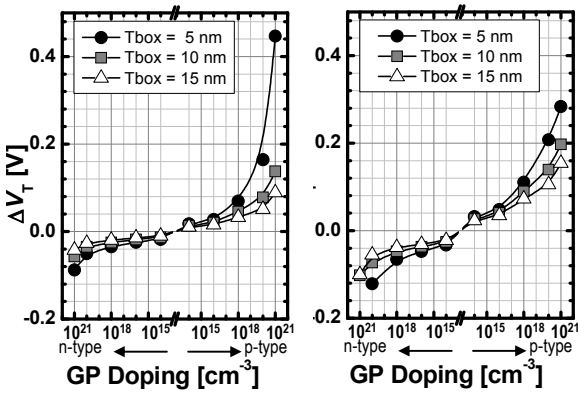

Fig. 5. Modulation of V_T with GP doping (a) TFET, (b) MOSFET. Here the MOSFET device differs from the TFET only in the polarity of source.

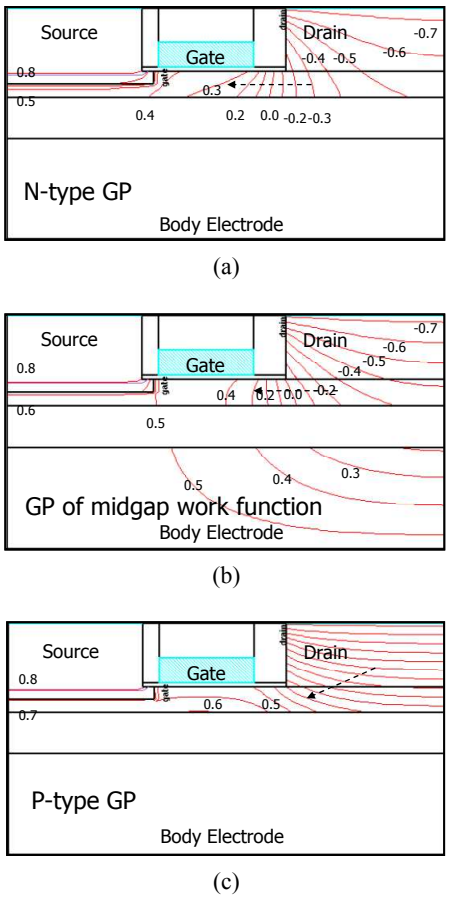

Fig. 6. Contours of conduction band energy with V_G = 0 V and V_{DS} = 1 V (a) n-type GP doping, (b) midgap GP, (c) p-type GP doping.

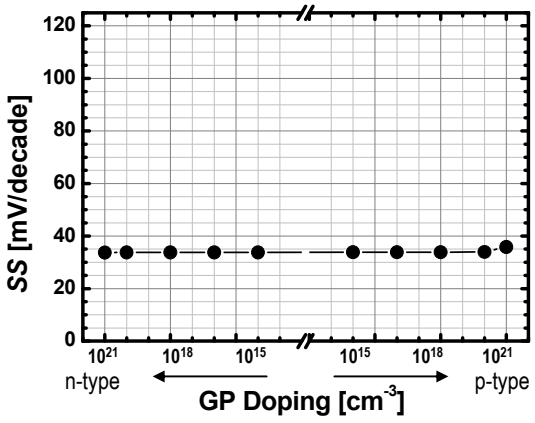

Fig. 7. Change of the *SS* of the model TFET with GP doping.

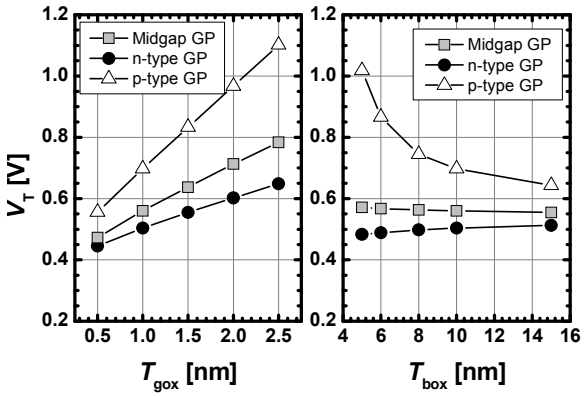

Fig. 8. Change of V_T-modulation with gate dielectric thicknesses (a) top-gate oxide, (b) bottom oxide. Here the dopings for GPs are all 1×10^{21} cm^{-3}. Gate work function is at the midgap.

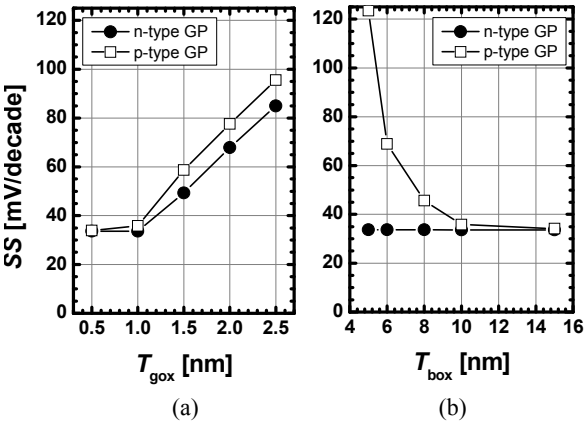

Fig. 9. Change of the *SS* with gate dielectric thicknesses (a) top-gate oxide, (b) bottom oxide. Here the dopings for GPs are all 1×10^{21} cm^{-3}.

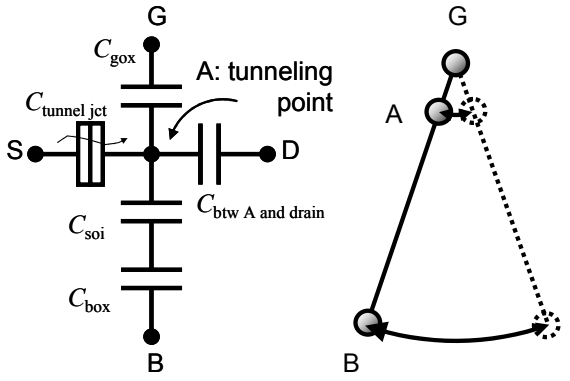

Fig. 10. Simple equivalent capacitor network model.

degradation of *SS* in Fig. 9 can be similarly explained. In the case of n-type GP-doping, the change in *SS* with BOX thickness is insignificant because the field from the drain weakens the coupling of potentials between GP doping region and the tunneling point.

III. CONCLUSIONS

We confirmed that the ground-plane technique for the UTBB-SOI MOSFET device is extendible to TFETs. Due to higher sensitivity to electric field, the effectiveness of GP doping in TFET was relatively smaller than that in MOSFET. P-type GP doping blocks the field from the drain only to increase the V_T. Since the capacitive coupling effect can degrade *SS*, a compromise between V_T-modulation window and *SS* degradation is needed. This is practically important in that both MOSFET and TFET can share common V_T-control scheme when these devices are co-integrated.

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