

Assistive Circuit for Lowering Minimum Operating Voltage and Balancing Read/Write Margins in an SRAM Array

Changhwan Shin

Abstract—There is a trade-off between read stability and writability under a full-/half-select condition in static random access memory (SRAM). Another trade-off in the minimum operating voltage between the read and write operation also exists. A new peripheral circuit for SRAM arrays, called a variation sensor, is demonstrated here to balance the read/write margins (*i.e.*, to optimize the read/write trade-off) as well as to lower the minimum operation voltage for both read and write operations. A test chip is fabricated using an industrial 45-nm bulk complementary metal oxide semiconductor (CMOS) process to demonstrate the operation of the variation sensor. With the variation sensor, the word-line voltage is optimized to minimize the trade-off between read stability and writability ($V_{WL,OPT} = 1.055$ V) as well as to lower the minimum operating voltage for the read and write operations simultaneously ($V_{MIN,READ} = 0.58$ V, $V_{MIN,WRITE} = 0.82$ V for supply voltage (V_{DD}) = 1.1 V).

Index Terms—Variability, CMOS, SRAM

I. INTRODUCTION

The steady miniaturization of transistors in every new generation of complementary metal oxide semiconductor (CMOS) technology is the major driving force that exponentially increases transistor density in integrated

circuits (ICs) [1]. As a result, the storage capacity of cache memory [*i.e.*, static random access memory (SRAM)] in IC chips such as the central processing unit (CPU) and the digital signal processor (DSP) has almost doubled in every new CMOS generation. However, this advancement has not only provoked an ever-increasing power density issue but has also caused a process-induced variability issue, especially in sub-100-nm CMOS technology nodes. Considering that more than half of the total chip area is occupied by SRAM arrays in IC chips, it is necessary to develop a circuit technique that (i) lowers power consumption in standby mode by minimizing operating voltage without losing the data stored in SRAM arrays, and (ii) enables a balance between the read and write margins at the minimum operating voltage under harsh process-induced variations to ensure the robustness and stability of SRAM arrays. In the work presented here, variation sensors were fabricated using an industrial 45-nm bulk CMOS technology near SRAM arrays, and they achieved both of the aforementioned requirements (*i.e.*, lowering minimum operation voltage for the read and write operations and balancing the read/write margins).

II. ASSISTIVE CIRCUIT

In an SRAM array, the SRAM bit cells controlled by the identical word-line voltage (*i.e.*, on the same row in the SRAM array) have to be writable as well as robust against half-select upset. It is well known that there is a trade-off between stability and write speed under the half-select condition, which can be measured by the read

static noise margin (RSNM) [2]. Increasing the ratio of the strength of the pass-gate (PG) transistor to that of the pull-up (PU) transistor can improve writability but degrades the RSNM. Conversely, decreasing the ratio of the strength of the PG transistor to that of the PU transistor can degrade writability but improves the RSNM. Because of the trade-off between the read and write margins, optimizing for writability worsens the half-select read stability, and vice-versa. A new peripheral circuit for SRAM arrays (Fig. 1) is presented to balance the read/write margins (*i.e.*, to optimize the read/write trade-off) as well as to lower the minimum operating voltage for the read and write operations (*i.e.*, $V_{MIN,READ}$ and $V_{MIN,WRITE}$). Under the process and voltage and temperature variation, the optimal word-line voltage ($V_{WL,OPT}$) is generated using multiple-variation sensor cells (*i.e.*, 16 sensors connected in a row) with a gate and active SRAM layouts (Fig. 1(c)). Fig. 1(a) shows the schematic of the single variation sensor including two half-cells that are configured for a worst-case read

situation (left-hand side of Fig. 1(a)) and a worst-case write situation (right-hand side of Fig. 1(a)). The worst-case write condition corresponds to a voltage divider with the PG device contesting a fully-on PU device to bring the internal node voltage (V_{in_write}) low, and the worst-case read condition consists of a resistive voltage divider with a fully-on pull-down (PD) transistor contesting the adjacent PG device to bring the internal node voltage (V_{in_read}) to a low value.

Note that the layout of the sensor is used up through the metal-1 layer to ensure maximum sensitivity to layout-sensitive variation. Fig. 1(b) shows the die photo of the test chip in which the variation sensors are positioned near the SRAM arrays, and Fig. 1(c) shows the entire block diagram, which exhibits how the single operational-amplifier is connected through a transmission multiplexer.

There are inverse sensitivities to PG in terms of read/write margins in SRAM bit-cells, so that if systematic/random variations occur in SRAM bit-cells, (i) V_{in_read} would be higher than a certain nominal value, resulting in the degraded read margin, and (ii) V_{in_write} would be higher than a certain nominal value, resulting in the degraded write margin. With this point in mind, we can draw on the fact that the variation sensor using the identical layout of the SRAM bit-cells through “metal 1” is able to sense the worst case V_{in_read} and V_{in_write} , resulting in the optimal word-line voltage (V_{WL}) for balancing the read/write margins. In other words, if the sensor can detect the penalty in the read margin (*i.e.*, V_{in_read} is higher than expected, due to variations that happened in the SRAM bit-cells), virtually shorting the V_{in_read} with V_{in_write} via the operational-amplifier compensates for the loss of the read margin thanks to the relatively increased write margin (*i.e.*, V_{in_write} should be lower than expected, due to the inverse sensitivities to PG).

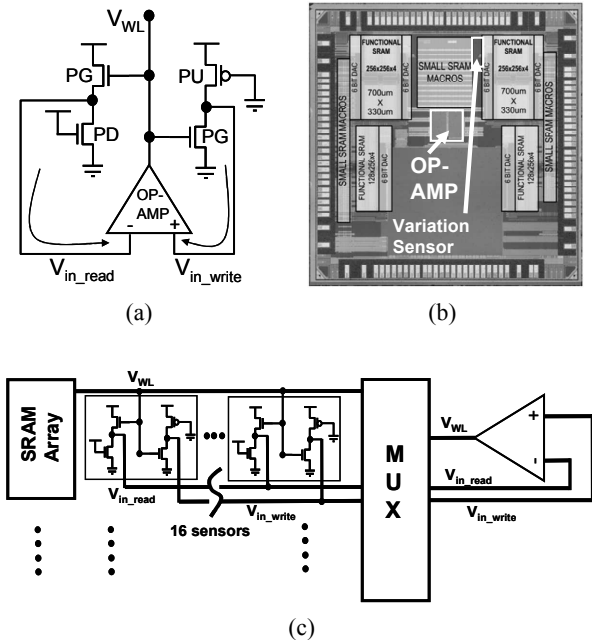


Fig. 1. (a) Schematic of the variation sensor: the operational-amplifier (op-amp) changes V_{WL} to optimize the read/write trade-off that occurs because of process-induced variations, (b) Die photo of the test chip. The sensors are located near the SRAM array, sharing the op-amp through the multiplexer (MUX), (c) Configuration of the 16-variation sensors with the MUX and op-amp to adjust V_{WL} within 10 mV of σV_{WL} . The op-amp is a single-stage folded-cascode amplifier with a gain (> 60 dB) in a $9000 \mu m^2$ area. Thick-oxide (tolerable up to 1.8 V) transistors with V_{DD} of 1.1 V were used to make sure a high gain and small 3σ offset of 2.4 mV.

III. MEASUREMENT RESULT & DISCUSSION

The bit-lines and word-lines are accessible only from the pins of the test chip. As a result, the bit-line read margin (BLRM) and bit-line write margin (BLWM) are measured to quantify read stability and writability, respectively [3]. Note that the BLRM is defined as the difference between the power supply voltage of the cell

(V_{DD}) and the smallest cell supply voltage that can retain the original state of the cell with a bit-line and word-line voltage of V_{DD} . The BLWM is defined as the highest bit-line voltage that can flip the original state of the cell with the word-line voltage and the opposite-side bit-line voltage of V_{DD} .

As shown in Fig. 2(a), the measured V_{WL} ($V_{WL,MEAS} = V_{DD} = 1.1$ V) for the SRAM array without the variation sensor is not optimal in terms of balancing the read and write margins (*i.e.*, $BLRM < BLWM$). The optimal word-line voltage ($V_{WL,OPT}$) generated by the variation sensors, however, lowers the V_{WL} by 45 mV in order to balance the read and write margins (*i.e.*, $BLRM = BLWM$). Fig. 2(b) shows the measured results of the read/write fail-bit count when V_{DD} is lowered from 1.1 V to 0.2 V and V_{WL} is $V_{WL,OPT}$. Because the read and write margins are balanced by the variation sensors, $V_{MIN,READ}$ is lowered without the degradation in $V_{MIN,WRITE}$ (not even a slight reduction in $V_{MIN,WRITE}$). In other words, the V_{WL} adjusted by the variation sensors not only balances the read/write margins but also simultaneously minimizes $V_{MIN,READ}$ and $V_{MIN,WRITE}$. Hence, the power consumption can be reduced when SRAM is operating at the minimum operating voltage, *i.e.*, in idle or standby mode.

Due primarily to the scaling challenges of the SRAM transistors, such as random/intrinsic variations, the read/write characteristics of the SRAM bit-cells have been controlled by peripheral circuits: (i) for the read margin: hierarchical or short bit-lines and read-assist

circuits [4-7], and (ii) for the write margin: write-assist circuits [8-10]. In using the read-assist circuits, the pass-gate disturbance can be reduced by decreasing the word-line voltage or the bit-line pre-charge voltage. On the other hand, in using the write-assist circuits, the pass-gate strength can be increased by boosting the word-line voltage or applying the negative bit-line voltage. Those read/write-assist circuits present conflicting requirements on SRAM device ratios, so that they should provide dynamic modulation of the device ratios. However, this work provides the static modulation of the device ratios as well as dynamically-balanced read/write margins under process-induced variations.

In [4-7], the tunable resistors in the word-line driver to adjust the word-line voltage high level were distributed across the SRAM array's rows/sub-arrays to amortize the area. They are akin to pass-gate threshold-voltage adjustment, but provide post-silicon tuning. This read-assist technique, however, would degrade read current as well as write-margin, so that this technique is an option if the performance target is slow, otherwise write-assist techniques should be used together.

In [8-10], the lower bit-line pre-charge voltage (generated by a local regulator, n-type device's pre-charge, or pulse techniques) can suppress cell disturbance. The optimal bit-line voltage is about 70% to 80% of power supply voltage, due mainly to reverse stability limitations. This write-assist technique, however, would degrade read current due to lower drain-to-source voltage in a pass-gate device.

In [11], the capacitively boosted word-line above power supply voltage (V_{DD}) would make the pass-gate device stronger, resulting in improved write-margin. The coupling happens once the word-line voltage reaches full V_{DD} and is floated. However, it would have the timing delay issue for boost (*e.g.*, negative clock edge) as well as cause a degraded read-margin in half-selected bit-cells. Of course, reliability concerns for the word-line over-voltage should be taken into account in using this write-assist technique.

In [4] and [10], the capacitively boosted bit-line is below ground voltage. The coupling occurs after the bit-line voltage reaches ground and is floated. As with using the word-line boosting technique for improving the write-margin [11], this technique should consider the timing delay issue for boost as well as the pass-gate

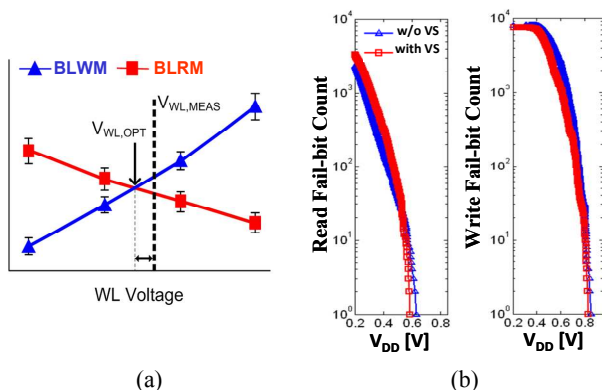


Fig. 2. (a) Data are measured from the bit cells of an array. Whiskers on each box indicate \pm one standard deviation, and the V_{WL} difference between two data points is 0.2 V. Note that the $V_{WL,MEAS}$ is V_{DD} of 1.1 V, (b) Read (left-hand side) and write (right-hand side) fail-bit counts when $V_{WL} = V_{WL,OPT}$. $V_{MIN,READ}$ with the variation sensor (VS) is 0.58 V, but without the variation sensor is 0.67 V. $V_{MIN,WRITE}$ with the variation sensor is 0.82 V, but without the variation sensor is 0.83 V.

Table 1. Comparison of various figures of merit

Figures of merit	This work	Read-assist: word-line under-drive [4], [5], [6], [7]	Read-assist: Regulated bit-line [8], [9], [10]	Write-assist: word line boost [11]	Write-assist: Negative bit-line [4], [10]	Write-assist: Cell supply collapse [11], [12], [13]
Read-margin	Balancing read & write	Improved	Improved	Degraded	Degraded	OK
Write-margin		Degraded	Degraded	Improved	Improved	Improved
Area penalty (cell efficiency)	Small	Small	Small	Small	Small	Small
V_{min}	Lowering for read/write	Lowering for read	Lowering for read	Lowering for write	Lowering for write	Lowering for write

device’s leakage in unselected rows.

Lastly but not least, in [11-13], the cell supply voltage (V_{DD}) was dynamically collapsed in the write-operation. This was implemented with a supply switch to the 2nd supply or floating voltage. However, the key technical issue depends on the data-retention voltage (DRV) of unselected bit-cells in the same column. If the collapsed V_{DD} is higher than the DRV [11, 12], the data stored would not be lost but would require a certain amount of restoring time. If the collapsed V_{DD} is lower than the DRV to achieve the maximum benefit from using the write-assist technique [13], the bit-cell is essentially shut off. But as long as the write speed is fast enough, the dynamic SRAM retention would not lose the stored data, akin to the DRAM’s.

With the understanding of the benefits and trade-offs in each technique, the qualitative comparison to this work is summarized in Table 1. Due to different technology used in each work, a quantitative comparison would not be appropriate.

IV. CONCLUSION

A variation sensor, a new type of peripheral circuit for an SRAM array, was designed and fabricated in a test chip employing an industrial 45-nm bulk CMOS process. The optimal word-line voltage for balancing the read and write margins was generated by the variation sensor consisting of 16 half-cells (*i.e.*, eight for the worst-case read and eight for the worst-case write). While the word-line voltage is optimally adjusted for balancing the read/write noise margins, the minimum operation voltage for the read and write operations was simultaneously reduced. The standby power consumption can be lowered

when the SRAM array runs at the minimum operating voltage.

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Changhwan Shin received the B.S. degree (top honors) in Electrical Engineering from Korea University, Seoul, Korea, in 2006 and the Ph.D. degree in Electrical Engineering and Computer Sciences from the University of California, Berkeley, in

2011. In 2011, he joined the Silicon Technology Group, Xilinx Inc., San Jose, CA, as a Senior Process/Device Engineer. In 2012, he joined the Faculty of the University of Seoul, Seoul, Korea. His current research interests include advanced CMOS device designs and their applications to variation-robust SoC memory and logic devices, as well as post-silicon technology such as paper electronics. Prof. Shin was the recipient of a fellowship from the Korea Foundation for Advanced Studies (KFAS) in 2004, the General Electric Foundation Scholar Leaders Award in 2005, the Best Paper Award and the Best Student Paper Award at the IEEE International SOI Conference in 2009, and the Best Paper Award at the European Solid State Device Research Conference (ESSDERC) in 2010. He has been serving on technical committees for the IEEE International SOI conference (now SOI-3D-Subthreshold, or S3S conference) and the European Solid State Device Research Conference (ESSDERC) since 2011. He has been serving on Associate Editor for *Advances in Electrical Engineering* (since 2012) and on Lead Guest Editor for *Journal of Electrical and Computer Engineering* in 2014.