Immunity Test for Semiconductor Integrated Circuits Considering Power Transfer Efficiency of the Bulk Current Injection Method

NaHyun Kim, Wansoo Nah, and SoYoung Kim

Abstract—**The bulk current injection (BCI) and direct power injection (DPI) method have been established as the standards for the electromagnetic susceptibility (EMS) test. Because the BCI test uses a probe to inject magnetically coupled electromagnetic (EM) noise, there is a significant difference between the power supplied by the radio frequency (RF) generator and that transferred to the integrated circuit (IC). Thus, the immunity estimated by the forward power cannot show the susceptibility of the IC itself. This paper derives the real injected power at the failure point of the IC using the power transfer efficiency of the BCI method. We propose and mathematically derive the power transfer efficiency based on equivalent circuit models representing the BCI test setup. The BCI test is performed on I/O buffers with and without decoupling capacitors, and their immunities are evaluated based on the traditional forward power and the real injected power proposed in this work. The real injected power shows the actual noise power level that the IC can tolerate. Using the real injected power as an indicator for the EMS test, we show that the on-chip decoupling capacitor enhances the EM noise immunity.**

Index Terms—**Electromagnetic susceptibility (EMS), bulk current injection (BCI), circuit immunity, on-chip decoupling capacitor, power transfer efficiency**

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I. INTRODUCTION

Due to the demand for high performance in electronic equipment, the density of transistors has increased and multi-chip package (MCP) and system in package (SiP) technologies have become widely used. In addition, as operating frequencies of processors have increased and circuits have become more complex, it has become impossible to ignore the large amounts of parasitic emissions generated by integrated circuits (IC). In an electromagnetic environment, cables and PCB traces can be used as the coupled route of the radio-frequency (RF) noise. Due to the demand for low power ICs, circuits are designed with reduced supply voltages resulting in the degradation of circuit immunity levels. Therefore, it is required to predict the EMS of the IC at the design stage and to perform EMS tests once the IC is fabricated [1, 2].

The international electrotechnical commission (IEC) established a standard for measuring the susceptibility characterization of IC electromagnetic (EM) wave up to 1 GHz, IEC 62132. IEC 62132-1 provides general information on the measurement of conducted and radiated EMS [3]. The BCI test, defined in IEC 62132-3, is a method for measuring the immunity of the IC in the presence of conducted RF disturbances [4]. Fig. 1 shows the basic test set-up for the BCI immunity test. Through the BCI test, RF current is injected onto one or a combination of wires.

BCI test modeling and simulation on I/O buffer circuits of low power mobile ICs were conducted in [5]. Forward power, which is the output power level of the RF noise generation source when the IC malfunctions,

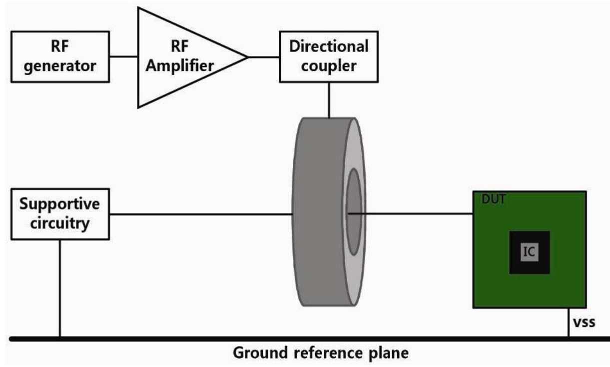


Fig. 1. Basic component for BCI test [4].

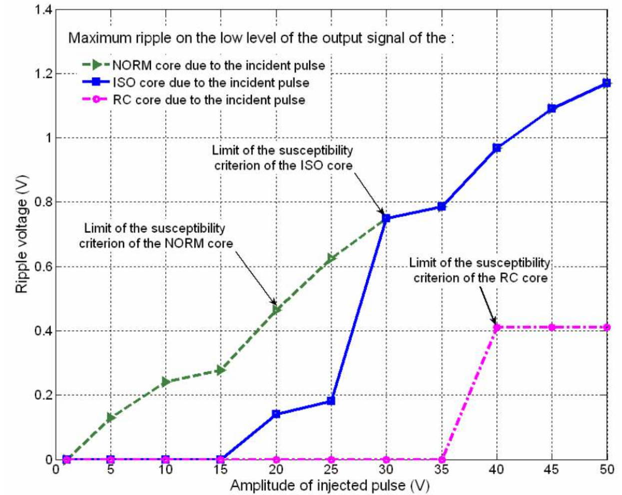


Fig. 2. Comparison between the immunities of the basic, the substrate insulation, and the on-chip decoupling capacitor IC [7].

has been used as an indicator of circuit immunity in previous research [5, 6]. However, the actual power injected to the IC depends on the frequency of injected EM noise and the transfer characteristics of the measurement equipment, the PCB, the package, and the IC impedance. Therefore, using the forward power as the indicator of circuit immunity cannot present the susceptibility of the IC itself. Particularly, in BCI, using the measured forward power as the indication of circuit immunity can be wrong because a significant amount of power is lost in the BCI probe and the subsequent noise injection path on the PCB and the package. In this work, we obtain an accurate model of power transfer efficiency throughout the RF injection path by creating an equivalent circuit model of the BCI test components and by extracting the input impedance of the IC. We calculate the formula for the power transfer efficiency when the RF power transfers from the RF generator to the IC. Using the power transfer efficiency, the real injected power into the IC can be derived and used as a new indicator of the susceptibility.

Many approaches have been proposed to enhance the immunity of ICs. In particular, Alaeldine compared the susceptibilities of a standard IC, an IC with a substrate insulation layer, and an IC with on-chip decoupling capacitors [7]. Fig. 2 compares the ripple voltage that occurred when electromagnetic noise was injected on the substrate of the three ICs. The IC with on-chip decoupling capacitors (RC core) showed the highest immunity. In this paper, the effectiveness of the on-chip decoupling capacitor will be analyzed in detail by comparing the real injected power developed in this work for I/O buffers with and without decoupling capacitors. The real injected power to the IC is extracted using power transfer efficiency from the forward power data, which is measured at the failure of the IC operation.

Section II describes the BCI test setup and the equivalent circuit model construction for power transfer efficiency calculation. In Section III, the analytic formula for the power transfer efficiency of the BCI test is derived and the accuracy of this model is verified with a circuit simulator. Using these power transfer efficiency results, Section IV presents the BCI test results based on the forward power and the real injected power to the IC. The I/O buffer immunity is compared for the test cases with and without on-chip decoupling capacitors. Finally, conclusions are given in Section V.

II. Bulk Current Injection Test Setup

1. Experimental Setup

The experimental setup for the BCI test is based on the IEC 62132-3 standard [4], and the test equipments are shown in Fig. 3. Basically, BCI noise is injected into the power line of the I/O buffer (VDDN). In the IC, there are other circuits, such as the clock tree, buffer output switching circuit, on-chip sensing circuit, which can be sensitive to power supply noise. Therefore, another power supply is used to separate ideal power (VDD) from noisy power (VDDN). The RF disturbance from the RF generator is coupled with the power line of the I/O buffer through the BCI probe. LISN blocks the BCI

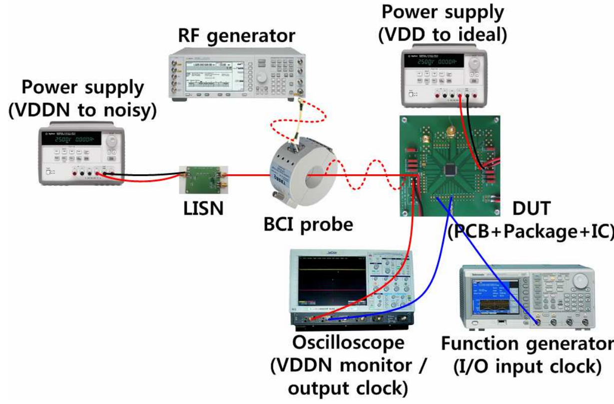


Fig. 3. The components of the BCI test.

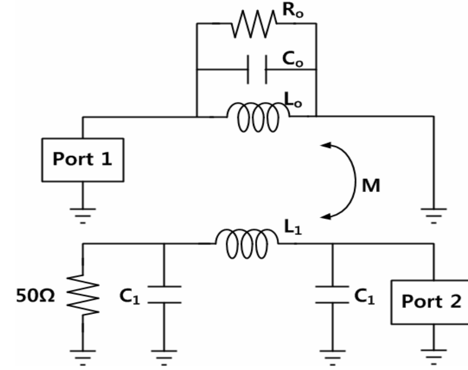


Fig. 4. The equivalent circuit model for the BCI probe [8].

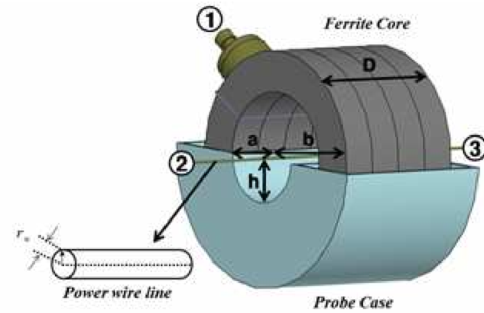


Fig. 5. Model parameters of BCI probe [8].

current from damaging the DC power supply. An input clock generated from the function generator activates the I/O buffer to switch on and off. Using the oscilloscope, the fluctuation of the VDDN and the output clock of the I/O buffer can be monitored.

2. Equivalent Circuit Modeling for Simulation

A. BCI probe modeling

An equivalent circuit model for the BCI probe can be composed as shown in Fig. 4. It is based on S-parameters in the frequency range of the BCI test and the probe geometry [8].

When the RF generator supplies forward power to port 1, a magnetic field is generated around the BCI probe, which then causes the induction current onto the cable in the center of the probe. The model parameters of the BCI are shown in Fig. 5. Self-inductance (L_o) of the BCI probe can be derived by (1) [9].

$$L_o = \frac{\mu_o \mu_r \cdot Dn^2}{2\pi} \ln\left(\frac{b}{a}\right) \; [H] \tag{1}$$

In Eq. (1), D is the width of the ferrite core, n is the rotation number of the ferrite core, and a and b are the inner and the outer radii, respectively. Eq. (2) derives the self-inductance (L_1) and capacitance (C_1) of the cable that passes through the center of the BCI probe.

$$L_1 = \frac{\mu_o}{2\pi}\left[\ln\left(\frac{2h}{r_w}\right)\right] \; [H/m] \tag{2}$$

$$C_1 \cong \frac{2\pi\epsilon_o}{\ln\left(\frac{2h}{r_w}\right)} \; [C/m]$$

where r_w is the radius of the cable, and h is the distance between the cable and the inner plane of the probe.

$$Z_{11}(\omega) = \frac{j\omega R_o L_T}{j\omega L_T + R_o - \omega^2 C_o R_o L_T} \tag{3}$$

$$\left(L_T = L_o + \frac{M^2}{L_1 + 2C_1},\; M = k\sqrt{L_o L_1}\right)$$

$$\omega_o = \frac{1}{\sqrt{L_T C_o}} \tag{4}$$

$$C_o = \frac{1}{\omega_o^2 L_T} \tag{5}$$

From the equivalent circuit model of the BCI probe, the input impedance at port 1, Z_{11}, is derived as (3). From Eq. (3), the anti-resonance frequency, ω_o, which maximizes Z_{11}, is expressed as Eq. (4). From the vector network analyzer measured Z_{11}, ω_o can be obtained. Using this frequency, the capacitance of the BCI probe can be determined from (5). Additionally, at the anti-

resonance frequency, the input impedance $Z_{11}(\omega_o)$ becomes R_o, so the resistance of the BCI probe is also obtained.

B. LISN modeling

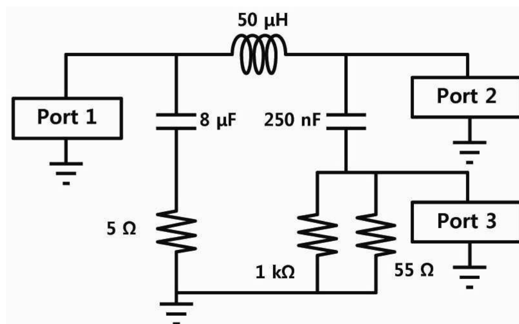
When the RF current induced by the BCI probe is injected to the device under test (DUT), this RF current may flow reversely in the power supply because of the impedance mismatch between the cable and PCB, the PCB and package, or the package and the IC chip. To prevent the RF current from damaging the power supply, an LISN is connected to the DC supply. The equivalent circuit model of LISN is shown in Fig. 6.

C. PCB modeling

The RF current induced by the BCI probe is injected to the IC through the PCB trace and the package. The four-layer PCB is designed for the BCI test, as shown in Fig. 7. The supply voltage of the I/O buffer with RF disturbance is injected to port 1, and is then transferred to port 2, the package pin, through the PCB trace. Port 3, which is connected to an oscilloscope, can monitor the supply voltage fluctuations caused by the transferred RF power.

The four-layer PCB consists of TOP, GND, PWR and BOTTOM layers as shown in Fig. 8. Noisy VDD (VDDN) is supplied to the package pin through the trace of the TOP plane. Ideal VDD which is supply voltage without the RF disturbance and VSS are evenly distributed to the PWR and GND layers, and they can be supplied to the chip through via.

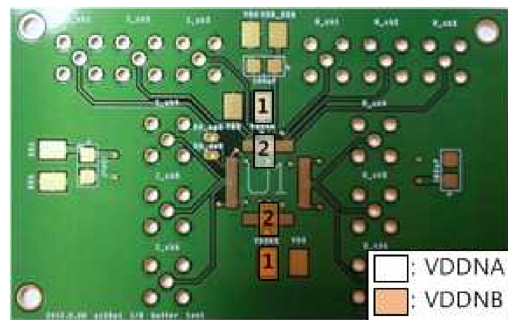
With the layer information, such as the thickness and material, the PCB can be modeled by using the CST, 3-D EM field simulator, as shown in Fig. 9 [10]. By setting the ports as shown in Fig. 7, the S-parameters can be obtained, and the equivalent circuit model is derived based on the S-parameters. A base frequency of 10 MHz is chosen to derive an accurate fitting model in the frequency range of the BCI test. Fig. 10 shows the equivalent circuit model of the PCB trace between port 1 (PAD) and port 2 (PKG pin),–and. Fig. 11 shows the comparison of the S_{21}'s obtained from the equivalent circuit model and the CST simulation at different frequencies. The equivalent circuit models for other PCB traces located between port2 and port3 to monitor injected noise shown in Fig. 7 are extracted using the same method.



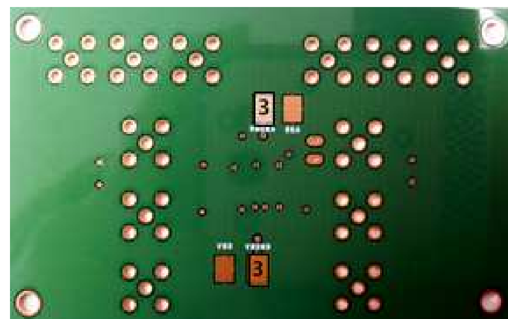
(a)

(b)

Fig. 6. Equivalent circuit model and the picture of LISN (a) the equivalent circuit model of LISN, (b) LISN implemented on PCB.



(a)



(b)

Fig. 7. The implemented PCB for BCI immunity test of the I/O buffer (a) TOP layer, (b) BOTTOM layer.

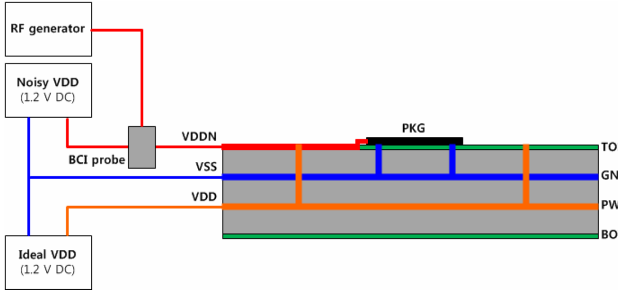


Fig. 8. The composition of four-layer PCB and the voltage transfer path.

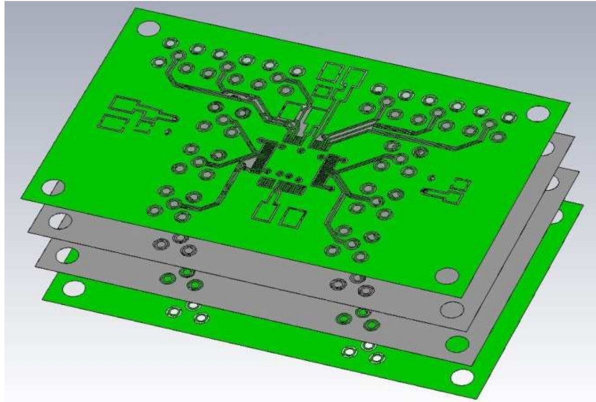


Fig. 9. The modeled PCB in the 3-D EM field simulator.

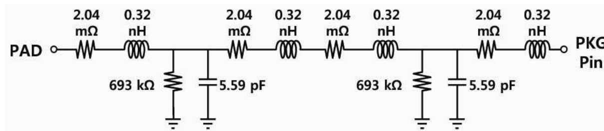


Fig. 10. The equivalent circuit model for PCB trace.

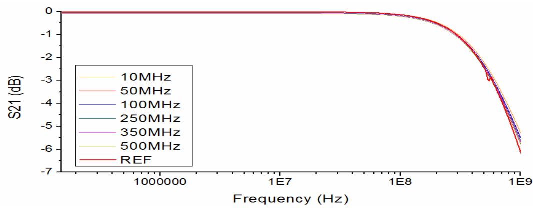


Fig. 11. Comparison of the equivalent circuit model of the VDDNA node and the CST simulation as the base frequency is swept.

D. Package modeling

In this paper, the type of package used is 80-pin TQFP (Thin Quad Flat Package). For more accurate modeling, an X-ray picture of the package was taken, as shown in Fig. 12. The induced RF current is injected into one of the two supply voltages as highlighted in Fig. 12: VDDNA, which is the noisy VDD and connected to the

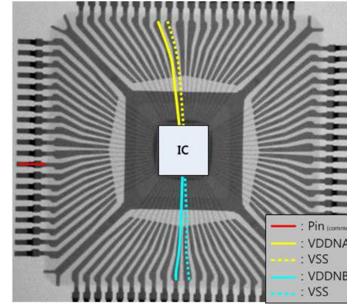


Fig. 12. X-ray of 80-pin TQFP.

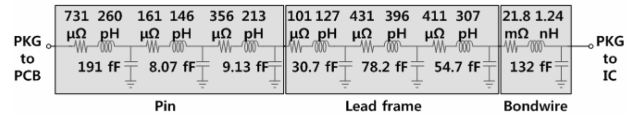


Fig. 13. The equivalent circuit model for 80-pin TQFP.

I/O buffer without on-chip decoupling capacitors, or VDDNB. which is the noisy VDD of the I/O buffer with on-chip decoupling capacitors. Each injection path is divided into pin, lead frame, and bond wire. And each part is divided in detail to approximate it as a rectangular conductor. As shown in Fig. 13, the equivalent circuit model is obtained using (8) derived from [11]. In the equations, w is the width, t is the thickness, l is the length, and h is the height of the conductor.

$$R=\rho\frac{l}{w\bullet t} \tag{8}$$

$$L=\frac{\mu_o l}{2\pi}\left[\ln\left(\frac{8h}{w+t}+1\right)\right]$$

$$C=\epsilon_o\epsilon_r l\left[1.13\left(\frac{w}{h}\right)+1.44\left(\frac{w}{h}\right)^{0.11}+1.46\left(\frac{t}{h}\right)^{0.42}\right]$$

E. IC impedance extraction

The electromagnetic wave generated by the RF generator is injected to the IC through the BCI test equipment, PCB, and package. In this injection process, there is a reflection wave because of the impedance mismatch between the IC and the RF injection path. Because not only the transfer characteristic of the RF injection path but also the reflection coefficient determines the real injected power to the IC, the IC impedance is a vital factor for extracting the power transfer efficiency. A layout photo of the IC for the BCI test is shown in Fig. 14. In the IC, I/O buffers with decoupling capacitors are connected to the VDDNA, and

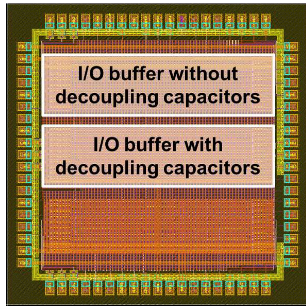


Fig. 14. The layout of IC for BCI test.

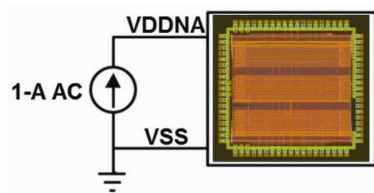
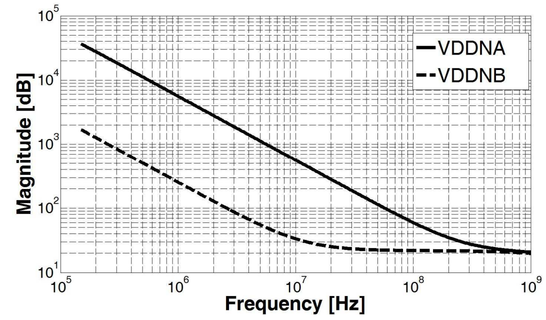


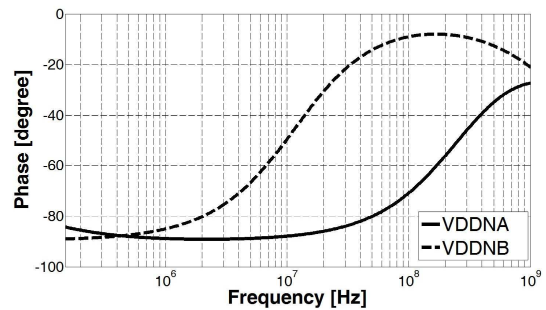
Fig. 15. The method of extracting chip impedance with 1-A AC current.

those without decoupling capacitors connected to the VDDNB. The capacitance of the decoupling capacitor is 1.34 nF and the decoupling capacitors are distributed over the area of the I/O buffer with the decoupling capacitors. The parasitic RC components are added to the netlist of the IC with the Star-RCXT of Synopsys based on the layout [12].

The input impedance can be obtained from the node voltage when the 1-A AC current is injected to the node of interest. Fig. 16 shows the input impedance obtained at the VDDNA and VDDNB power pins.

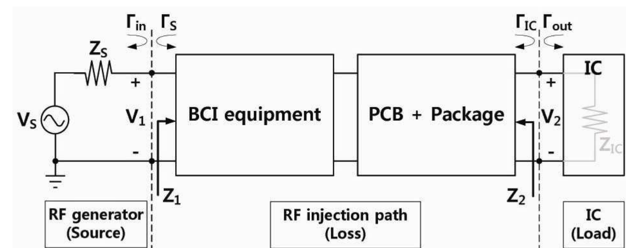


(a)

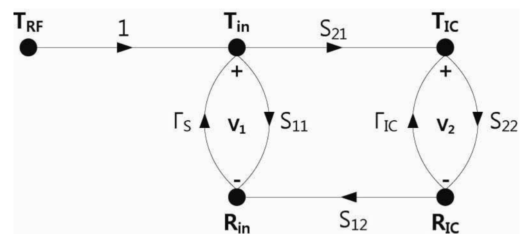


(b)

Fig. 16. The simulated IC input impedance at VDDNA and VDDNB (a) Magnitude, (b) Phase.



(a)



(b)

Fig. 17. (a) The 2-port circuit network diagram of the BCI test, (b) the flow of RF power with the scattering parameters and the reflection coefficient.

III. POWER TRANSFER EFFICIENCY DERIVATION

Using the equivalent circuit models obtained in the preceding section, the two-port network in Fig. 17(a) can be found. While the power gain is generally used for the two-port network, in this paper, the power transfer efficiency is used instead. The power gain is the ratio of the power entering into a two-port network to the real power injected into the IC. On the other hand, the power transfer efficiency is defined as the ratio of the power measured at the RF generator to the real injected power estimated at the input of IC. Whereas the results of the EMS test are usually reported by the external forward power from the RF generator in the traditional BCI method, the immunity of the IC itself should be indicated by the real injected power at the input of the IC. The power transfer efficiency (H_p) is defined as below.

$$H_P = \frac{P_{IC}}{P_{RF}} \tag{9}$$

where P_{RF} is the power transmitted to the load when the load impedance is matched, and P_{IC} is the real power injected to the test IC. Fig. 17(b) shows the flow of RF power. T_x and R_x are the incident power and the reflected power, respectively, at a certain node x. T_{RF} describes the forward power of the RF generator, P_{RF}. The sum of T_{IC} and R_{IC} represents the real power injected into the IC, P_{IC}. These S-parameters are obtained by terminating both ends of the RF injection path with characteristic impedance Z_o, which is 50 Ω.

First, the forward power reported from the RF generator is the power transmitted to the load when the load impedance is matched with Z_S, the source impedance of the RF generator. Therefore, P_{RF} is expressed as the following

$$P_{RF} = \frac{1}{2}\frac{\left(\frac{1}{2}V_S\right)^2}{R_S} = \frac{1}{8}\frac{V_S{}^2}{R_S} \tag{10}$$

Using the definition of the scattering parameters and Γ_{IC}, the reflection coefficient at the IC, the input voltage waveforms are

$$V_1{}^- = S_{11}V_1{}^+ + S_{12}V_2{}^+ = S_{11}V_1{}^+ + S_{12}\Gamma_{IC}V_2{}^- \tag{11}$$
$$V_2{}^- = S_{21}V_1{}^+ + S_{22}V_2{}^+ = S_{21}V_1{}^+ + S_{22}\Gamma_{IC}V_2{}^- \tag{12}$$

By arranging (12) in terms of V_2^- and substituting it into (11), we obtain the following equation for Γ_{in}.

$$\Gamma_{in} = \frac{V_1{}^-}{V_1{}^+} = S_{11} + \frac{S_{12}S_{21}\Gamma_{IC}}{1 - S_{22}\Gamma_{IC}} \tag{13}$$

Similarly, the equation for Γ_{out} is also deduced.

$$\Gamma_{out} = \frac{V_2{}^-}{V_2{}^+} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{14}$$

Γ_{in} is shown in terms of Z_1 and Z_o as below.

$$\Gamma_{in} = \frac{Z_1 - Z_o}{Z_1 + Z_o} \tag{15}$$

Using (13) and (15),

$$Z_1 = Z_o\frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} \tag{16}$$

V_1 is obtained by scaling V_S depending on Z_S and Z_1.

$$V_1 = V_S\frac{Z_1}{Z_S + Z_1} = V_1{}^+ + V_1{}^- = V_1{}^+(1 + \Gamma_{in}) \tag{17}$$

Substituting (16) into (17) and arranging (17) in terms of V_1^+,

$$V_1{}^+ = \frac{V_S}{2}\frac{1 - \Gamma_S}{1 - \Gamma_S\Gamma_{in}} \tag{18}$$

the relationship between V_1^+ and V_2^- is derived from (12).

$$V_2{}^- = \frac{S_{21}}{1 - S_{22}\Gamma_{IC}}V_1{}^+ = \frac{V_S}{2}\frac{1 - \Gamma_S}{1 - \Gamma_S\Gamma_{in}}\frac{S_{21}}{1 - S_{22}\Gamma_{IC}} \tag{19}$$

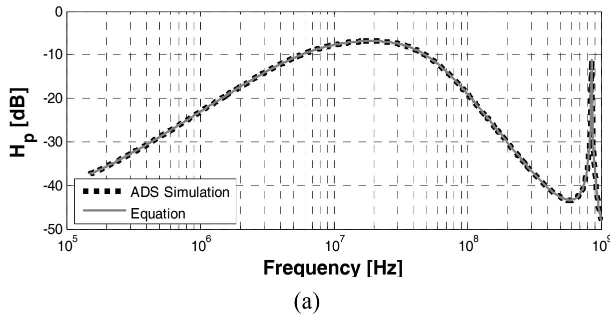
The power transferred to the load is

$$\begin{aligned} P_L &= \frac{1}{2Z_o}|V_2{}^-|^2(1 - |\Gamma_L|^2) \\ &= \frac{|V_S|^2}{8Z_o}\frac{|1 - \Gamma_S|^2}{|1 - \Gamma_S\Gamma_{in}|^2}\frac{|S_{21}|^2}{|1 - S_{22}\Gamma_L|^2}(1 - |\Gamma_L|^2) \end{aligned} \tag{20}$$

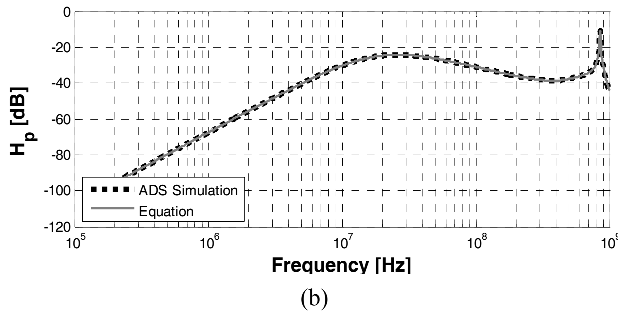
Finally, by substituting (10) and (20) into (9), the equation of the power transfer efficiency is derived as follows.

$$H_P = \frac{R_S}{Z_o}\frac{|1 - \Gamma_S|^2}{|1 - \Gamma_S\Gamma_{in}|^2}\frac{|S_{21}|^2}{|1 - S_{22}\Gamma_L|^2}(1 - |\Gamma_L|^2) \tag{21}$$

To verify the proposed formula, the equivalent circuit model is simulated using Advanced Design System (ADS), and the transferred power is measured at the load input [13]. The power directly before the load is measured when the RF generator is set to generate 0 dBm power to obtain the power transfer efficiency. Two load conditions, 50-ohm load and RLC-load (R=8.7 Ω, L=1.75 nH, C=22 pF) are used for validation. As Fig. 18 shows, the results of the equation and the simulation



(a)



(b)

Fig. 18. The comparison between simulation results and the equation (a) 50 Ω load, (b) RLC load.

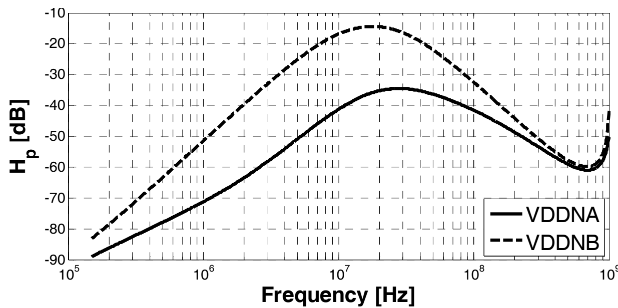


Fig. 19. The power transfer efficiency from the RF generator and the power pad of the IC.

match well.

Substituting the IC impedance obtained from Section II.2.E, into the load impedance of the equation model, the RF power injected to the power pad of I/O buffers is predicted as shown in Fig. 19. When the RF generator supplies 0 dBm power, the power measured at the power pad is the power transfer efficiency from the RF generator and the power pad of the test chip. VDDNA is the power line of the I/O buffer without on-chip decoupling capacitors, and VDDNB is the power line of the I/O buffer with on-chip decoupling capacitors. The power transfer efficiency is higher for the I/O buffer with decoupling capacitors (VDDNB), indicating that this IC is more immune to the coupled electromagnetic noise.

IV. MEASUREMENT RESULTS

The BCI test is conducted on a grounded table as shown in Fig. 20. The RF power is injected to the BCI probe and the magnetically coupled noise is combined with the 1.2 V DC supply voltage. This VDDN (noisy VDD) is used as the supply voltage to the DUT. The oscilloscope monitors the voltage fluctuation where the wire is connected to the PCB. The forward power is measured from the RF generator when the VDDN fluctuates to less than 1.1 V. This power measured from the RF power source, which we call the traditional forward power, was used as the immunity indicator in previous research [5, 6]. The same tests are constructed for two cases of the I/O buffer: one is without any decoupling capacitors (VDDNA), and the other is with decoupling capacitors (VDDNB). As defined in IEC 62132-3, the frequency range of the BCI test is from 150 kHz to 1 GHz.

Fig. 21 shows the EMS characteristic of two types of I/O buffers based on the forward power. In the traditional method of predicting immunity using forward power, it is interpreted that if the forward power is higher, the IC immunity to external EM noise is higher. However using the traditional forward power as an immunity measure of

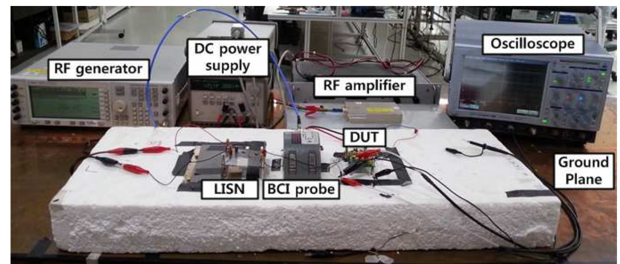


Fig. 20. The BCI test environment.

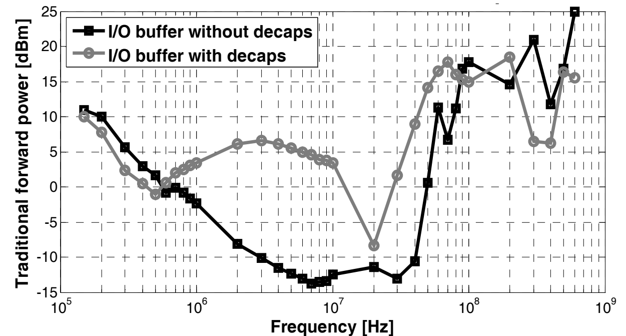


Fig. 21. The EMS characteristic of I/O buffers based on the traditional forward power.

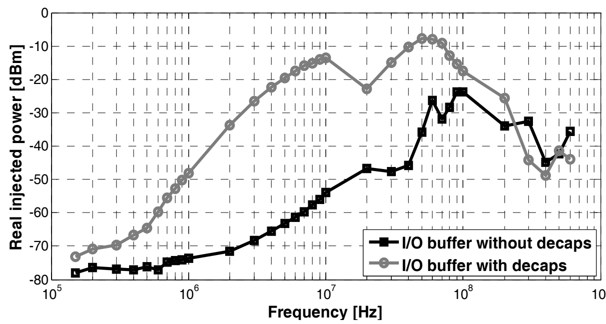


Fig. 22. The EMS characteristic of the I/O buffers based on the real injected power considering the power transfer efficiency.

the IC can be inaccurate because it does not consider the power loss of the RF injection path. Although the measured power at the RF source, the forward power, can be high, a significant portion of it can be lost in the RF injection path. The real injected power from the RF source to the IC can be found by applying the power transfer efficiency of BCI test, as shown in Fig. 19. The real injected power at the point where the IC fails can be plotted as a function of frequency, as shown in Fig. 22. The actual RF power level the IC can tolerate is much lower that what is measured at the source. In addition, the results show that the presence of the on-chip decoupling capacitor improves the IC immunity.

As shown in Figs. 19 and 22, the power transfer efficiency and the real injected power versus frequency show similar trends. When the power transfer efficiency is high, the immunity of the IC is strong. This means that the frequency range where the IC is vulnerable to EM disturbance is predominantly predicted by the power transfer efficiency. While IC immunity seems high at frequencies above 100 MHz based on the forward power prediction, it is actually low based on the estimation of real injected power. This is due to the transfer characteristic of the BCI probe [8].

The immunity evaluation based on the forward power does not indicate that on-chip decoupling capacitors inserted between power and ground nodes makes the circuit more robust against EM noise. Once the circuit immunity is predicted based on the real injected power, the I/O buffer shows higher immunity with the decoupling capacitors under 200 MHz, as shown in Fig. 22. Therefore, the amount of decoupling capacitance should be selected such that it shows high immunity characteristics in the frequency range of exposed EM noise in the system environment.

V. CONCLUSIONS

In this paper, the power transfer efficiency is proposed and can be mathematically derived from the equivalent circuit models of the BCI test setup to estimate the real injected power at the failure point of the IC operation. In the BCI test, the external RF noise passes through the BCI test equipment, such as the BCI probe and the trace the of PCB and package. The power loss of the BCI equipment depends on the frequency of the RF noise. The proposed analytical model for power transfer efficiency is validated through ADS simulation based on the equivalent circuit models for the BCI test setup. The effectiveness of the on-chip decoupling capacitor on the RF susceptibility of the I/O buffer circuit is reported based on the real injected power using BCI method. The IC immunity prediction based on traditional forward power overestimates significantly because of the transfer characteristics of the BCI probe and the noise injection paths. The experimental results indicate that the frequency range where the IC is vulnerable to EM disturbance is predominantly predicted by the power transfer efficiency. The proposed immunity evaluation based on the estimated real injected power can be applied in the IC immunity evaluation following the BCI test method from IEC 62132-3 for more accurate prediction of the EMS of the IC, and without adding the additional current measurement probe.

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