An Inductive-coupling Link with a Complementary Switching Transmitter and an Integrating Receiver

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***Abstract*—A transceiver for a high-speed inductive-coupling link is proposed. The bi-phase modulation (BPM) signaling scheme is used due to its good noise immunity. The transmitter utilizes a complementary switching method to remove glitches in transmitted data. To increase the timing margin on the receiver side, an integrating receiver with a pre-charging equalizer is employed. The proposed transceiver was implemented via a 130-nm CMOS process. The measured timing window for a 10^{-12} bit error rate (BER) at 1.8 Gb/s was 0.33 UI.**

***Index Terms*—Inductive link, Bi-phase modulation, BPM, complementary switching, integrating receiver**

I. INTRODUCTION

Printed circuit board (PCB)-based 2D systems have limitations in terms of bandwidth and power efficiency due to their long signal paths. A popular method of shortening the signal paths is stacking chips with micro-bumps or using Through-Silicon Vias (TSV). Micro-bumps connect the balls of the stacked chips in a face-to-face configuration, which makes it challenging to stack more than 3 chips. TSVs are likely more suitable for stacking a large number of chips, but their implementation is expensive due to the additional processes, reliability problems, and yield loss. On the other hand, proximity wireless communication methods such as capacitive-coupling and inductive-coupling do not suffer from problems associated with making mechanical contacts. Such schemes also have less contact-loading and allow for the minimization or removal of electro-static discharge (ESD) protection circuits. However, capacitive-coupling has several restrictions in that it cannot be used unless the chips are stacked face-to-face and it cannot provide a large transmitting power over long distances in scaled processes with low supply voltages because the signal strength is determined by the supply voltage. In contrast, inductive-coupling is a current-driven scheme and thus, the transmit power can be increased for a long distance channel, even at low supply voltages, by increasing the current [1, 2]. In addition, the transmission gain can be enhanced by increasing the mutual inductance between two coils. However, the aforementioned solutions are not favorable because they require large power consumption or a large chip area. Furthermore, larger inductors accompany a larger parasitic capacitance and resistance, which comprises the low pass filter, thereby degrading signal transmission [2]. To overcome these limitations and accelerate the adoption of inductive-coupling links in many applications, we must refine the transmit signals and eliminate possible glitches rather than overpower the signal. For reliable signal sensing in a noisy environment, the sampling time window of conventional inductive-coupling links must also be widened. In this work, the two main signaling methods for inductive coupling links,

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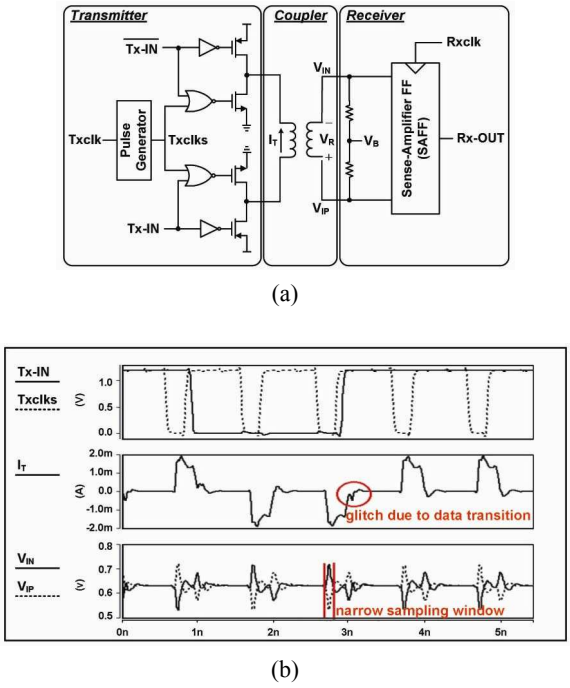


Fig. 1. Conventional BPM inductive-link (a) schematic, (b) simulated waveforms with a 1-Gb/s data rate.

non-return-to-zero (NRZ) and bi-phase modulation (BPM) signaling are reviewed in Section II. Both a transmitter structure that can improve the quality of the transmitted signal and a receiver circuit that dramatically widens the data sampling time window are then proposed. Especially, we first recognize the effectiveness of the integrating receiver [8, 9] in the BPM inductive link and successfully demonstrate its superior performance. Circuit details are discussed along with the simulation results in Section III, while the measurement results are given in Section IV. Lastly, conclusions from our work are presented in Section V.

II. INDUCTIVE-COUPLING SYSTEM WITH BPM SIGNALING

1. Conventional Inductive-Coupling Systems

In the NRZ inductive-coupling system, signal coupling occurs only when the transmit signal is in transition, i.e., rising or falling. Because there is no switching activity when identical data are transmitted, the NRZ system consumes relatively low power. However, there is a high risk of false data detection when the noise level exceeds the sensitivity of the receiver. Consequently, the NRZ system has a larger bit error rate (BER) in noisy environments [3, 4]. BPM signaling can be used to overcome some of the problems related to inductive links with NRZ signaling. Fig. 1 shows a simplified schematic and the signal waveforms of a conventional BPM inductive link. Pulse trains (*Txclks*) for the transmitter are first generated from a clock. When *Txclks* is low, I_T flows through the *Tx* inductor upward or downward depending on the polarity of the transmitted data (*Tx-IN*). The I_T pulses are then coupled to *Rx* as the voltage signal, V_R (= V_{IN}-V_{IP}). The voltage signal is ultimately sampled at the sampling window shown in Fig. 1(b) and converted to a CMOS-level signal (*Rx-OUT*) by a sense-amplifier type comparator. In contrast to the NRZ system, a voltage signal (V_R) is generated on the receiver side even when *Tx-IN* is not changed. Thus, the risk of false detection is greatly reduced. Here, the polarity of V_R is determined by *Tx-IN*. The topology in Fig. 1(a) has been successfully used for low frequencies up to 1 GHz [5, 6]. However, the operation frequency of the conventional BPM structure is limited due to a number of reasons. First, the valid sampling time window at the receiver is too narrow, as denoted in Fig. 1(b). The valid window of V_R is determined by the short duration of the I_T transition. For example, the sampling timing margin of the conventional BPM system [5, 6] in Fig. 1 is only about 0.1 UI (~100 ps) with a 1 GHz operating frequency. Second, unexpected *Tx* glitch noise limits the operating speed. I_T is not supposed to appear when *Txclks* stays high. However, glitches in I_T are observed when *Txclks* is high and *Tx-IN* is inverted. The parasitic capacitors of the inductor and switching devices at the two ends of the inductor also serve as sources and sinks of charge when *Tx_IN* is inverted, leading to the formation of an undesired path for I_T. The I_T glitch can be interpreted as inter-symbol interference and it must be resolved before the next sampling event. Otherwise, the data rate will be limited.

2. Proposed Transceiver for BPM Inductive Links

Given the narrow sampling window at the receiver, it is hard to correctly position the sampling clock edge. In addition, noise and jitter further reduce the timing margin under real operating conditions. To precisely control the

clock edge, we must increase the complexity of the circuit with feedback loops [7] and improve the resolution of the phase interpolator in the clock generator. Oversampling is another solution, but it consumes a large amount of power and circuit area and it may not work with such a narrow timing window. Instead of refining the sampling clock and precisely positioning its edge, widening the sampling widow can be viewed as a much easier option. To expand the timing window of BPM inductive links, we adopted the integrating receiver structure [8, 9] shown in Fig. 2. In the proposed receiver, an integrator is inserted between the front-end receiver (pre-amplifier) and the sampler. A simplified schematic of the integrator and the conceptual waveforms are displayed in Figs. 2(b) and (c). When *Rxclk* is low, the coupled data, $V_{IN\_N/P}$, and integrator input data, $V_{AMP-OUTN/P}$, are not valid, and then the two capacitors, *C*, are pre-charged to the same level. However, when *Rxclk* is high, the pre-charging switches are opened. The current, *I*, is then directed by $V_{IN-N/P}$ and the voltage difference between V_{ITG_OUTP} and V_{ITG_OUTN} represents the integration of 'V_{IN-P}-V_{IN-N}'. Finally, the sampler samples and holds the output of the integrator. As shown in Fig. 2(c), the sampling timing margin with the integrator can be increased significantly when compared to that in the case without an integrator.

It is relatively simple to eliminate I_T glitches from *Tx*. By gating *Tx_IN* with *Txclks* for both the NMOS and PMOS transistors in the driver, we can reduce I_T glitches caused by *Tx_IN* transitions. We can further refine the I_T waveforms by providing additional DC paths when all switches are turned off. In the next section, details regarding the circuit of the proposed receiver and transmitter will be provided after the overall transceiver architecture is described.

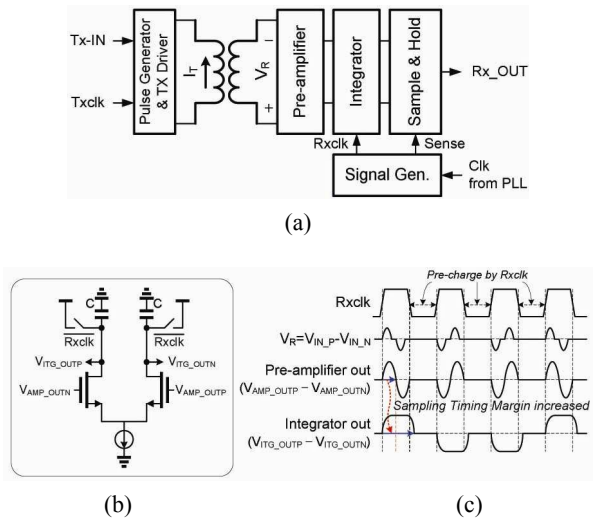


Fig. 2. Inductive link with an integrating receiver (a) block diagram of the link, (b) the simplified integrator, (c) conceptualized operation of the integrator.

III. CIRCUIT IMPLEMENTATION

1. Transceiver Architecture

Fig. 3 shows the test system with the proposed 1.8-Gb/s inductive link, which consists of *Tx*, *Rx*, and two identical inductors. Each inductor has a 6.3-nH inductance and occupies an area of 390x390 μm2. In *Tx*, the internal phase-locked loop (PLL) provides 1.8-GHz 4-phase clocks (0°, 90°, 180, and 270°). Parallel random data from the pseudo random binary sequence (PRBS) generator are serialized to 1.8-Gb/s serial data by the 16:1 serializer and synchronized with the 0° PLL output clock. The BPM pulse generator produces a short pulse train (*Txclks*) using the multi-phase clocks, and converts the serialized data to complimentary signals (*Tx_IN* and *Tx_INb*). In the *Tx* driver, *Tx_IN* and *Tx_INb* are gated by *Txclks* and inject bi-phase current pulses (I_T) into the inductor. I_T transitions are coupled to the inductor on the *Rx* side, and induce V_R at the receiver input. The pre-driver then amplifies V_R and passes it to the integrator. As described in Section II, the integrator expands the valid time window for the subsequent sampler. Finally, the sampler recovers the signal to the CMOS level. Operation timings of the integrator and sampler are controlled by the retimed clocks from the sensing signal generator.

Assuming that the *Tx* and *Rx* will eventually be integrated in a package, a common reference clock is routed to both *Tx* and *Rx* in the test system. The optimum phase of the sampling clock (*Sense*) can be determined by the phase adjustment block at initialization [9]. In the calibration mode, the transmitter sends deterministic test patterns from the PRBS generator over the data link. The received signals are then sampled by the clock of which the phase is tuned by the phase interpolator. The sampled data are deserialized and compared with the pre-determined PRBS data. Changing the phase interpolator setting and monitoring the number of errors from the

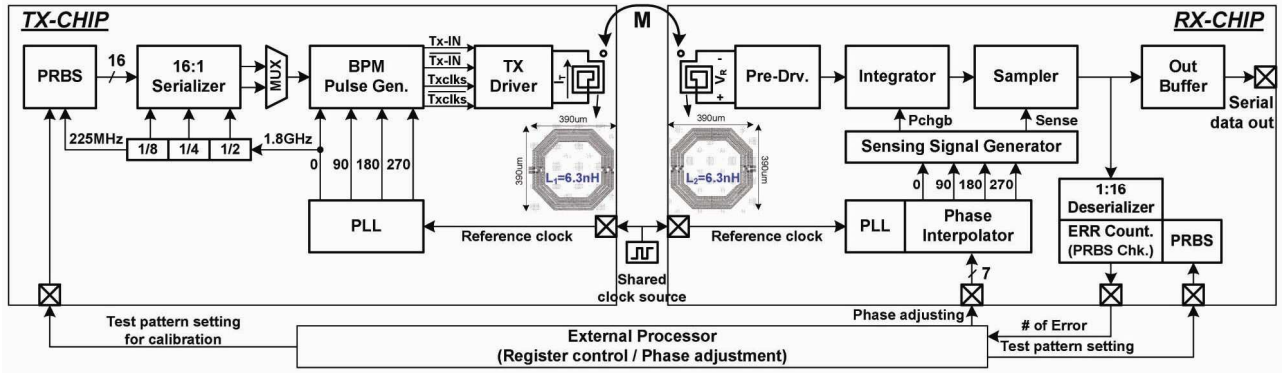
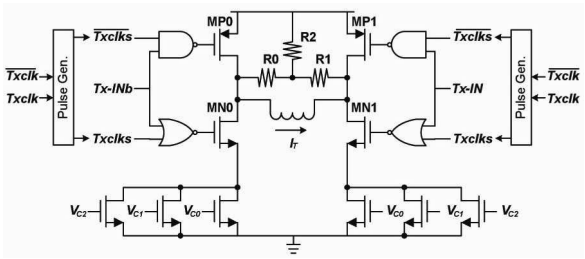


Fig. 3. Implemented inductive link block diagram.

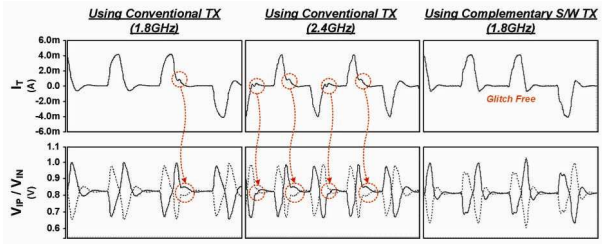
PRBS checker, the left and right edges of the timing window are determined. Finally, the Phase Interpolator (PI) setting is adjusted so that the sampling clock edge is located at the center of the timing window. For the characterization purpose, the phase interpolator setting can also be controlled by the external registers.

2. Complementary Switching Tx

Fig. 4(a) shows a schematic of the complementary switching *Tx* driver modified from the conventional BPM driver in Fig. 1(a). Here, *Txclks* is a 1.8-GHz clock with a 75% duty-cycle ratio. That is, it stays high between 0° and 270°, and goes low between 270° and 360°. *Tx-IN* and *Tx-INb* are passed to the gates of the PMOS and NMOS transistors and the I_T current path is formed through the inductor only when *Txclks* is low. Because the inputs for the PMOS switches (MP0 and MP1) are gated by *Txclksb*, glitches due to *Tx-IN/b* transitions do not appear in the proposed structure. As shown in Fig. 4(b), glitches associated with the conventional driver are transmitted to the input of the receiver (V_{IP}/V_{IN}) and then amplified by the pre-driver. With a relatively low data rate (e.g., 1.8 Gb/s), the impact of this glitch can be resolved before the next bit arrives at the receiver. However, as the data rate increases, the timing margin before the next bit decreases as shown in Fig. 4(b). On the other hand, the proposed complementary switching *Tx* is glitch-free and thus, inter-symbol interference (ISI) due to the glitch is not observed. In the conventional driver, the inductor nodes become floating when both the PMOS and NMOS switches are turned off. To prevent noise coupling through the inductor during this floating period, three additional resistors (*R0, R1*, and *R2*)



(a)



(b)

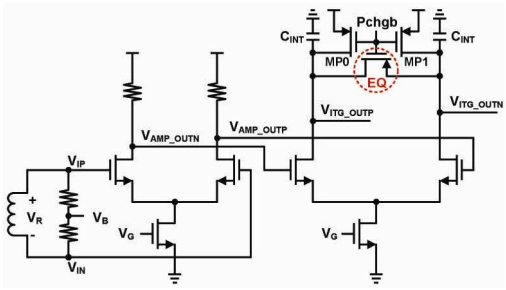
Fig. 4. Proposed complementary switching transmitter (a) schematic, (b) simulation with a conventional TX.

provide DC paths from the inductor to the power supply. In addition, the added resistors reduce the Q-factor of the LC tank which consists of an inductor and parasitic capacitors at its ports. The resistance values are determined as follows. The resistance must be large enough so as not to steal current from the inductor. However, an excessively large resistance leads to a Q-factor that is undesirably high, resulting in underdamped transient responses and I_T ringing behavior. In the implemented structure, the *R0* and *R1* values were determined as 5.3 kΩ. With this value, IT itself is slightly underdamped, but compensates for the bandwidth limitation of the pre-amplifier at the receiver. By digitally controlling V_{C0}, V_{C1}, and V_{C2}, the peak value of

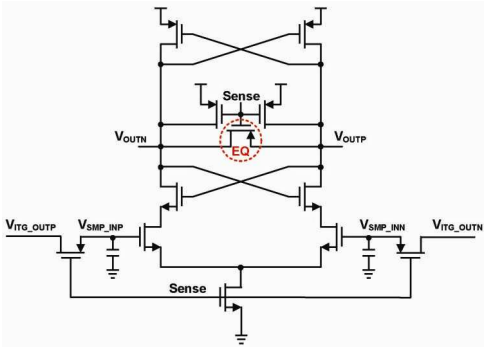
I_T can be adjusted from 2 mA to 4, 6, 8, 10, and 12 mA according to the communication distance.

3. Integrating Rx

Figs. 5(a) and (b) show the schematics of the implemented integrating receiver, which consists of 3 stages: the pre-amplifier, the integrator, and the sampler. The signals in the *Tx* and *Rx* data paths and their timing relationships are displayed in Fig. 6. The pre-amplifier amplifies small inductively-coupled signals, $V_{IP/N}$, to the integrator inputs, $V_{AMP\_OUTP/N}$. The 3-dB bandwidth of the pre-amplifier is set close to the operating frequency of 1.8 GHz. Therefore, the pre-amplifier shows weak integrating behavior. That is, initial peaking of $V_{IP/N}$ is effectively amplified, while the subsequent invalid small ringings are attenuated. However, the pre-amplified BPM signals, $V_{AMP\_OUTP/N}$, still have very narrow sampling



(a)



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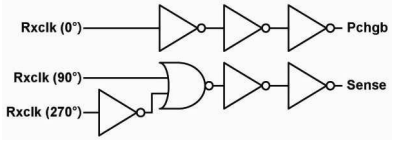


(c)

Fig. 5. Integrating receiver (a) pre-driver and integrator, (b) sense-amp type comparator, (c) sensing signal generation logic.

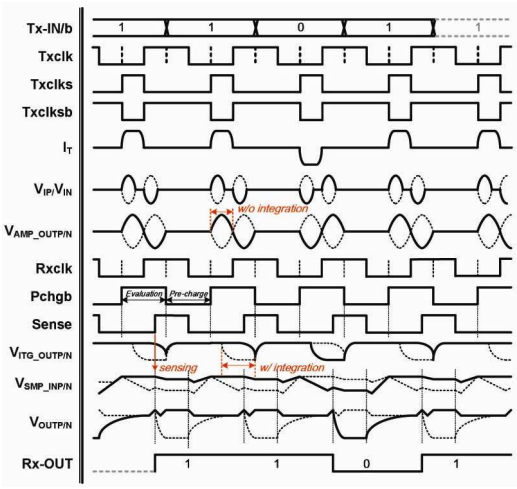
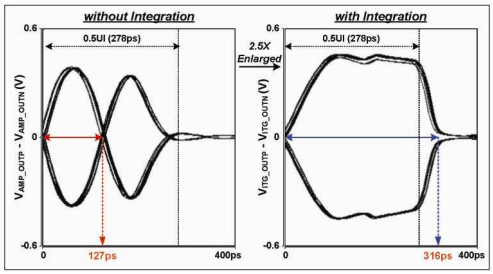


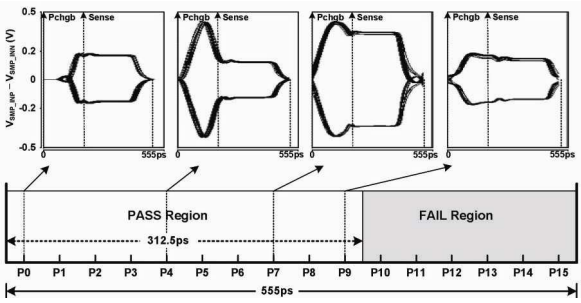
Fig. 6. Conceptualized waveforms of the proposed inductive-link system.

timing windows, as denoted in Fig. 6. The integrator stage after the pre-amplifier significantly expands the sampling timing window, as mentioned in Section II. 2. When the pre-charging signal, *Pchgb*, is low, the integrator resets the voltage across the capacitors (C_{INT}) to zero. The equalizing transistor (EQ) in the integrator is turned on as soon as *Pchgb* goes low, and it shorts the differential output nodes to expedite the pre-charging behavior. While the input data are valid, *Pchgb* becomes high and the pre-charging transistors (MP0, MP1) are turned off. At this point, the tail current is steered by 'V_{AMP_OUTN}-V_{AMP_OUTP}', and 'V_{AMP_OUTN}-V_{AMP_OUTP}' is integrated as the differential integrator output, 'V_{ITG_OUP}-V_{ITG_OUTN}'. As shown in Fig. 6, the valid timing window of 'V_{ITG_OUP}-V_{ITG_OUTN}' is significantly expanded when compared to that of 'V_{AMP_OUTN}-V_{AMP_OUTP}'. For the next sampling stage, a sense-amp-type comparator is used. The integrator outputs are sampled when the sampling clock, *Sense*, is high, and converted to CMOS level signals by the subsequent latch.

To guarantee stable operation of the comparator, the integrator outputs are held as $V_{SMP\_INP/N}$ while *Sense* is high. The sampling timing margin can be estimated from the eye diagram of 'V_{ITG_OUP}-V_{ITG_OUTN}', as shown in Fig. 7(a). The eye diagram of 'V_{ITG_OUP}-V_{ITG_OUTN}' appears wider than that of 'V_{AMP_OUTN}-V_{AMP_OUTP}'. However, this opened eye does not accurately represent the actual timing margin because *Pchgb* and the integrating window are also shifted as the sampling clock (*Sense*) edge moves. In this regard, the timing margin must be



(a)



(b)

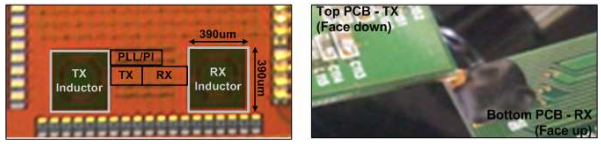
Fig. 7. (a) Comparison of sampling window, (b) Sampler sensing margin.

estimated by shifting the sampling clock. By shifting the *Rx* sampling clock with 16 steps (P0~P15 in Fig. 7(b)) in a simulation, we measured the sampling timing margin. The eye diagrams of 'V_{SMP_INP}-V_{SMP_INN}' at P0, P4, P7, and P9 are also plotted with *Pchgb* and *Sense* rising edges. The sampling timing margin of the proposed receiver was about 312.5 ps (9/16 UI at 1.8 Gb/s), which is 2.5 times wider than that in the ideal case without an integrator.

IV. MEASUREMENT

The test chip and boards shown in Fig. 8(a) was fabricated using 130-nm CMOS technology. The *Tx* and *Rx* parts were assembled on two separate PCBs by a chip-on-board process. For the link test, the *Tx* and *Rx* PCBs are facing each other, as shown in Fig. 8(b), and the two bare silicon chips are in contact with one another. The thickness of the passivation layers between the face-to-face stacked inductors is 28 um, while the relative permeability of the passivation layers is approximately 1.0. Because inductor alignment is crucial for optimum coupling performance, all tests were conducted on a probe station with tunable aligners.

The measured BER bathtub curves with 1.5-Gb/s and



(a) (b)

Fig. 8. (a) Photograph of the die, (b) link test setup.

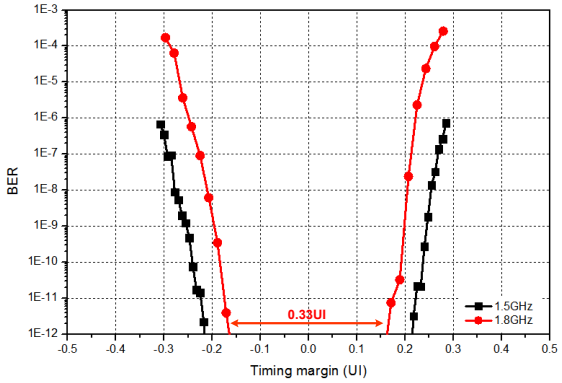
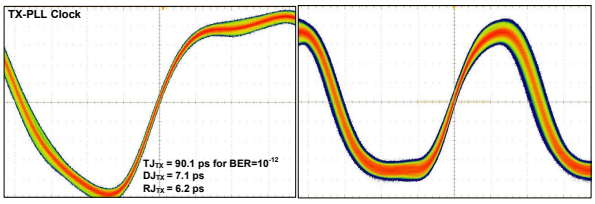


Fig. 9. Measured BER of 1.5-Gb/s and 1.8-Gb/s data rates with 2^{7-1}pattern



(a) (b)

Fig. 10. Measured jitters of (a) the Tx PLL clock, (b) the Rx PI clock.

1.8-Gb/s data rates are shown in Fig. 9. With a 2^7-1 PRBS pattern, a BER of over 10^{-12} was achieved, and the timing margin was 0.33 UI (=182 ps) at 1.8 Gb/s. To estimate the contribution of clock jitters in closing the timing margin of the link, the *Tx* and *Rx* clocks were monitored. The measured clock waveforms are shown in Fig. 10. The measured deterministic jitter (DJ) and random jitter (RJ) of the *Tx* clock (Tx PLL output) were 7.1 ps and 6.2 ps, respectively, while the Rx clock had a DJ of 18.6 ps and an RJ of 6.8 ps. The jitter of the *Rx* clock was slightly worse than that of the *Tx* clock because it goes through an additional phase interpolator. Assuming that the *Tx* and *Rx* clock jitters are uncorrelated, the calculated total jitter based on a 10^{-12} BER [9] is about 117 ps (=0.21 UI). From the simulation

Table 1. Performance Summary

	Ref. [3]	Ref. [5]	Ref. [11]	Ref. [12]	This work
Technology	0.35 um	0.18 um	0.065 um	0.13 um	0.13 um
Signaling	NRZ	BPM	4PAM*	MPM**	BPM
Data rate	1.25 Gb/s	1 Gb/s	2.5 Gb/s	1.2 Gb/s	1.8 Gb/s
Ch. Length	60 um	30 um	1 mm	1 mm	28 um
Power per lane	46 mW @3.3V	2.89 mW @1.8V	15 mW @1.2V	4.7 mW @1.2V	3.44 mW @1.3V

* PAM: Pulse Amplitude Modulation
** MPM: Mono-Phase Modulation

results in Section III.C, the sampling time margin with the ideal clocks was determined to be about 312.5 ps. Therefore, the estimated timing margin is approximately 194.5 ps (=0.35 UI for 1.8 Gb/s), which is close to the measured results in Fig. 9. The *Tx* and *Rx* consume 1.83 mW and 1.61 mW from a 1.3-V power supply, respectively. The measurement results are summarized and compared with other published findings in Table 1.

V. CONCLUSIONS

A 1.8-Gb/s BPM inductive-coupling link with a complementary switching transmitter and an integrating receiver was proposed. Instead of sampling sharp and narrow signals at the receiver input, the proposed receiver integrates the input signals and samples relatively stabilized signals, which effectively widens the sampling time window and improves the noise immunity. The complementary switching transmitter also neatly shapes the transmitted signal by removing invalid glitches. A simulation showed that the proposed transceiver enlarges the timing margin by a factor of 2.5. To demonstrate the concept of the proposed transceiver, we constructed an inductive link with test chips mounted on PCBs. The *Tx* and *Rx* chips fabricated via a 0.13-um CMOS process consumed a total power of 3.44 mW when operating at 1.8 Gb/s. The measured timing margin for a BER of 10^{-12} was 0.44 UI at 1.5 Gb/s and 0.33 UI at 1.8 Gb/s.

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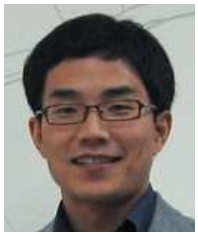

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