JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.15, NO.6, DECEMBER, 2015 ISSN(Print) 1598-1657
http://dx.doi.org/10.5573/JSTS.2015.15.6.695 ISSN(Online) 2233-4866

A 1-V 1.6-GS/s 5.58-ENOB CMOS Flash ADC using Time-Domain Comparator

Han-Yeol Lee[1], Dong-Gil Jeong[1], Yu-Jeong Hwang[1], Hyun-Bae Lee[2], and Young-Chan Jang[1]

***Abstract*—A 1-V 1.6-GS/s 5.58-ENOB flash ADC with a high-speed time-domain comparator is proposed. The proposed time-domain comparator, which consumes low power, improves the comparison capability in high-speed operations and results in the removal of preamplifiers from the first-stage of the flash ADC. The time interpolation with two factors, implemented using the proposed time-domain comparator array and SR latch array, reduces the area and power consumption. The proposed flash ADC has been implemented using a 65-nm 1-poly 8-metal CMOS process with a 1-V supply voltage. The measured DNL and INL are 0.28 and 0.41 LSB, respectively. The SNDR is measured to be 35.37 dB at the *Nyquist* frequency. The FoM and chip area of the flash ADC are 0.38 pJ/c-s and 620 × 340 μm^2, respectively.**

***Index Terms*—Flash ADC, high-speed time-domain comparator, time interpolation, low power**

I. INTRODUCTION

Attributed to their simple architecture and operation, flash analog-to-digital converters (ADCs) with a resolution of 6-7 bits and a conversion rate greater than 1 GS/s are used in multiband orthogonal frequency division multiplexing ultra-wide-band (MB-OFDM UWB) receivers and digital read channels of data storage devices [1-3]. As these flash ADCs are usually integrated on the same chip as large digital-signal processing blocks, and the supply voltage of the digital blocks is reduced to a small value by scaling, it is convenient to reduce the required supply voltage of the ADCs to the same value as the digital supply voltage. Furthermore, to reduce power consumption, it is essential to remove the analog blocks, such as source followers and preamplifiers, that consume static current in the ADCs. Generally, a flash ADC uses a source follower and preamplifier array to reduce the input capacitance and increase the voltage gain [1]. However, the area and power consumption of a flash ADC increase owing to the use of a source follower and preamplifiers that consume static current. The flash ADC reported in prior literature [2] reduced power consumption by using voltage comparators and a time-domain latch interpolation, and by removing preamplifiers altogether. However, the measured effective number of bits (ENOB) was approximately 4.89 bits at the *Nyquist* frequency despite the inclusion of an offset calibration circuit for the voltage comparator.

In this paper, a time-domain comparator is proposed for a 1.6-GS/s 6-bit flash ADC with 1-V_{PP} differential input voltage range and a 1-V supply voltage. The proposed time-domain comparator improves the operating speed with low kickback noise by the addition of two inverters and an SR latch to a conventional sense-amplifier. A source follower and preamplifiers are removed in order to decrease the power consumption of the flash ADC. Furthermore, the number of comparators used in the flash ADC is reduced by using two-factor interpolation. Section II describes the architecture of the flash ADC and the circuit of the proposed high-speed time-domain comparator. Furthermore, the proposed

Manuscript received Sep. 30, 2015; accepted Oct. 25, 2015
[1] School of Electronic Engineering, Kumoh National Institute of Technology, 61, Daehak-ro, Gumi, Gyungbuk 39177, Korea.
[2] SK Hynix Semiconductor Inc., Icheon, Gyeonggi, Korea
E-mail : ycjang@kumoh.ac.kr

time-domain comparator is analyzed by comparing it with conventional comparators. The measured results of the flash ADC are discussed in Section III. Finally, Section IV presents the conclusion of this paper.

II. ADC Architecture and Circuit Implementation

The proposed flash ADC consists of a track/hold (T/H) with a bootstrapped switch, a reference driver for 5-bit resolution, a comparator array, a digital encoder, and a clock generator, as shown in Fig. 1. The comparator array consists of 35 first-stage comparators and 69 second-stage comparators including the dummy blocks for the termination of resistor averaging network [1]. Resistor averaging is implemented by using resistors to connect the outputs of the sense-amplifier in each first-stage comparator. Further, two-factor interpolation is achieved using second-stage comparators to reduce the number of first-stage comparators [2, 3]. In the proposed flash ADC, a source follower and preamplifiers that are commonly implemented have been removed using the proposed high-speed time-domain comparator with low kickback noise. The input capacitance of the proposed flash ADC is approximately 1 pF. The holding capacitance of the track/hold and the input equivalent capacitance of the comparator array are 700 fF and 300 fF, respectively. The digital encoder generally uses flip-flop arrays to implement a pipeline scheme for high-speed operation [4]. In this work, true single-phase clocked flip-flops with a leakage current compensation circuit are used as a digital encoder [5].

1. Operation of Proposed Time-Domain Comparator

A sense-amplifier is widely used for the first-stage comparator of a voltage comparator and generally outputs the signal with a CMOS logic level by maximizing its voltage gain even though the voltage difference of two input signals (ΔV_{IN}) is small. However, the dynamic performance of a voltage comparator using a sense-amplifier can be degraded because the evaluation and precharge period for the sense-amplifier is reduced as the operation frequency of a voltage comparator increases. Furthermore, a sense-amplifier with a large voltage gain can generate a large kickback noise and increase the precharge period required for the next evaluation.

The proposed time-domain comparator improves the comparison capability for a small ΔV_{IN} in a high-speed operation. It consists of a sense-amplifier and two inverters for the first-stage comparator, and an SR latch for the second-stage comparator, as shown in Fig. 2(a). Following the precharge period of the first-stage comparator, the sense-amplifier with a fully differential

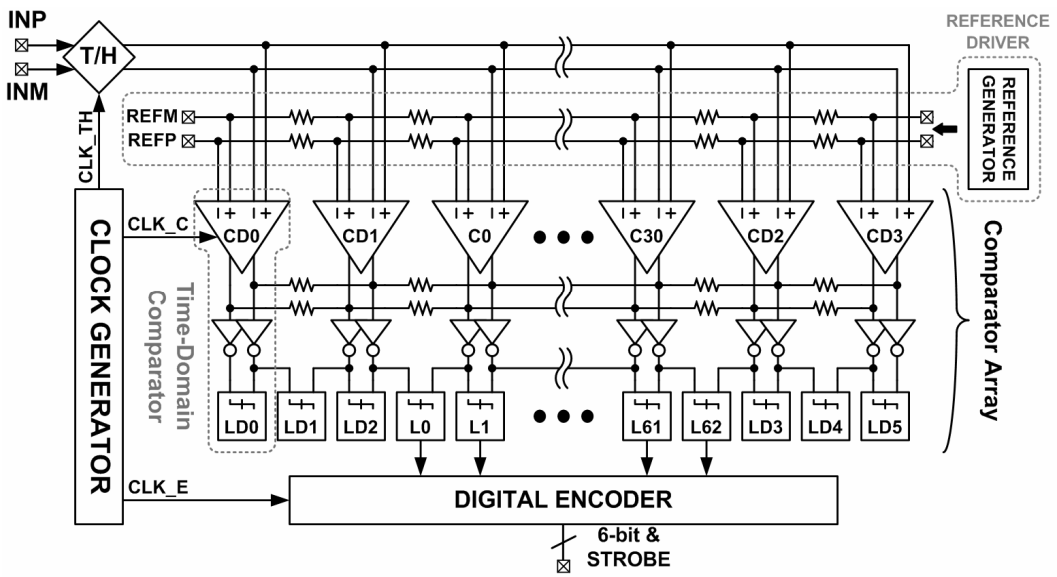


Fig. 1. Block diagram of proposed flash ADC.

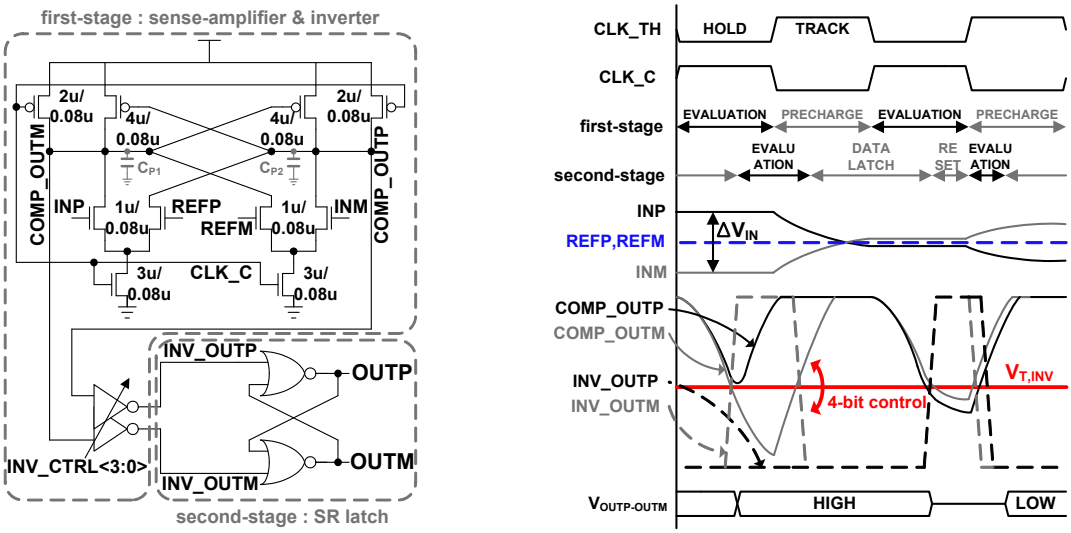


Fig. 2. Proposed time-domain comparator (a) circuit diagram, (b) timing diagram.

architecture evaluates the voltage level of the input analog signal compared to that of the reference voltage. When ΔV_{IN} is large, the sense-amplifier of the first-stage comparator outputs the signal with a CMOS logic level, and the proposed comparator operates as a conventional voltage comparator. When ΔV_{IN} is small, the functionality of the proposed comparator changes as the SR latch compares the time difference generated in the process of comparison, during which two outputs of the sense-amplifier are precharged to the voltage level of V_{DD}, as shown in Fig. 2(b). First of all, for the time-domain operation of the proposed comparator, the voltage gain of the first-stage comparator is designed to be smaller than that of conventional voltage comparator by using small-sized input transistors. It results in reducing the kickback noise caused by the proposed time-domain comparator. Furthermore, the precharging time for the sense-amplifier of the proposed comparator can be reduced because the sense-amplifier produces output signals with a small swing instead of a CMOS logic level during the evaluation period in the high-speed operation, as shown in Fig. 2(b). Secondly, two logic threshold voltage ($V_{T,INV}$) controllable inverters are added in the first-stage comparator for the time-domain operation of the proposed comparator.

As shown in Fig. 2(b), the SR latch of the second-stage comparator can compare small time differences if at least one of two signals, *COMP_OUTP* and *COMP_OUTM*, is maintained at a lower voltage level than $V_{T,INV}$ of the two inverters during the evaluation period. Thus, $V_{T,INV}$ of the two inverters is controlled by a 4-bit digital code for the small time-difference detection of the SR latch despite the process, voltage, temperature variations and change of the operation frequency. Furthermore, the two inverters remove the input load mismatch of the SR latch. During the time-domain operation, the proposed comparator with a small voltage gain for the first stage effectively uses a small portion of the precharge period as the time evaluation period by using two logic threshold voltage controllable inverters added in the first-stage comparator.

Fig. 3 is the circuit diagram of the logic threshold controllable inverter used in the first-stage comparator. A digital code, *INV_CTRL[3:0]*, controls $V_{T,INV}$ of the two inverters by changing the total width of the activated PMOSFET and NMOSFET. Fig. 4 shows the minimum ΔV_{IN} ($\Delta V_{IN,MIN}$) of the proposed comparator required for the high-speed operation at an frequency from 1.2 GHz to 2.0 GHz according to $V_{T,INV}$ of the two inverters. As ΔV_{IN} gets smaller, a higher $V_{T,INV}$ is required for high-speed operation of the proposed time-domain comparator because at least one of two signals, *COMP_OUTP* and *COMP_OUTM*, has to be at a lower voltage level than $V_{T,INV}$ of the two inverters during the evaluation period. Furthermore, the optimum $V_{T,INV}$ increases because the evaluation period of the sense-amplifier, the first-stage comparator of the proposed time-domain comparator, is reduced as the operation frequency increases. From the

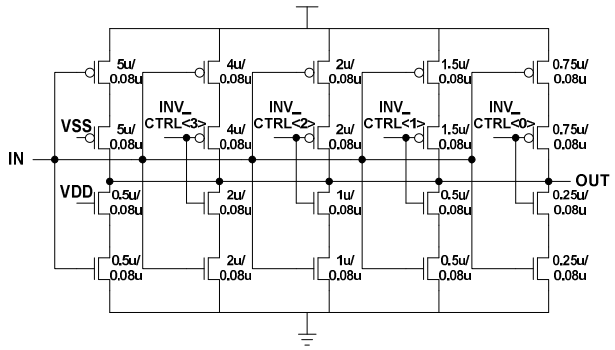


Fig. 3. Circuit diagram of logic threshold voltage controllable inverter.

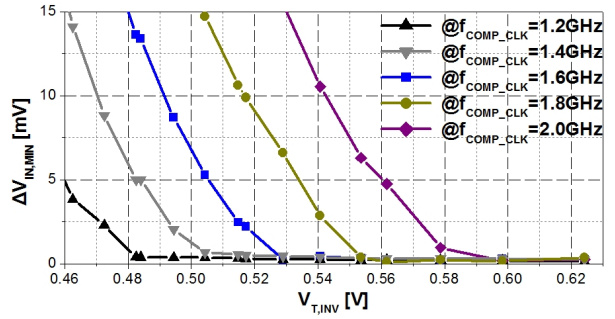


Fig. 4. Minimum sensing voltage of proposed comparator according to logic threshold voltage of two inverters.

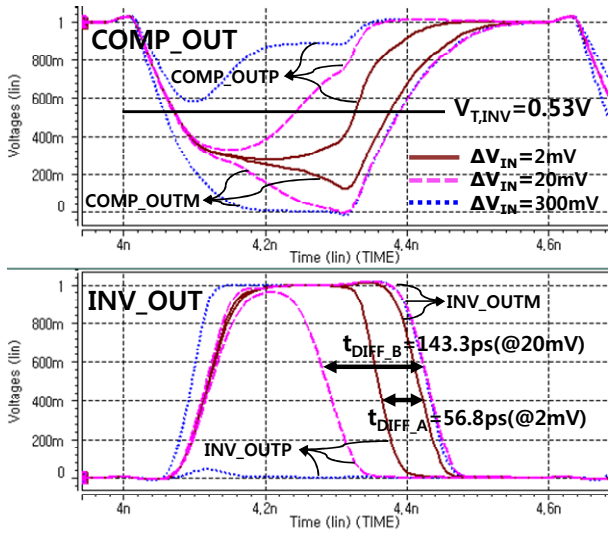


Fig. 5. Simulation results for operation of first-stage comparator.

simulation results of Fig. 4, $V_{T,INV}$ of the two inverters is set to be higher than 0.53 V for time-domain operation of the proposed comparator at an operation frequency of 1.6 GHz in this work. Fig. 5 shows the simulation results for the operation of the first-stage comparator of the proposed time-domain comparator according to ΔV_{IN}; this is performed at the operation frequency of 1.6 GHz. The proposed time-domain comparator operates as a general voltage comparator when ΔV_{IN} is 300 mV. However, the proposed comparator operates as a time-domain comparator using the time difference (t_{DIFF_A}) generated in the precharging process when ΔV_{IN} is at small values such as 2 mV and 20 mV. In this case, $V_{T,INV}$ of the two inverters is set to be 0.53 V, which is higher than the voltage of two signals, *COMP_OUTP* and *COMP_OUTM*, during the evaluation period at a sampling rate of 1.6 GS/s. The total capacitances of nodes *COMP_OUTP* and *COMP_OUTM* of the first-stage comparator have an effect on the time difference generating operation in the proposed comparator. The total capacitance of each node, including the input load capacitance of the following inverter, is approximately 35 fF.

2. Performance of Proposed Time-Domain Comparator

To analyze the performance of the proposed time-domain comparator, the proposed time-domain comparator is compared with two conventional comparators. Fig. 6 shows the circuits for the first-stage of two conventional comparators. The architecture of the first conventional comparator shown in Fig. 6(a) has a dynamic comparator that uses a preamplifier [1]. The preamplifier enhances the voltage gain in a high-speed operation and reduces the kickback noise. The second conventional comparator depicted in Fig. 6(b) is based on a sense-amplifier [3, 6, 7]. The preamplifier in this comparator has been removed to decrease power consumption. Fig. 7 shows the simulated minimum clock period ($T_{CLK,MIN}$) required for high-speed operation of each comparator versus ΔV_{IN} to verify the dynamic performance of the proposed time-domain comparator. In this simulation, one of two input stages is removed from the first-stage comparator so that the proposed time-domain comparator is operated as a comparator with two input signals.

Three comparators use the second-stage comparator shown in Fig. 2(a), and the power consumption of each comparator is 100 μW. According to the simulation results of Fig. 7, the proposed time-domain comparator requires a clock period of 478.5 ps to compare the voltage difference of 1 mV and can compare a voltage difference of 0.2 mV with a clock period of 625 ps.

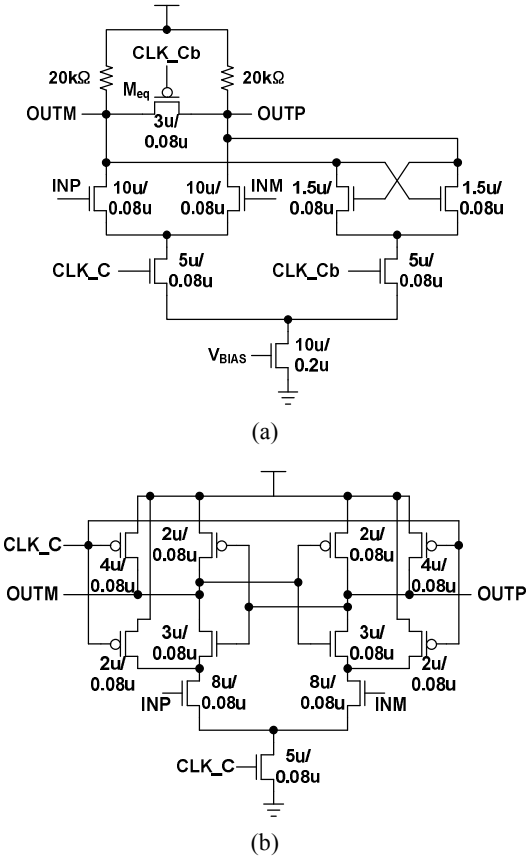


Fig. 6. Circuit diagrams of conventional comparators (a) dynamic comparator with preamplifier, (b) sense-amplifier based comparator.

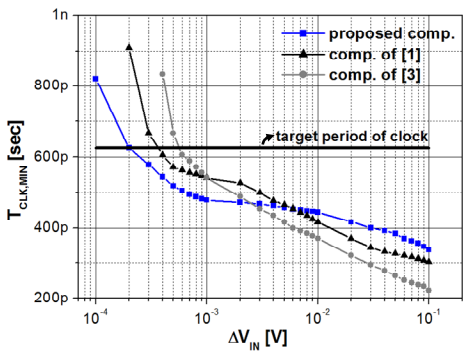
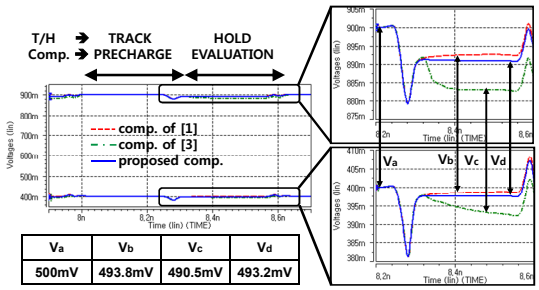


Fig. 7. Minimum period of comparator clock according to input voltage difference of comparator.

Because the first-stage comparator of the proposed time-domain comparator converts the small voltage difference to the time difference during an evaluation period, the analog noise such as charge injection and kickback noise should be minimized. The proposed time-domain comparator reduces kickback noise by using small-sized input transistors for the sense-amplifier of the first-stage comparator, as shown in Fig. 2(a). Fig. 8



Va	Vb	Vc	Vd
500mV	493.8mV	490.5mV	493.2mV

Fig. 8. Simulation results for kickback noise of comparator.

shows the simulation results for the kickback noise of the conventional comparators [1, 3] and the proposed comparator. When the differential input voltage of the two comparators in a precharge period, V_a, is 500 mV, which is the maximum differential input voltage of this flash ADC, the differential input voltages of two conventional comparators and the proposed comparator in an evaluation period, V_b, V_c, and V_d, are 493.8 mV, 490.5 mV, and 493.2 mV, respectively. The proposed comparator has low kickback noise similar to the conventional voltage comparator that utilizes a preamplifier [1].

III. Implementation and Measurement Results

The proposed flash ADC in Fig. 9 was fabricated using a 65-nm 1-poly 8-metal CMOS process with a 1-V supply voltage. The chip, including all pads, has a size of 1400 × 900 μm^2. The active area of the flash ADC is 620 × 340 μm^2. The power consumption of the track/hold, reference driver, and comparator array for the analog blocks are 2.7 mW, 2.06 mW, and 7.02 mW, respectively. Furthermore, the power consumption of the digital encoder and clock generator are 11.6 mW and 5.69 mW, respectively.

Figs. 10 and 11 show the measured frequency spectrum of the ADC output and the dynamic performance versus the frequency of the analog input signal. The measured SNDR is 35.37 dB at a sampling rate of 1.6 GS/s when the frequency of a 1-V_{PP} differential sinusoidal input signal is 795.51 MHz. An ENOB of more than 5.5 bits is maintained up to 800 MHz for the analog input signal. For the power efficiency of the ADC, the figure of merit (FoM) is given by Eq. (1).

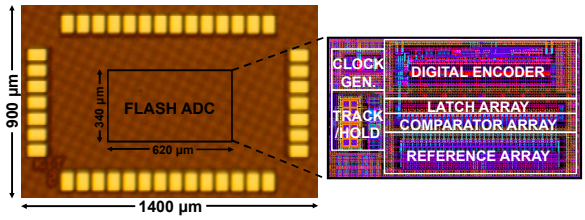


Fig. 9. Chip photograph.

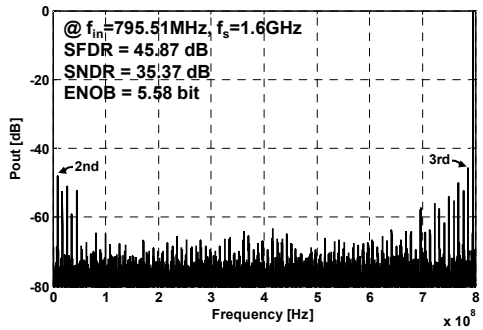


Fig. 10. Measured output spectrum.

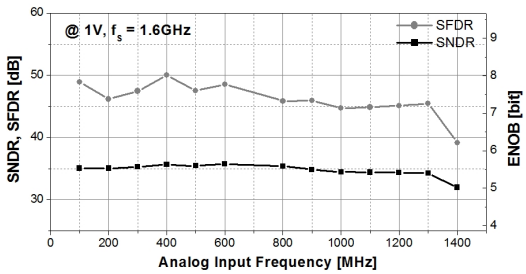


Fig. 11. Measured SNDR and SFDR versus input frequency.

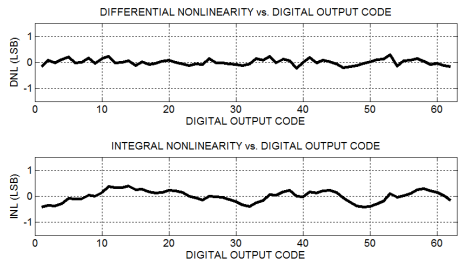


Fig. 12. Measured DNL and INL.

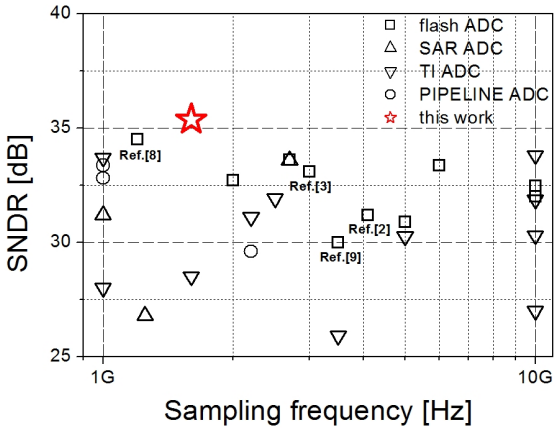
$$\text{FoM} = P/(2 \cdot \text{ERBW} \cdot 2^{\text{ENOB@Nyquist}}) \qquad (1)$$

The FoM of the flash ADC is 0.38 pJ/c-s. Fig. 12 shows that the DNL and INL are +0.28/-0.22 LSB and +0.41/-0.38 LSB, respectively.

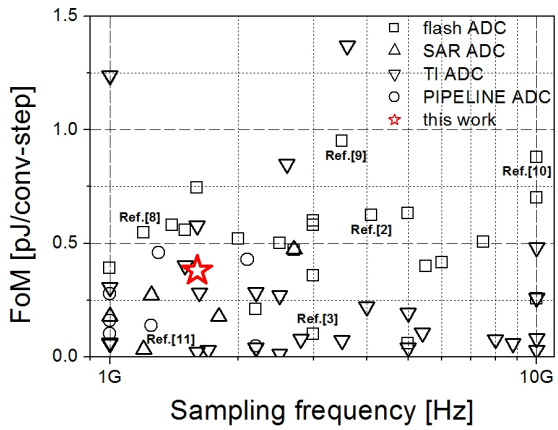
Table 1 and Fig. 13 summarize the performance comparison with previously reported high-speed ADCs. Fig. 13(a) presents the SNDR of 6-bit ADCs, and Fig. 13(b) shows the FoM of ADCs with a sampling rate of a few GHz, including recently reported high-speed ADCs [10, 11]. The ADC reported in literature [3] consumes a small power of 11 mW. However, this design does not fully support a binary 6-bit resolution. The proposed

Table 1. Performance summary and comparison

	Ref. [2]	Ref. [3]	Ref. [8]	Ref. [9]	This work
Technology	90 nm	40 nm	45 nm	90 nm	65 nm
Architecture	flash	flash	flash	flash	flash
Supply [V]	1.2	1.1	1.2	0.9	***1.0***
Resolution [bit]	6	6	6	6	6
f_s [GS/s]	4.1	3.0	1.2	3.5	1.6
ENOB [bit] @ Nyquist freq.	4.89	5.21	5.44	4.69	***5.58***
DNL [LSB]	0.49	-	0.5	0.5	***0.28***
INL [LSB]	0.74	0.35	0.6	0.96	0.41
Power [mW]	76.0	11.0	28.5	98	11.8(analog) 17.3(digital)
Area [mm^2]	2.75	0.021	0.1	0.15	0.21
FoM [pJ/c-s]	0.63	0.10	0.58	0.95	0.38



(a)



(b)

Fig. 13. Performance comparison (a) SNDR, (b) FoM.

ADC achieves a highest ENOB of 5.58 bits with a comparable FoM.

IV. CONCLUSIONS

In this work, a flash ADC with a high-speed time-domain comparator was proposed and has been implemented using a 65-nm 1-poly 8-metal CMOS process with a 1-V supply voltage. To reduce the power consumption and area of the flash ADC, analog blocks such as the source follower and preamplifier array are removed by using the proposed time-domain comparator. True single-phase clocked flip-flops with a leakage current compensation circuit were used for the digital encoder. The measured DNL and INL are 0.28 and 0.41 LSB, respectively. The SNDR was measured to be 35.37 dB at the *Nyquist* frequency. The FoM and chip area of the flash ADC are 0.38 pJ/c-s and $620 \times 340\ \mu m^2$, respectively.

ACKNOWLEDGMENTS

This research was supported by SK Hynix Inc., the MSIP, Korea, under the C-ITRC (IITP-2015-H8601-15-1011) supervised by the IITP, and the Basic Science Research Program through the NRF funded by the Ministry of Education (2013R1A1A4A01012914).

REFERENCES

[1] M. Choi and A. A. Abidi, "A 6-b 1.3Gsample/s A/D converter in 0.35-μm CMOS," *IEEE J. Solid-State Circuits,* Vol. 36, No. 12, pp. 1847-1858, Dec. 2001.

[2] J.-I. Kim, B.-R.-S. Sung, W. Kim, and S.-T. Ryu, "A 6-b 4.1-GS/s Flash ADC With Time-Domain Latch Interpolation in 90-nm CMOS," *IEEE J. Solid-State Circuits,* Vol. 48, No. 6, pp. 1429-1441, Jun. 2013.

[3] Y.-S. Shu, "A 6b 3GS/s 11mW fully dynamic flash ADC in 40nm CMOS with reduced number of comparators," *IEEE Symp. VLSI Circuits*, pp. 26-27, Jun. 2012.

[4] V. Hiremath and S. Ren, "A novel ultra high speed reconfigurable switching encoder for Flash ADC," *Proc. The IEEE National Aerospace and Electronics Conference*, pp. 320-323, July 2011.

[5] H.-Y. Lee and Y.-C. Jang, "A true single-phase clocked flip-flop witch leakage current compensation," *IEICE Electronics Express*, Vol. 9, No. 23, pp. 1807-1812, Dec. 2012.

[6] T. Kobayashi, K. Nogami, T. Shirotori, and Y. Fujimoto, "A current-controlled latch sense amplifier and a static power-saving input buffer for low-power architecture," *IEEE J. Solid-State Circuits,* Vol. 28, No. 4, pp. 523-527, Jun. 1993.

[7] D. Schinkel, E. Mensink, E. Klumperink, E.V. Tuijl, and B. Nauta, "Double-Tail Latch-Type Voltage Sense Amplifier with 18ps Setup+Hold Time," *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 314-315, Feb. 2007.

[8] P. Veldhorst, G. Goksun, A.-J. Annema, B. Nauta, B. Buter, and M. Vertregt, "A 0.45pJ/conv-step 1.2Gs/s 6b full-Nyquist non-calibrated flash ADC in 45nm CMOS and its scaling behavior," *IEEE Proc. European Solid-State Circuits Conf.,* pp.464-467, Sept. 2009.

[9] K. Deguchi, N. Suwa, M. Ito, T. Kumamoto, and T. Miki, "A 6-bit 3.5GS/s 0.9-V 98-mW flash ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits,* Vol. 43, No. 10, pp. 2303-2310, Oct. 2008.

[10] Y. Xu, L. Belostotski, and J. W. Haslett, "A 65-nm CMOS 10-GS/s 4-bit Background-Calibrated Noninterleaved Flash ADC for Radio Astronomy", *IEEE Trans. VLSI*, Vol. 22, No. 11, pp. 2316-2325, Nov. 2014.

[11] L. Kull, T. Toifl, M. Schmatz, P. A. Francese, C. Menolfi, M. Braendli, M. Kossel, T. Morf, T. M. Andersen, and Y. Leblebici, "A 3.1mW 8b 1.2GS/s single-channel asynchronous SAR ADC with alternate comparators for enhanced speed in 32nm digital SOI CMOS", *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, pp. 468-469, Feb. 2013.

Han-Yeol Lee was born in Gimcheon, Korea, on 1986. He received the B.S. and M.S. degrees in the department of electronic engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2012 and 2014, respectively. He is currently pursuing the Ph.D. degree in the Department of Electronic Engineering from Kumoh National Institute of Technology, Gumi, Korea. His current research interests are in the design of data converters.

Dong-Gil Jeong was born in Ulsan, Korea, on 1988. He received the B.S. and M.S. degrees in the department of electronic engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2013 and 2015, respectively. In 2015, he joined Siliconworks, Daejeon, Korea. His research interest includes automotive sensor.

Yu-Jeong Hwang was born in Masan, Korea, on 1990. She received the B.S. and M.S. degrees in the department of electronic engineering from Kumoh National Institute of Technology, Gumi, Korea, in 2013 and 2015, respectively. She is currently pursuing the Ph.D. degree in the Department of Electronic Engineering from Kumoh National Institute of Technology, Gumi, Korea. Her current research interests are in the design of PLL circuits.

Hyun-Bae Lee was was born in Seoul, Korea, on 1976. He received the B.S. degree in Physics, Yonsei University, Seoul, Korea, in 1999, and the M.S. and Ph.D. degrees from the Department of Electronic and Electrical Engineering, POSTECH, Kyungbuk, Korea, in 2001 and 2006, respectively. He joined SK hynix, Icheon, Korea, in 2011, where he is currently a Senior Engineer in the High Speed Interface Design Team. His research interests include off-chip/on-chip signal integrity, low-power sense amplifier circuit, high-speed low-power clocking circuits, and high-speed transceiver circuits.

Young-Chan Jang was born in Daegu, Korea, on 1976. He received the B.S. degree in the department of electronic engineering from Kyung-pook National University, Daegu, Korea, in 1999 and the M.S. and Ph.D. degrees in electronic engineering from Pohang University of Science and Technology (POSTECH), Pohang, Korea, in 2001 and 2005, respectively. From 2005 to 2009, he was a Senior Engineer in the Memory Division, Samsung Electronics, Hwasung, Korea, working on high-speed interface circuit design and next-generation DRAM. In 2009, he joined the Faculty of School of Electronic Engineering, Kumoh National Institute of Technology, Gumi, Korea, where he is currently Professor. His current research area is high-performance mixed-mode circuit design for VLSI systems such as high-performance signaling, clock generation, and analog-to-digital conversion.