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Design of DC Side Voltage and Compensation Analysis of THD for Shunt Power Quality Controller under System Load of Rectifier with R-L Load

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Abstract – For a shunt power quality controller (SPQC) the DC side voltage value which is closely related to the compensation performance is a significant parameter. Buy so far, very little discussion has been conducted on this in a quantitative manner by previous publications. In this paper, a method to design the DC side voltage of SPQC is presented according to the compensation performance in the single-phase system and the three-phase system respectively. First, for the reactive current and the harmonic current compensation, a required minimal value of the DC side voltage with a zero total harmonic distortion (THD) of the source current and a unit power factor is obtained for a typical load, through the equivalent circuit analysis and the Fourier Transform analytical expressions. Second, when the DC side voltage of SPQC is lower than the above-obtained minimal value, the quantitative relationship between the DC side voltage and the THD after compensation is also elaborated using the curve diagram. Hardware experimental results verify the design method.

Keywords: Power quality, Shunt power quality controller (SPQC), DC side voltage, Total harmonic distortion (THD), Compensation performance, Harmonics

1. Introduction

As advanced equipment for improving the power quality, Shunt Power Quality Controller (SPQC) combines the functions of Shunt Active Power Filter (SAPF) [1, 2] and Static Synchronous Compensator (STATCOM) [3, 4]. The SPQC can be used to compensate both the reactive current and the harmonic current. Three-phase voltage source converter is widely employed in SPQC [5]. The SPQC has a DC side voltage control loop to keep the DC side voltage as a constant which has a big influence on the compensation performance. When the SPQC is used to compensate the reactive current and the harmonic current, the higher the DC side voltage is, the better the compensation result is. However, with higher DC side voltage, voltage stress of the power device will be larger, and it will increase the cost. In addition, higher DC side voltage will cause bigger converter losses. So, in order to reduce the losses in practical applications, it is desirable to make the constant rated value of the DC side voltage as low as possible. According to the analysis above, the choice of the DC side voltage constant rated value of SPQC is very important, and needs a detailed quantitative analysis and specification.

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The researches on the DC side capacitor and DC voltage are very important. In many applications, the DC side voltage is controlled as a constant [6-8]. In [9], for a given DC side voltage, the maximum fundamental out voltage was shown in a wind generating system, and, it was very useful that the paper presented the relationship between the DC side voltage and the maximum fundamental output voltage. Furthermore, in [10], the selection of the DC side voltage for the Static Var Generator was presented, and the relationship between the compensation performance and the DC side voltage was also analyzed. These two papers mainly focused on the DC side voltage with the fundamental output voltage. However, the situation that the output voltage and the output current were the harmonic components was not discussed in these two papers. For the PAPF, in [11], an approximate value of the DC side voltage was presented, and the DC side voltage was selected as 1~1.3 p.u.. In [11], the DC side voltage selection methods presented approximate values. However the DC side voltage should be selected more accurately. In [12], the values of the DC side voltage were selected by considering the capability of reactive power compensation and harmonics current reduction. And, the capacitor value was designed to reduce the fluctuations of the DC side voltage caused by load unbalance and load change. The selection method of the DC side voltage was more accurate, but it may be a little complex. Especially, it is difficult to obtain the capability of harmonics current reduction. In [13], the DC side voltage reference was constant and was determined by simulation and experimental studies.

Simulation method was valid, but it was inconvenient. In order to design an accurate DC side voltage, in [14], the effect of the DC side voltage on the compensation performance of a PAPF was studied by focusing on 5th negative and 7th positive harmonic sequences. The minimal required DC side voltage for the linear modulation range was presented. But, only focusing on 5th and 7th harmonics was not comprehensive, and the method, which was mentioned in [14] to determine a DC side voltage value for all harmonic currents, was too complex. An accurate method to select the DC side voltage was presented in [15] for the system load with phase control six-pulse converter. The minimal DC side voltage was obtained by using the voltage instantaneous space vectors in the d-q orthogonal coordinates. The optimal instantaneous space vectors voltage was the minimum voltage that always existed inside the hexagon when the SVPWM was used. The selection method of the minimal DC side voltage mentioned in [15] was very useful. However, the further study should be presented when the DC side voltage was smaller than the minimal value, because the full compensation for harmonic current was not necessary at most of situations. When the DC side voltage is smaller than the minimal value and the modulation is nonlinear, the influence of the DC side voltage on the compensation performance has not been discussed in published papers. The relationship between the compensation performance and the DC side voltage should be analyzed in a quantitative manner.

This paper focuses on the design method of the DC voltage and the relationship between the compensation performance and the DC voltage. Specifically, the contributions of this paper are:

1) A required minimal value of the DC voltage for full compensation is presented.
2) For the situation where the DC voltage is smaller than the above-obtained minimal value, the quantitative relationship is detailed between the DC voltage value and the THD after compensation.
3) The DC side voltages of the single-phase system, the three-phase system with SPWM control and the three-phase system with SVPWM control are analyzed respectively.

2. DC Side Voltage Analysis and Specification

2.1 System configuration

There are two types of systems which are the single-phase system shown in Fig. 1 and the three-phase system shown in Fig. 2, where u_k(k=a, b, c) is the instantaneous value of the source phase voltage, i_{Lk} is the instantaneous value of the load phase current, i_{sk} is the instantaneous value of the source phase current, i_{ck} is the instantaneous value of the output phase current, and U_{dc} is the average value of the DC side voltage. Assume that the system is balanced, the single-phase equivalent circuit is shown in Fig. 3, where u_s is the instantaneous value of the source voltage, u_L is the instantaneous value of the voltage of inductor, i_c is the instantaneous value of the output current, u_I is the instantaneous value of the output voltage of converter. The losses of the converter are regarded as the active power in the resistor of the inductor [16].

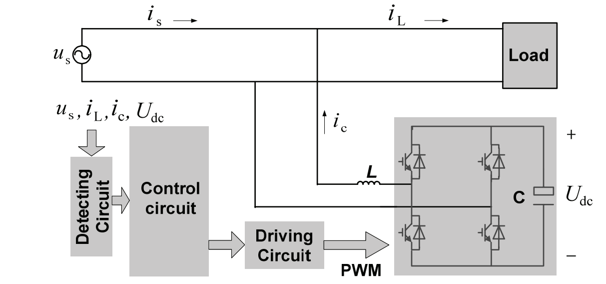


Fig. 1. Single-phase main circuit of the SPQC

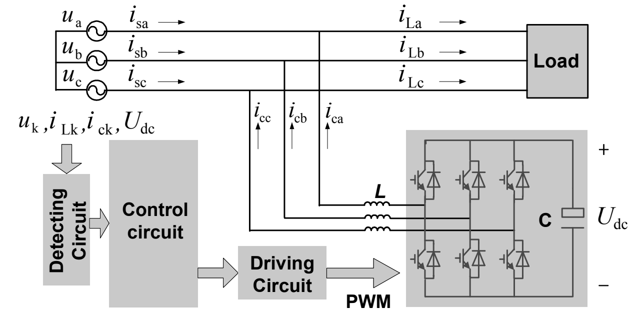


Fig. 2. Three-phase main circuit of the SPQC

2.2 Design of DC side voltage

The method of analysis adopts the superposition principle of the single-phase equivalent circuit in Fig. 3, and the relationship equations are shown in Eqs. (1) and (2).

$$u_{If} = u_s + L\frac{di_{cf}}{dt} \tag{1}$$

$$u_I = u_{If} + u_{Ih} = u_s + L\frac{di_{cf}}{dt} + L\frac{di_{ch}}{dt} \tag{2}$$

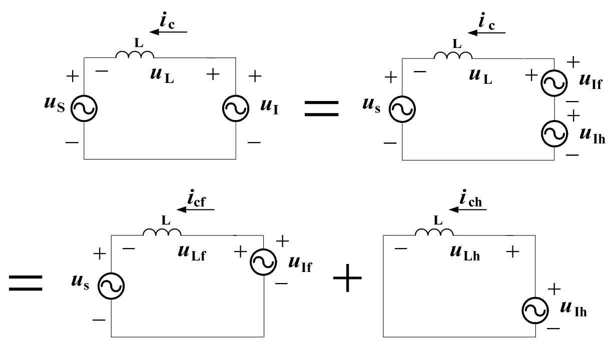


Fig. 3. Circuits of the principle of superposition

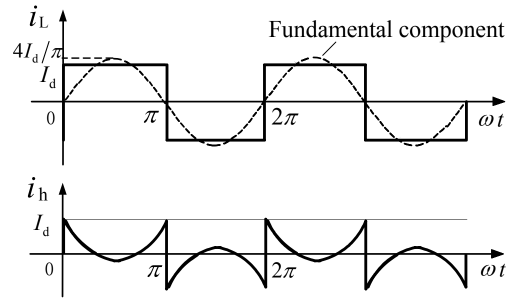


Fig. 4. System load current and reference current (single phase)

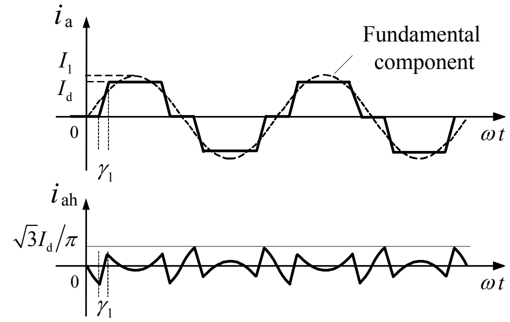


Fig. 5. System load current and reference current (three phases)

The maximal value of the output voltage (u_{I_max}) and the DC side voltage are shown in Eqs. (3) and (4), where k=1 for the single-phase system, $k = 1/2$ for the Sinusoidal Pulse Width Modulation (SPWM) and $k = 1/\sqrt{3}$ for the Space Vector Pulse Width Modulation (SVPWM) of the three-phase system [17-19]. The modulation index m=1.

$$u_{I\_max} = kmU_{dc} \tag{3}$$

$$U_{dc} = \frac{1}{km} u_{I\_max} \tag{4}$$

There are two basic issues for the PWM control of SPQC: The minimal DC side voltage for full compensation; and the influence on the THD of the source current when the DC side voltage is lower than the minimal value for the part compensation.

The system load is the rectifier with resistive and inductive load. The system load current and the output reference current are shown in Figs. 4 and Fig. 5. In Fig. 4, the single-phase load current is the ideal quadrate waveform. In Fig. 5, in the three-phase system, it is not an ideal waveform and it can be considered as a trapezoidal waveform which the overlap angles are less than 10º (usually occurring in electrical plants) [20].

2.3 Minimal DC side voltage at full compensation (For Single-phase System)

By using the Fourier analysis, the load current can be expressed as Eq. (5), where ω is the radian frequency of the fundamental component. The output reference current is shown in Eq. (6).

$$\begin{aligned} i_L &= \frac{4}{\pi} I_d \left[\sin \omega t + \frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \cdots \right] \\ &= \frac{4}{\pi} I_d \sum_{n=1,3,5,\cdots}^{\infty} \frac{1}{n} \sin n\omega t \end{aligned} \tag{5}$$

$$\begin{aligned} i_{ch} &= \frac{4}{\pi} I_d \left[\frac{1}{3}\sin 3\omega t + \frac{1}{5}\sin 5\omega t + \cdots \right] \\ &= \frac{4}{\pi} I_d \sum_{n=3,5,\cdots}^{\infty} \frac{1}{n} \sin n\omega t \end{aligned} \tag{6}$$

The inductor voltage can be expressed as Eq. (7).

$$\begin{aligned} u_{Lh} &= \frac{4}{\pi} I_d \omega L \left[\cos 3\omega t + \cos 5\omega t + \cdots \right] \\ &= \frac{4}{\pi} I_d \omega L \sum_{n=3,5,\cdots}^{\infty} \cos n\omega t \end{aligned} \tag{7}$$

Assume that

$$f_1(\omega t) = \cos 3\omega t + \cos 5\omega t + \cdots = \sum_{n=3,5,\cdots,25} \cos n\omega t \tag{8}$$

The output current can be shown as Eq. (9).

$$I_{ch} = \frac{4}{\pi} I_d \sqrt{\sum_{n=3,5,7,\cdots,25} \left(\frac{1}{\sqrt{2}n} \right)^2} \tag{9}$$

According Eqs. (7) and (9), the waveform of $f_1(\omega t)$ is shown in the Appendix by using the mathematical software. The peak value of $f_1(\omega t)$ in Eq. (8) is 25.9 at ωt=0. Because the peak value of $\omega L I_{ch} f_1(\omega t)$ is much larger than the peak value of the source voltage, the peak value of the output voltage can be expressed as Eq. (10), where the source phase voltage is $u_s = \sqrt{2}U_s \sin(\omega t + \varphi)$, φ is the phase between the source phase voltage and the source phase current, and I_{cq} is the RMS value of the output reactive current (assume that I_{cq} is RMS value of the required output reactive current).

$$U_{dc} = u_{I\_max} \approx \sqrt{2}\left[\left(U_s + \omega L I_{cq} \right) \sin \varphi + 25.9 \times \omega L I_{ch} \right] \tag{10}$$

When the output harmonic current is zero, the DC side voltage is 1.414(U_s+ωLI_{cq}). From Eq. (10), the DC side voltage is related to the phase φ and the output harmonic current. Assume that the base of per-unit is (U_s+ωLI_{cq}) and k_L=ωLI_{ch}/(U_s+ωLI_{cq}), the DC side voltage in Eq. (10) can be expressed as Eq. (11). The minimal DC side voltage with the typical values of phase φ is illustrated in Fig. 6. If

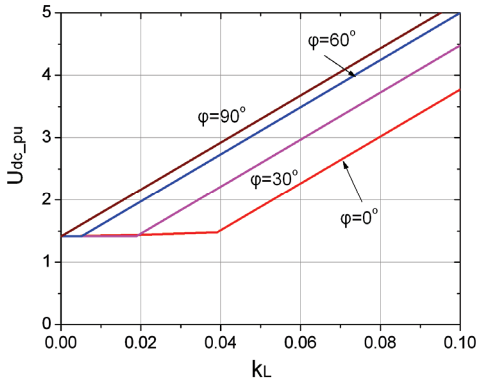


Fig. 6. Relationship between the minimal DC side voltage and k_L (single phase)

the peak value of $25.9\omega LI_{ch}f_1(\omega t)$ is smaller than the value of $(U_s+\omega LI_{cq})$, the DC side voltage is determined by the peak value of $(U_s+\omega LI_{cq})$. When the DC side voltage is lower than $1.414(U_s+\omega LI_{cq})$, the DC side voltage is chosen as $1.414(U_s+\omega LI_{cq})$. So, there is an inflection point of the curves. The current of harmonic orders from 5th to 25th is just considered.

$$U_{dc\_pu}=\sqrt{2}\sin\varphi+\sqrt{2}k_L\times 25.9 \tag{11}$$

2.4 Minimal DC side voltage at full compensation (For Three-phase system with SPWM control)

When the SPWM is used in three-phase system, the load current from 0~π can be considered as Eq. (12) from Fig. 5, where γ_1 is overlap angle.

$$i_a=\begin{cases}0 & 0<\omega t\le\frac{\pi}{6}-\frac{\gamma_1}{2}\\ \frac{I_d}{\gamma_1}(\omega t-\frac{\pi}{6}+\frac{\gamma_1}{2}) & \frac{\pi}{6}-\frac{\gamma_1}{2}<\omega t\le\frac{\pi}{6}+\frac{\gamma_1}{2}\\ I_d & \frac{\pi}{6}+\frac{\gamma_1}{2}<\omega t\le\frac{\pi}{6}+\frac{2\pi}{3}-\frac{\gamma_1}{2}\\ -\frac{I_d}{\gamma_1}(\omega t-\frac{2\pi}{3}-\frac{\pi}{6}-\frac{\gamma_1}{2}) & \frac{\pi}{6}+\frac{2\pi}{3}-\frac{\gamma_1}{2}<\omega t\le\frac{2\pi}{3}+\frac{\pi}{6}+\frac{\gamma_1}{2}\\ 0 & \frac{2\pi}{3}+\frac{\pi}{6}+\frac{\gamma_1}{2}<\omega t\le\pi\end{cases} \tag{12}$$

The Fourier series of load current from 0 to 2π is shown in Eq. (13). And, the output reference current can be obtained as Eq. (14). The RMS value of the output reference current is expressed as Eq. (15), when the current of harmonic orders from 5th to 25th is just considered.

$$i_a=\sum_{n=1}^{\infty}\frac{8}{n\pi}I_d\frac{1}{n\gamma_1}\sin n\left(\frac{\pi}{3}\right)\sin\frac{n\gamma_1}{2}\sin\frac{n\pi}{2}\sin n\left(\omega t-\frac{\gamma_1}{2}\right) \tag{13}$$

$$i_{ch}=\sum_{n=1}^{\infty}\left[\frac{8}{n\pi}I_d\frac{1}{n\gamma_1}\sin n\left(\frac{\pi}{3}\right)\sin\frac{n\gamma_1}{2}\sin\frac{n\pi}{2}\right]\sin n\left(\omega t-\frac{\gamma_1}{2}\right) \tag{14}$$

$$I_{ch}=\frac{I_d}{\sqrt{2}}\sqrt{\sum_{n=5,7,11,13,17,19,23,25}\left[\frac{8}{n\pi}\frac{1}{n\gamma_1}\sin n\left(\frac{\pi}{3}\right)\sin\frac{n\gamma_1}{2}\sin\frac{n\pi}{2}\right]^2} \tag{15}$$

Assume that the inductor voltage is u_L. I_{ch} is the RMS of output current of phase *a*. u_L can be expressed as Eq. (16).

$$u_L=\sqrt{2}\omega LI_{ch}\times f_2(\omega t) \tag{16}$$

Where

$$f_2(\omega t)=\frac{\sum_{n=5,7,11,13,17,19,23,25}\left[\frac{8}{\pi}\frac{1}{n\gamma_1}\sin n\left(\frac{\pi}{3}\right)\sin\frac{n\gamma_1}{2}\sin\frac{n\pi}{2}\right]\cos n\left(\omega t-\frac{\gamma_1}{2}\right)}{\sqrt{\sum_{n=5,7,11,13,17,19,23,25}\left[\frac{8}{n\pi}\frac{1}{n\gamma_1}\sin n\left(\frac{\pi}{3}\right)\sin\frac{n\gamma_1}{2}\sin\frac{n\pi}{2}\right]^2}} \tag{17}$$

The peak value of $f_2(\omega t)$ is $f(\gamma_1)$. By using the mathematical software, the values of $f(\gamma_1)$ can be obtained according to γ_1. The relationship between $f(\gamma_1)$ and γ_1 is illustrated in Fig. 7. From Fig. 7, the value of $f(\gamma_1)$ can be gotten according to the value of γ_1.

Because the peak value of $\omega LI_{ch}f(\gamma_1)$ is much larger than the peak value of the source voltage, the value of the output voltage reaches the peak value at $\omega t=\pi/6$. The minimal DC side voltage is shown in Eq. (18). The DC side voltage in Eq. (18) can be expressed as Eq. (19). And, the relationship between the minimal value and k_L are carried out in Fig. 8 with different γ_1 and φ.

$$U_{dc}=2\sqrt{2}\left(U_s+\omega LI_{cq}\right)\sin\left(\frac{\pi}{6}+\varphi\right)+2\sqrt{2}\omega LI_{ch}f(\gamma_1) \tag{18}$$

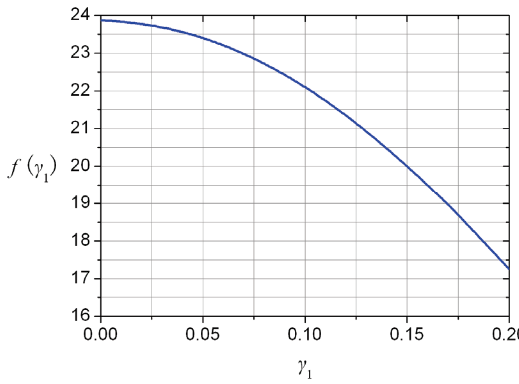


Fig. 7. Relationship between $f(\gamma_1)$ and γ_1

$$U_{dc} = 2\sqrt{2}\sin\left(\frac{\pi}{6}+\varphi\right)+2\sqrt{2}k_L f(\gamma_1) \tag{19}$$

2.5 Minimal DC side voltage at full compensation (For three-phase system with SVPWM control)

When the SVPWM is used in three-phase system, the output voltages of inverter are shown in Eq. (20). The output voltages are transformed into α-β frame, and the voltage vector are expressed as Eq. (21) and Eq. (22) [21, 22]. The switching vectors are shown in Eq. (23). If the voltage vector exists inside the hexagon in Fig. 9, the THD of the source current after compensation is zero [14].

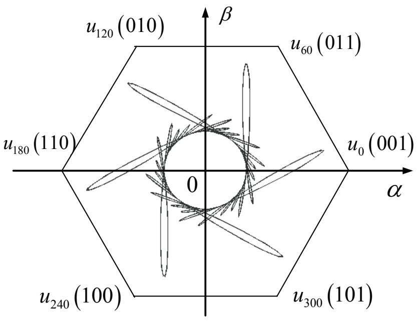
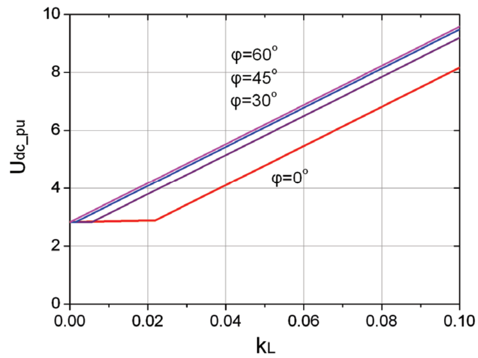
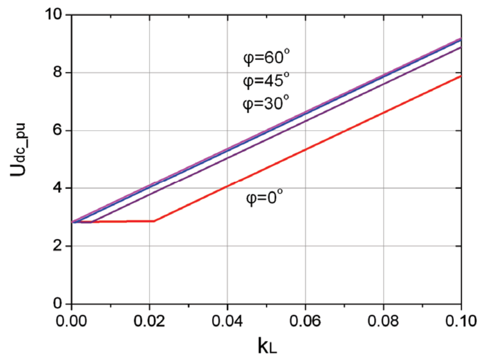


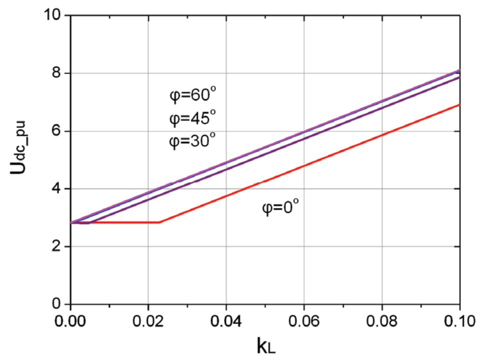
Fig. 9. Relationship between space vector and hexagon (for full compensation)



(a) γ_1=0°

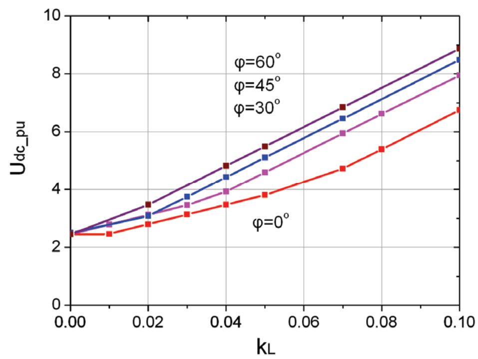


(b) γ_1=5°

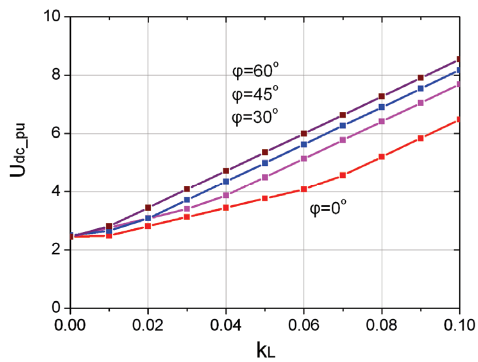


(c) γ_1=10°

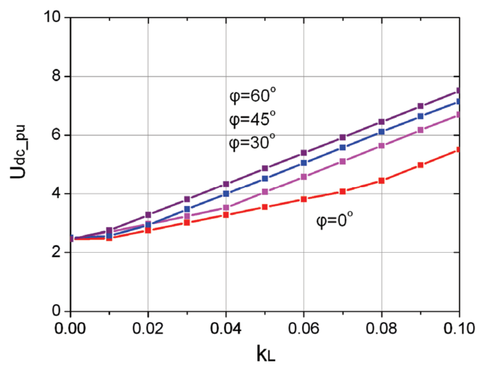
Fig. 8. Relationship between the minimal DC side voltage and k_L (three-phase system with SPWM control)



(a) γ_1=0°



(b) γ_1=5°

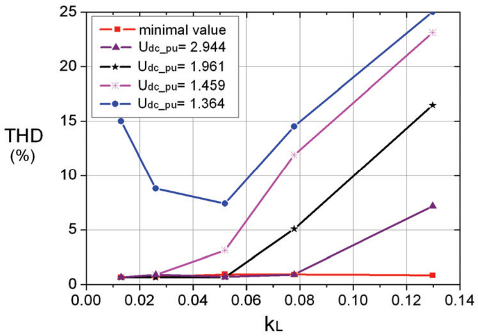


(c) γ_1=10°

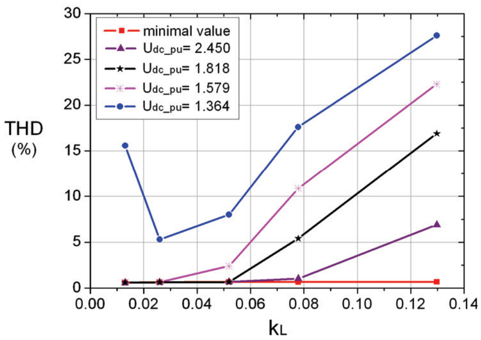
Fig. 10. Relationship between the minimal DC side voltage and k_L (three-phase system with SVPWM control)

$$\begin{cases} u_{\text{I\_a}} = \sqrt{2}\left(U_{\text{s}} + \omega L I_{\text{ch}}\right)\sin\left(\omega t + \varphi\right) + \sqrt{2}\omega L I_{\text{ch}} f(\gamma_1) \\ u_{\text{I\_b}} = \sqrt{2}\left(U_{\text{s}} + \omega L I_{\text{ch}}\right)\sin\left(\omega t + \varphi - \dfrac{2\pi}{3}\right) + \sqrt{2}\omega L I_{\text{ch}} f(\gamma_1) \\ u_{\text{I\_c}} = \sqrt{2}\left(U_{\text{s}} + \omega L I_{\text{ch}}\right)\sin\left(\omega t + \varphi + \dfrac{2\pi}{3}\right) + \sqrt{2}\omega L I_{\text{ch}} f(\gamma_1) \end{cases} \tag{20}$$

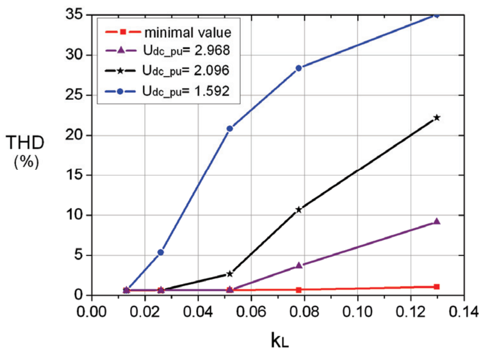
$$\begin{cases} u_{\text{I\_alpha}} = \sqrt{\dfrac{2}{3}}\left[u_{\text{I\_a}} - \dfrac{1}{2}u_{\text{I\_b}} - \dfrac{1}{2}u_{\text{I\_c}}\right] \\ u_{\text{I\_beta}} = \sqrt{\dfrac{2}{3}}\left[\dfrac{\sqrt{3}}{2}u_{\text{I\_b}} - \dfrac{\sqrt{3}}{2}u_{\text{I\_c}}\right] \end{cases} \tag{21}$$



(a) φ=0°



(b) φ=30°



(c) φ=60°

Fig. 11. Relationship between DC side voltage and compensation performance (single phase)

$$\vec{v} = \begin{bmatrix} u_{\text{I\_alpha}} \\ u_{\text{I\_beta}} \end{bmatrix} \tag{22}$$

$$|u_0| = |u_{60}| = |u_{120}| = |u_{180}| = |u_{240}| = |u_{300}| = \sqrt{\frac{2}{3}}U_{\text{dc}} \tag{23}$$

The minimal DC side voltage is shown in Fig. 10 with different γ_1 and φ by using the mathematical software.

3. Analysis of Compensation Characteristics with DC Side Voltage Lower than the Minimal Value

In order to reduce the DC side voltage, the compensation performance can be reduced, as long as the requirement of THD after compensation is satisfied. When the DC side voltage is lower than the minimal value, the modulation control is the non-linear control. It is very difficult to analyze the relationship between the compensation performance and the DC side voltage. A group of simulation results are present to obtain the relationship between the compensation performance and the DC side voltage in this paper.

3.1 For single-phase system

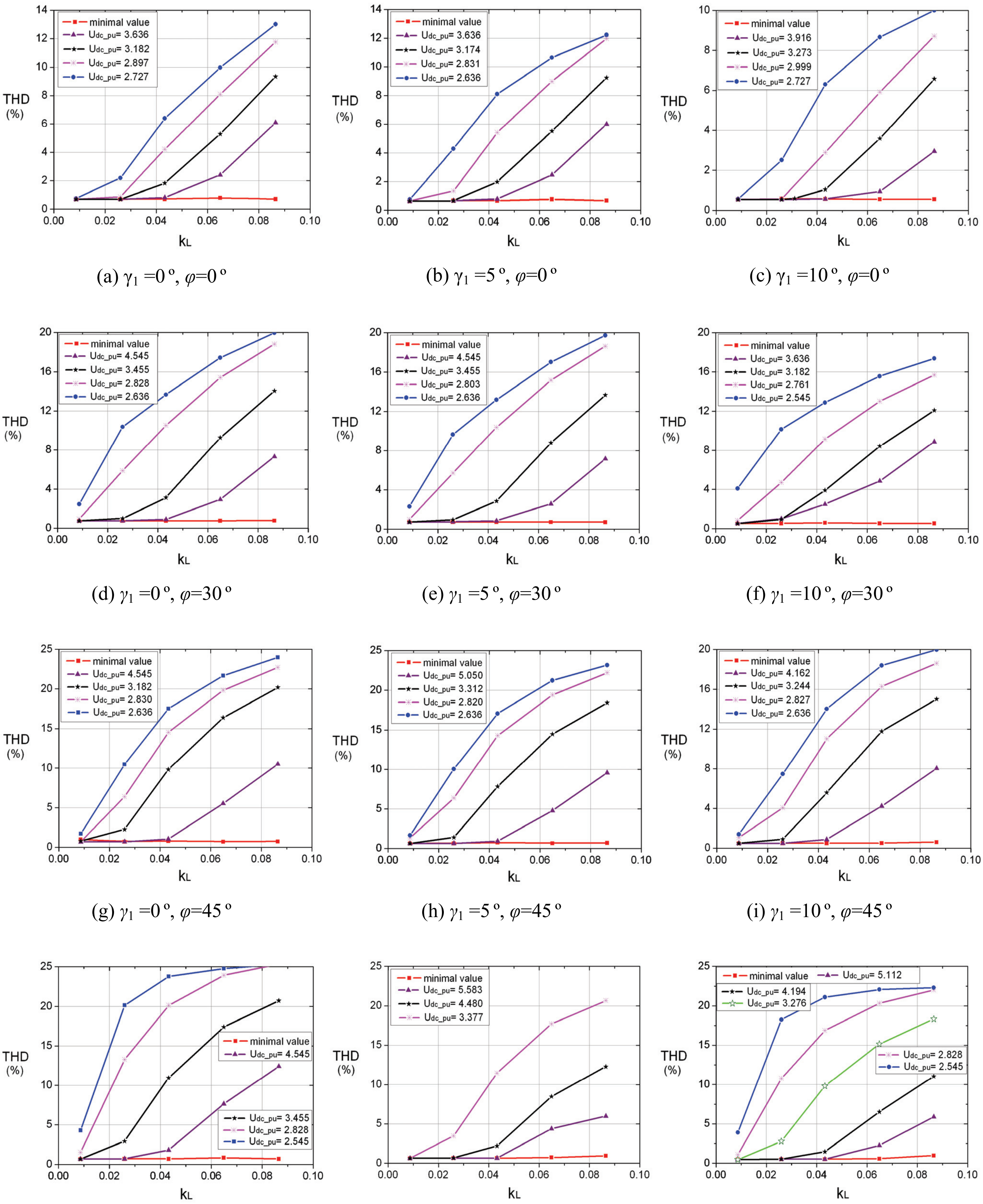
In Fig. 11, with different φ and k_{L}, the THD of the source current is presented. The THD becomes unregulated when the DC side voltage is lower than 1.414 times of the peak value of the source voltage. Because the DC side voltage of inverter is 1.414 p.u. when the output current is zero. If I_{cq} is changed, the base of per-unit is also changed to (U_{s}+$\omega L I_{\text{cq}}$), and $U_{\text{dc\_pu}}$ in the figure is based on the per-unit value.

3.2 For three-phase system with SPWM control

When the DC side voltage is lower than the minimal value, the modulation control is the non-linear control. A group of simulation results are present to obtain the relationship between the compensation performance and the DC side voltage in this paper. From Fig. 12, with different φ, k_{L} and γ_1, the THD of the source current after compensation is presented. With those curves, the relationship between the compensation performance and the DC side voltage are obtained.

3.3 For Three-phase system with SVPWM control

When the DC side voltage is lower than the minimal value, the THD of the source current after compensation is presented in Fig. 13 with different φ, k_{L} and γ_1 by using the simulation software.



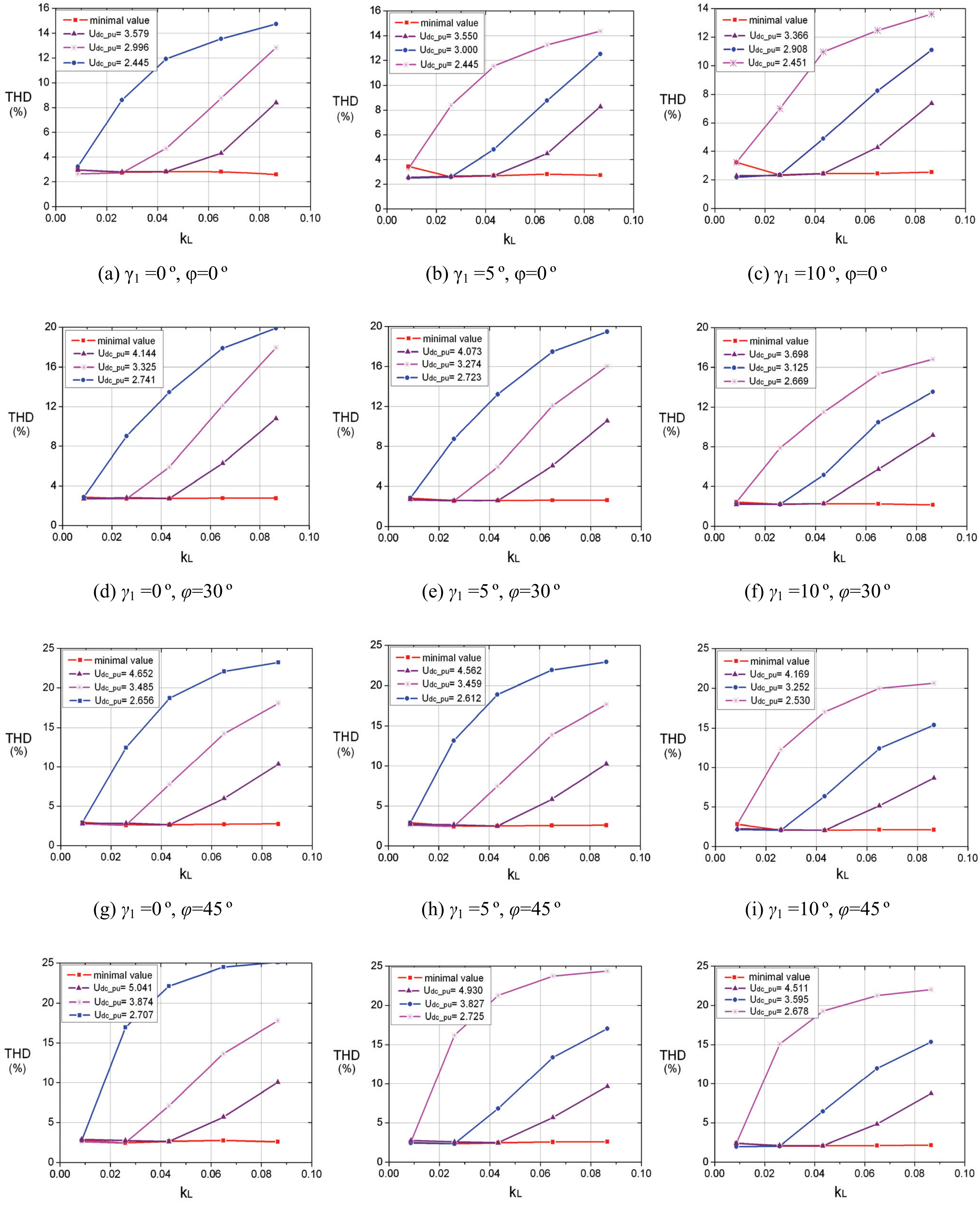
(a) γ_1 =0°, φ=0°　(b) γ_1 =5°, φ=0°　(c) γ_1 =10°, φ=0°

(d) γ_1 =0°, φ=30°　(e) γ_1 =5°, φ=30°　(f) γ_1 =10°, φ=30°

(g) γ_1 =0°, φ=45°　(h) γ_1 =5°, φ=45°　(i) γ_1 =10°, φ=45°

(j) γ_1 =0°, φ=60°　(k) γ_1 =5°, φ=60°　(l) γ_1 =10°, φ=60°

Fig. 12. Relationship between DC side voltage and compensation performance for three-phase system with SPWM control



(a) γ_1 =0°, φ=0° (b) γ_1 =5°, φ=0° (c) γ_1 =10°, φ=0°

(d) γ_1 =0°, φ=30° (e) γ_1 =5°, φ=30° (f) γ_1 =10°, φ=30°

(g) γ_1 =0°, φ=45° (h) γ_1 =5°, φ=45° (i) γ_1 =10°, φ=45°

(j) γ_1 =0°, φ=60° (k) γ_1 =5°, φ=60° (l) γ_1 =10°, φ=60°

Fig. 13. Relationship between DC side voltage and compensation performance for three-phase system with SVPWM control

4. Simulation and Experimental Results

The simulation investigation and the experiment were carried out to verify the minimal DC side voltage equations and the output current equations after changing DC side voltages.

For a design example, in three-phase system for full compensation, the DC side voltage was related to the phase angle between the source phase voltage and the peak value of inductor voltage. When the system load was diode rectifier with resistive and inductive load, the phase angle was 0º. In Fig. 14, the inductor was 0.4mH. The RMS of the source phase voltage was 220V. The output current (RMS) was 93.6A.The modulation index was 1, and the triangular wave modulation SPWM was used.

In Fig. 14, the overlap angle was $\gamma 1=0$ and the DC side voltage for full compensation was 1104V according to the theoretical analysis. The compensation result was acceptable with a minimal DC side voltage 1104V and the THD of the source current after compensation was 0.5% (harmonic current from 5^{th} to 25^{th} order was just considered), which approximately equaled to the theoretical value (0%). The simulation results verified the analysis and the conclusion about the minimal DC side voltage. Because of the current tracking error and the dead time of PWM, in practical applications, the DC side voltage should be higher than the theoretical value, when the SPQC is designed. The theoretical value is the best situation with zero tracking error and one modulation index. The Eq. (11), Eq. (19) and diagrams can be used as a reference of the best situation.

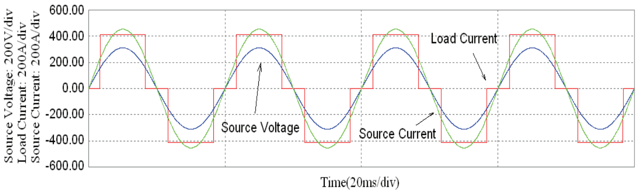


Fig. 14. Compensation result with the minimal DC side voltage (for SPWM)

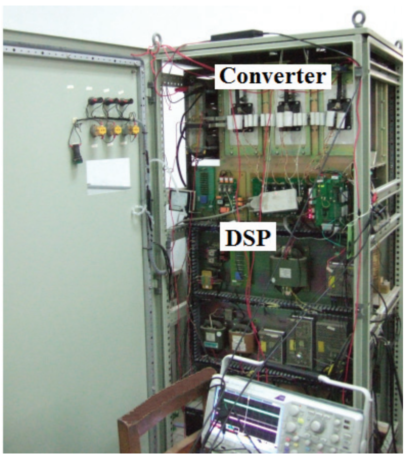


Fig. 15. Experimental hardware view

However, in the practical applications, the voltage which is lower than 1104V is used, as the compensation result with a THD lower than 5% is satisfied.

In order to verify the analysis results, the hardware experiment has been carried out which is shown in Fig. 15. For a design example, the three-phase inverter was used. The DSP TMS320F2812 was used to realize the direct current control strategy and the PWM control method. The peak value of the phase source voltage is U_s=70.7V, the inductor is 5.5mH, the capacitor of DC side is 3333uF, and I_{cq} is zero.

For the SPWM control, in Fig. 16, the overlap angle was 5.9º and $\gamma_1 \approx 17$. The output current was 0.086 p.u., and the theoretical DC side voltage was 6.963 p.u.. The dead time of PWM was 4μs and the switching frequency was 15kHz, so the error was approximately 6%, then the minimal DC side voltage was modified as 7.558 p.u.. In Fig. 17, the source current after compensation was presented with the minimal DC side voltage. The THD of the source current was very small and it was 3.5%(from 5^{th} to 25^{th}) after compensation. From the experimental results, the selection method of the minimal DC side voltage was verified. Because of the current tracking error and the dead time of PWM, in practical applications, the DC side voltage should be higher than the theoretical value, when the SPQC was designed. The theoretical value was the best situation with a zero tracking error and one modulation index. The Eq. (19) and diagrams can be used as a reference of the best situation.

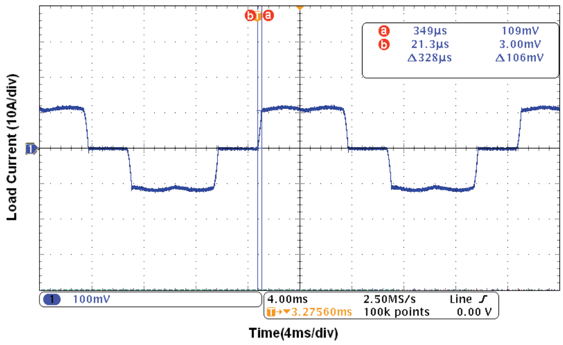


Fig. 16. Load current

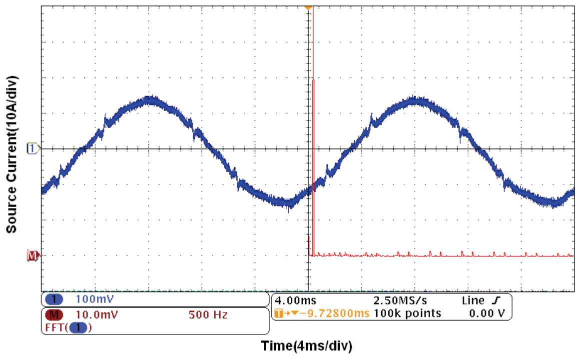


Fig. 17. Source current after compensation

The simulation and experimental results verified the design method of the DC side voltage. For a design point of view, the equations and curves of DC side voltage can be used as reference to determine DC side voltage. The dead time of PWM and the current tracking error should be considered, and chooses a suitable DC side voltage according to the desired THD.

5. Conclusion

In this paper, a method to design the DC side voltage of SPQC and the DC side voltage rated value are presented according to the compensation performance. A required minimal value of the DC side voltage for full compensation is obtained for a typical harmonic current. In order to reduce the DC side voltage, the compensation performance can be reduced, as long as the requirement of THD after compensation is satisfied. The quantitative relationship between the DC voltage and the THD after compensation is detailed when the DC voltage is smaller than the above-obtained minimal value by using the curve diagrams. The curve diagrams can be used as a reference of the best situation, and the DC side voltage should be higher than the best situation with the tracking error and dead time. Hardware experimental results verify the validity of the design method.

Acknowledgements

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Appendix

A. Derivation of Eq. (9)

The RMS value of the output reference current (I_{ch}) is

$$I_{ch}=\sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_{ch}^2 d(\omega t)}$$
$$=\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{4}{\pi}I_d\sum_{n=3,5,\cdots,25}\frac{1}{n}\sin n\omega t\right)^2 d(\omega t)}$$

Because

$$\int_0^{2\pi}\left(\sum_{n=3,5,\cdots,25}\frac{1}{n}\sin n\omega t\right)^2 d(\omega t)$$
$$=\int_0^{2\pi}\left[\sum_{n=3,5,\cdots,25}\left(\frac{1}{n}\sin n\omega t\right)^2\right]d(\omega t)$$

the RMS value of the output reference current (I_{ch}) is

$$=\frac{4}{\pi}I_d\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\sum_{n=3,5,\cdots,25}\left(\frac{1}{n}\sin n\omega t\right)^2 d(\omega t)}$$
$$=\frac{4}{\pi}I_d\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\sum_{n=3,5,\cdots,25}\left(\frac{1}{n}\right)^2\frac{1-\cos 2n\omega t}{2}d(\omega t)}$$
$$=\frac{4}{\pi}I_d\sqrt{\sum_{n=3,5,7,\cdots,25}\left(\frac{1}{\sqrt{2}n}\right)^2}$$

B. Derivation of Variable 25.9 in Eq. (10) by the Mathematical Software

According equations (7) and (9), draw the waveform of $f_1(\omega t)$ in equation (10) by the mathematical software. Then, the value of 25.9 can be obtained in the following figure, that is, the peak value of the waveform is approximately 25.9.

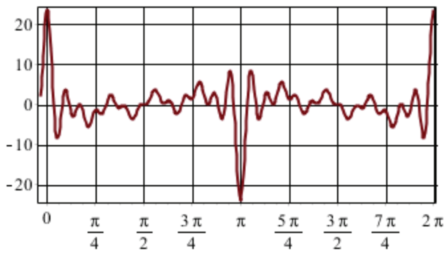

Fig. 18. Waveform of $f_1(\omega t)$

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