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Threshold Voltage Properties of OFET with CuPc Active Material

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Abstract

In this study, organic field-effect transistors (OFETs) using a copper phthalocyanine (CuPc) material as an active layer and SiO_2 as a gate insulator were fabricated with varying active layer thicknesses and channel lengths. Further, using a thermal evaporation method in a high-vacuum system, we fabricated a CuPc FET device of the top-contact type and used Au materials for the source and drain electrodes. In order to discuss the channel formation and FET characteristics, we observed the typical current–voltage characteristics and calculated the threshold voltage of the CuPc FET device. We also found that the capacitance reached approximately 97 pF at a negative applied voltage and increased upon the accumulation of carriers at the interface of the metal and the CuPc material. We observed the typical behavior of a FET when used as an n-channel FET. Moreover, we calculated the threshold voltage to be about 15–20 V at $V_{DS} = -80$ V.

Index Terms: Copper phthalocyanine (CuPc), Current–voltage characteristics, Organic FET, Threshold voltage

I. INTRODUCTION

Organic semiconductors have recently been used as active layers in electronic devices such as field-effect transistors (FETs) [1]. Over the last two decades, organic materials and organic semiconducting devices have become a focus of intense research and advancement in both academia and industry. This significant commercial interest in organic electronics stems from their potential as building blocks for inexpensive and structurally flexible electronic devices, including radio-frequency identification tags, smart cards, light-emitting diodes, and flexible displays [2, 3]. For applications involving active circuits, organic field-effect transistors (OFETs) are the devices at the heart of switching and logic operations. The mobility of charger carriers is generally lower than that of crystalline inorganic semiconductors, thereby limiting switching frequencies and demanding higher voltages for similar current levels. The general electrical characteristics of OFETs are well described within the model of metal-oxide semiconductor FET (MOSFET) theory since the electrical properties of OFETs depend on the properties of the organic layer, such as the active layer material used and the material thickness. Recent improvements to the manufacturing process and modifications of the device structure allow for the fabrication of OFETs with mobility comparable to that of amorphous silicon semiconductors with the former material being a popular choice for the fabrication and performance evaluation of organic thin-film devices [4, 5]. Copper phthalocyanine (CuPc) materials are widely used in organic

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light-emitting diodes (OLEDs) and OFETs. Thus far, considerable experimental effort, such as modification of the film quality, has been devoted to the improvement of the device performance. It is important to understand the electrostatic phenomena at the interface between metal and organic materials in order to improve the organic FET device performance. According to the recent research, it has been revealed little by little that carrier was supplied from source or drain electrode in organic FET. In such situation, understanding of the injection behavior of charges at the metal/organic interface is necessary to improve the organic FET operation. Thus the study of the electrostatic interfacial phenomena in organic FET device, which strongly affects the injection behavior at the organic film and metal interfaces, is of special importance to the fields of organic electronics [3].

In the present paper, we present the current–voltage (I–V) characteristics to clarify that the carrier transport and the threshold voltage were estimated from the I–V curves in CuPc FETs with varying active layer thicknesses and channel lengths. Further, we observed the capacitance–voltage (C–V) properties of a CuPc FET for determining the charge carrier characteristics between an organic layer and an inorganic substrate.

II. DEVICE FABRICATION

Fig. 1 shows the device structure of a top-contact CuPc FET, the molecular structure of the CuPc materials, and the experimental setup for the measurement of the I–V and C–V characteristics. An Au electrode and a substrate were subjected to an ultraviolet (UV)/ozone treatment on the SiO_2 insulating layer for 30 minutes before deposition of the CuPc material and were used a silicon wafer as a substrate.

CuPc was deposited onto the substrate by using the thermal evaporation method at a deposition rate of 0.5 (Å/s) at 10^{-6} Torr, in various thicknesses such as 5, 10, 20, 40, and 80 nm. Further, the channel length (L) was 30, 40, 50, and 100 mm, and the channel width (W) was fixed at 3 mm. The I–V and C–V measurements were carried out under ambient conditions by using a source meter (Keithley type 2400) and an LCR meter.

III. RESULTS AND DISCUSSION

In OFET devices, the drive current flowing between the source and the drain, I_{DS}, of the transistor in a linear regime, predicted using the gradual channel approximation, can be expressed as follows:

$$I_{DS} = \frac{W}{L} \mu C_i (V_G - V_{th} - V_{DS}) V_{DS} \ , \qquad (1)$$
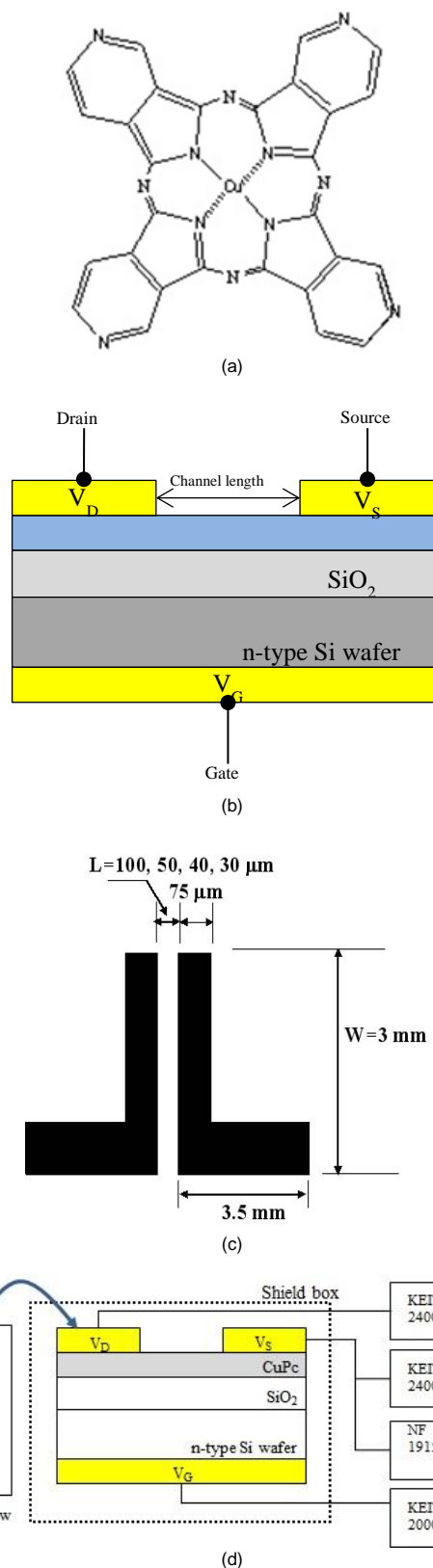
Fig. 1. Schematic of the CuPc molecular structure and the CuPc field-effect transistor device. (a) Molecular structure. (b) Device structure (side view). (c) Device structure (top view). (d) Experimental setup.

(a)

(b)

(c)

(d)

(e)
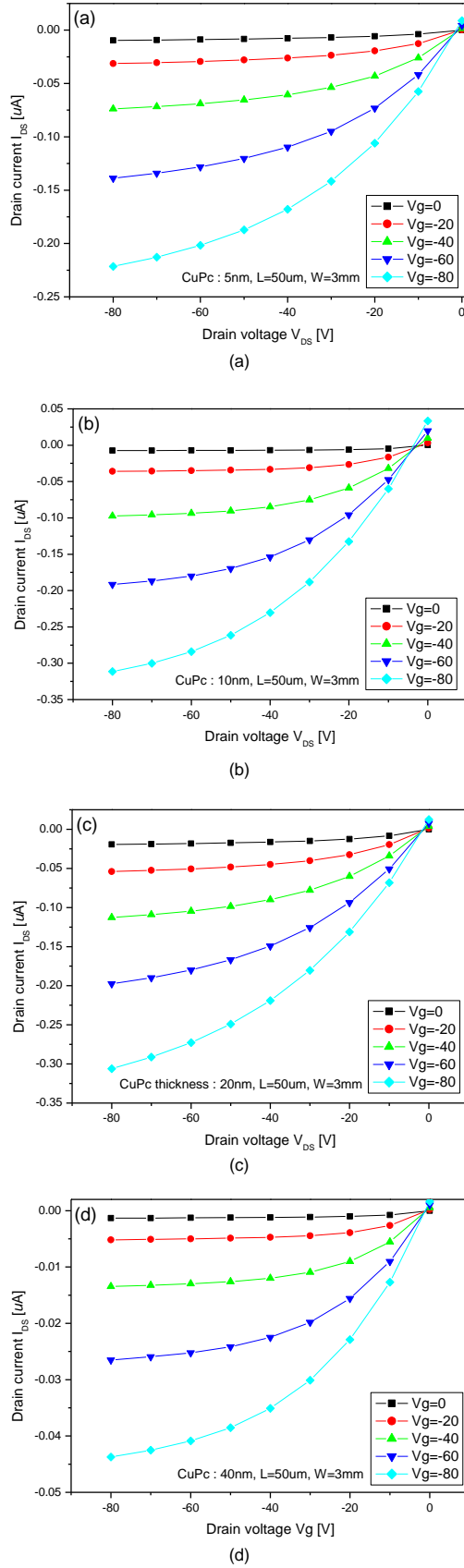
Fig. 2. I−V characteristics of CuPc field-effect transistor devices with different thicknesses of the CuPc thin films: (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 40 nm, and (e) 80 nm.

where W denotes the channel width, L represents the channel length, μ denotes the mobility, and C_i indicates the capacitance of the SiO$_2$ insulating layer. Further, V_G denotes the gate voltage and V_{th} represents the threshold voltage. When $V_{DS} > V_G - V_{th}$, the transistor operates in the saturation regime. The drive current under saturation conditions is dependent on V_{DS}, and thus, (1) can be simplified as follows:

$$I_{DS} = \frac{W}{2L}\mu C_i (V_G - V_{th})^2. \tag{2}$$

In the saturation regime, μ can be calculated from the slope of the plot of the square root of the drain current versus V_G. Further, when a voltage is applied between the source and the gate, a change is induced at the insulator–semiconductor interface [6].

Fig. 2 shows the current–voltage (I_{DS}–V_{DS}) characteristics of CuPc top-contact FETs having various thicknesses such as 5, 10, 20, 40, and 80 nm. The applied gate voltage ranged from 0 to –80 V, and the scanning rate for the calculation of I_{DS}−V_{DS} ranged from 0 to –80 V and also shows the typical FET behavior.

We calculated the carrier mobility of the CuPc FET on the basis of the electrical properties of the CuPc thin films having different active layer thicknesses.

The mobility was 9.7×10^{-5} cm^{2}V^{-1}s^{-1}, 7.1×10^{-5} cm^{2}V^{-1}s^{-1}, 2.5×10^{-5} cm^{2}V^{-1}s^{-1}, and 1.2×10^{-5} cm^{2}V^{-1}s^{-1} for 5-nm-thick, 20-nm-thick, 40-nm-thick, and 80-nm-thick CuPc FET devices, respectively. The mobility of the CuPc FETs was not very high in comparison with the mobility of pentacene FET, as a reported in references [3, 7] (Fig. 3).

From an elementary analysis of I_{DS}–V_{GS} characteristics shown in Fig. 4, we concluded that the CuPc FETs have a threshold voltage V_{th} of about 15–20 V at V_{ds} = –80 V. Fig. 4(e) shows that the CuPc FET has a threshold voltage of about 50 V at V_{DS} = –80 V.

This can be attributed to the fact that the CuPc FET with an active layer thickness of 80 nm did not exhibit sufficient saturation at $V_{ds} = -80$ V, as can be confirmed from Fig. 2(e). Fig. 5 shows a comparison of CuPc FET characteristics of different CuPc thin films at $V_G = -80$ V. The channel length (L) and width (W) were 50 µm and 3 mm, respectively.
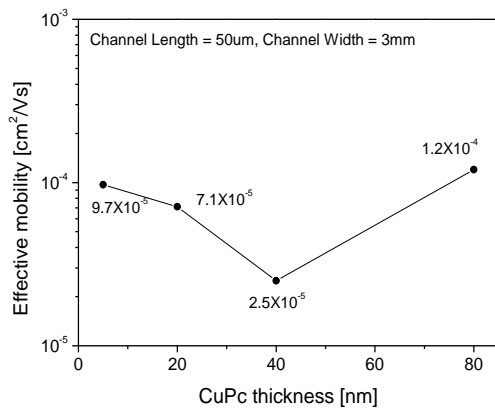

Fig. 3. Effective mobility of CuPc field-effect transistor devices with different thicknesses of CuPc thin films: (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 40 nm, and (e) 80 nm.

(a)

(b)

(c)

(d)

(e)
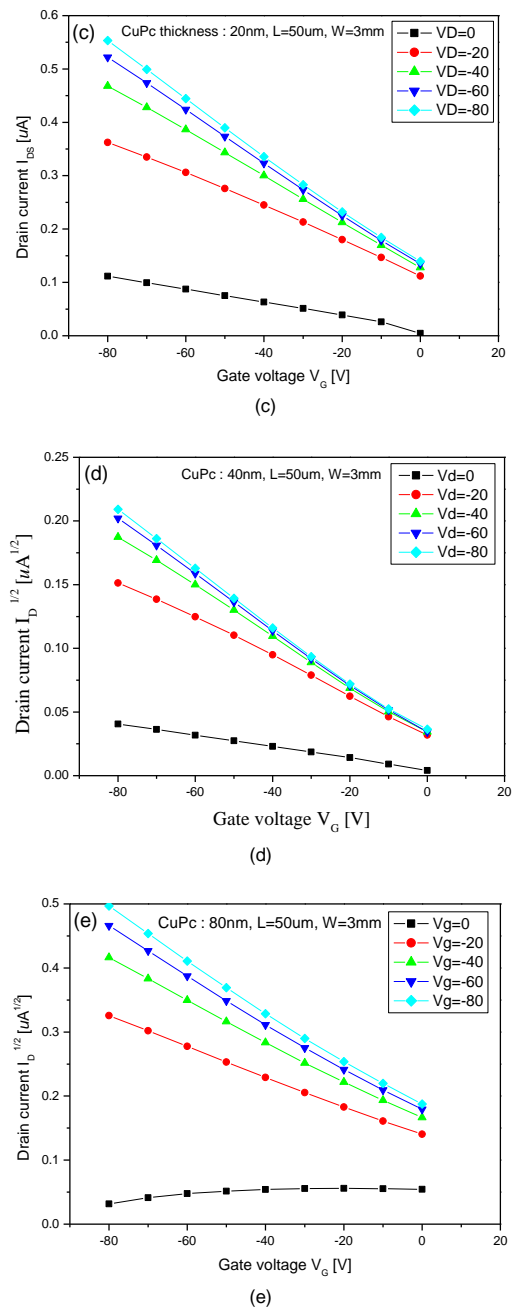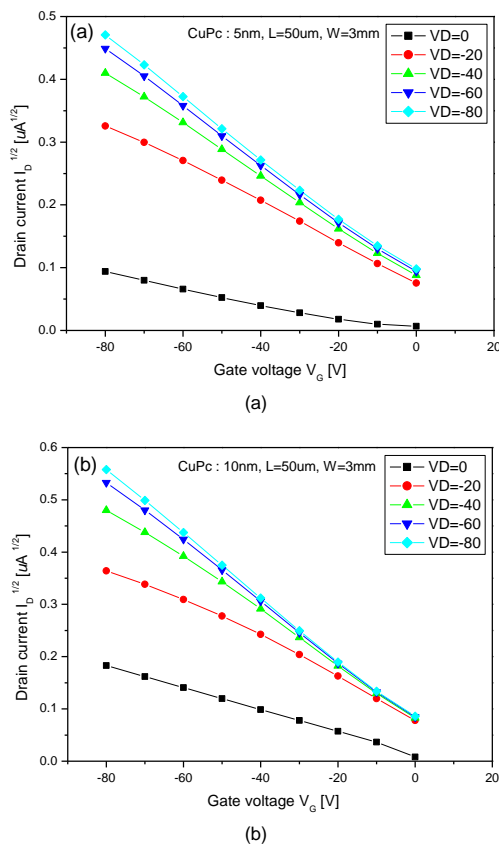
Fig. 4. Transfer characteristics of CuPc field-effect transistor devices with different thickness of CuPc thin films: (a) 5 nm, (b) 10 nm, (c) 20 nm, (d) 40 nm, and (e) 80 nm.

From Fig. 5, we observed that in the 10-nm CuPc FET device, the drain current was higher than that in the other devices. Note that we fabricated CuPc FET devices with different channel lengths of 30, 40, and 100 µm for estimating the electrical characteristics of CuPc FETs.

Fig. 6 shows the I–V characteristics of CuPc FETs with different channel lengths such as 30, 40, and 100 µm. The CuPc FET with a channel length of 40 µm exhibited typical
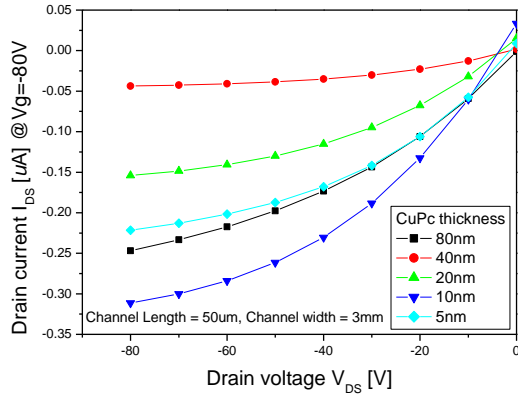
Fig. 5. Comparison of I_{DS} vs. V_{GS} of the CuPc field-effect transistor with different CuPc thin films at V_G = 80 V (channel length and width were fixed at 50 µm and 3 mm, respectively).

FET characteristics (Fig. 6(c)), and that with a channel length of 100 µm exhibited leakage current at a low drain voltage of less than 10 V. Further, the CuPc FET with a channel length of 30 µm did not have a saturation region at a high drain voltage, as shown in Fig. 6(a).

From Fig. 7, we infer that the threshold voltage did not change much for CuPc FETs having different channel lengths. Fig. 8 shows the C–V characteristics of the CuPc FETs, and the bias voltage in the region ranges from –40 V to 40 V at 43 Hz.

From Fig. 8, we infer that the capacitance of the samples increases with an increase in the negative bias voltage and approaches about 97 pF but does not saturate. In this case, the source and the drain electrodes were shorted, and the gate bias voltage V_G was applied with reference to the source voltage V_S.

These results were observed for top-contact FETs, and the C−V characteristics can be understood on the basis of a metal-insulator-semiconductor (MIS) capacitor. Further, the difference in the capacitance of the samples with varying channel lengths of the CuPc FETs corresponded to the amount of accumulated carriers at the interface between CuPc and SiO_2, which served as an insulating layer [3].

To understand the increase in the capacitance at the interface with bias voltage, the Maxwell–Wagner model was introduced to the top-contact CuPc FET devices.

The ideal image of the Maxwell–Wagner model was explained at the interface such as two dielectric materials in the FET device as shown in Fig. 9. Fig. 9 shows the ideal circuit for this model and the equivalent circuit for double-layered capacitance [3]. The material parameters of each dielectric and the circuit parameters of the equivalent circuit are as follows:

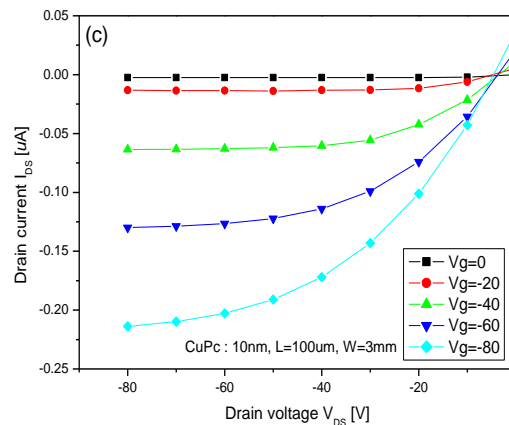$$G_1 = \sigma_1 \frac{s}{d_1}, \quad C_1 = \epsilon_1 \frac{s}{d_1}, \tag{3}$$

$$G_2 = \sigma_2 \frac{s}{d_2}, \quad C_2 = \epsilon_2 \frac{s}{d_2}. \tag{4}$$
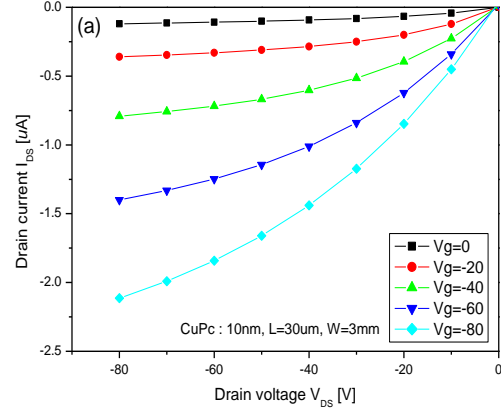
(a)
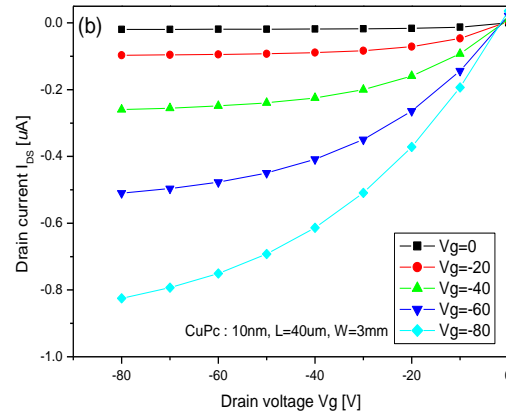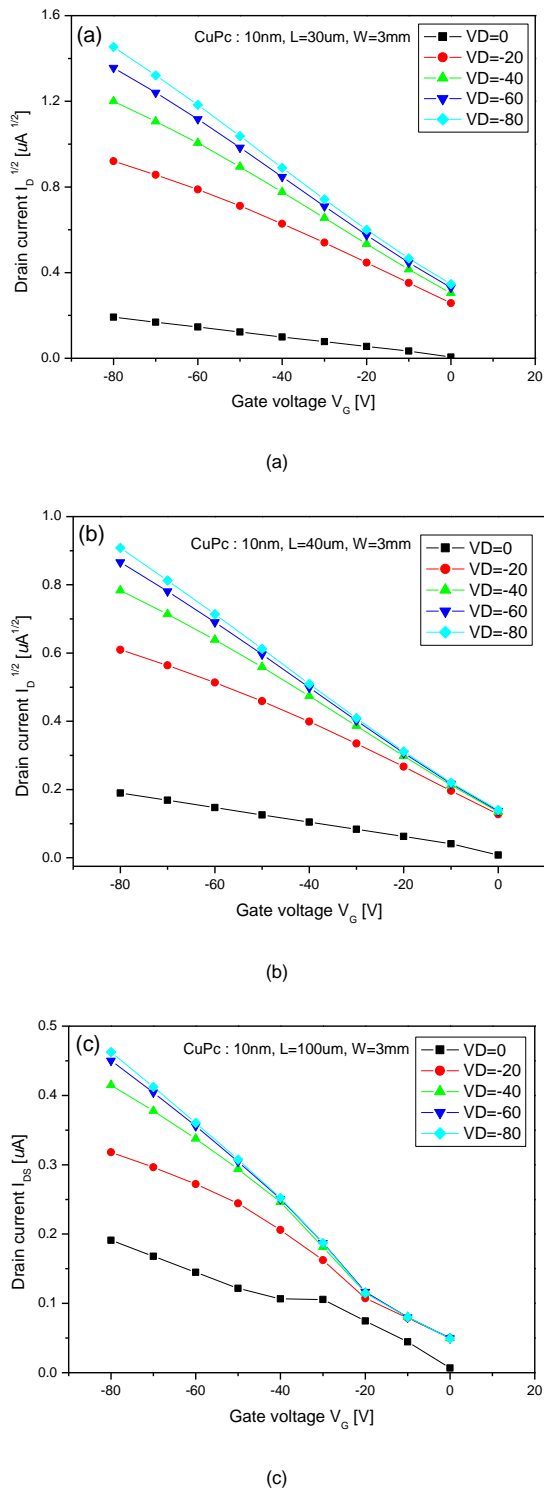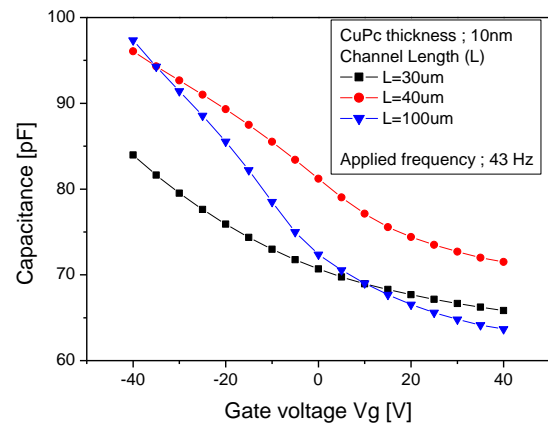

(b)

(c)

Fig. 6. I–V characteristics of the CuPc field-effect transistor device with different channel lengths: (a) 30 µm, (b) 40 µm, and (c) 100 µm.

(a)

(b)

(c)

Fig. 7. Transfer characteristics of CuPc field-effect transistor devices with varying channel lengths: (a) 30 μm, (b) 40 μm, and (c) 100 μm.

Fig. 8. C–V characteristics of CuPc field-effect transistor devices with varying channel lengths: (a) 30 μm, (b) 40 μm, and (c) 100 μm.
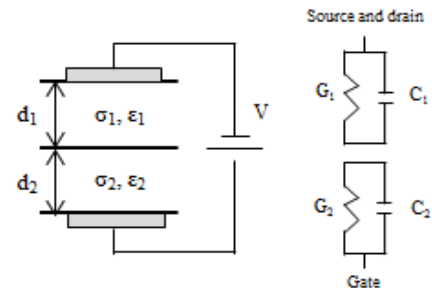
Fig. 9. Ideal circuit of the Maxwell–Wagner model and the equivalent circuit for double-layered capacitance.

IV. CONCLUSIONS

We fabricated the top-contact CuPc FETs with various CuPc thicknesses and different channel lengths. Further, we discussed the transistor properties of these top-contact CuPc FETs, such as the I–V and C–V characteristics. We noted that the increase in capacitance corresponded to the accumulation of carriers at the interface of the metal and CuPc materials.

It is important to understand the electrostatic phenomena at the interface between metal and organic materials in order to improve the organic FET device performance. We confirmed the amount of accumulated carriers as 97 pF at the interface between the CuPc layer and the SiO_2 layer from Fig. 8. Further, we calculated that the threshold voltage for varying CuPc thicknesses was about 15−20 V at $V_{DS} = -80$ V. Moreover, the carrier mobility of CuPc was calculated to be about 1.2×10^{-5} $cm^2V^{-1}s^{-1}$ for the 80-nm-thick CuPc FET.

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