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An Wideband GaN Low Noise Amplifier in a 3x3 mm^2 Quad Flat Non-leaded Package

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***Abstract*—An ultra-compact and wideband low noise amplifier (LNA) in a quad flat non-leaded (QFN) package is presented. The LNA monolithic microwave integrated circuit (MMIC) is implemented in a 0.25 μm GaN IC technology on a Silicon Carbide (SiC) substrate provided by Triquint. A source degeneration inductor and a gate inductor are used to obtain the noise and input matching simultaneously. The resistive feedback and inductor peaking techniques are employed to achieve a wideband characteristic. The LNA chip is mounted in the 3×3-mm^2 QFN package and measured. The supply voltages for the first and second stages are 14 V and 7 V, respectively, and the total current is 70 mA. The highest gain is 13.5 dB around the mid-band, and -3 dB frequencies are observed at 0.7 and 12 GHz. Input and output return losses (S_{11} and S_{22}) of less than -10 dB measure from 1 to 12 GHz; there is an absolute bandwidth of 11 GHz and a fractional bandwidth of 169%. Across the bandwidth, the noise figures (NFs) are between 3 and 5 dB, while the output-referred third-order intercept points (OIP3s) are between 26 and 28 dBm. The overall chip size with all bonding pads is 1.1×0.9 mm^2. To the best of our knowledge, this LNA shows the best figure-of-merit (FoM) compared with other published GaN LNAs with the same gate length.**

***Index Terms*—GaN, inductive peaking, low noise amplifier (LNA), quad flat non-leaded (QFN) package, resistive feedback, source degeneration**

I. INTRODUCTION

There has been a great deal of effort invested into incorporating GaN technology for power amplifiers in the transmitters of defense electronic radar systems, because it provides excellent radio frequency (RF) power density and capability at low and high frequencies. Traditionally, for a receiver in radar, GaAs technology has been widely used with a limiter to protect the receiver from high power jamming signals and transmitter leakage because of its low breakdown voltage, which increases the NF and cost [1]. Recently, GaN technology has also been considered as a good candidate for the LNA in the radar receiver because of its decent noise characteristic and excellent survivability, such that receivers using GaN LNA do not need RF limiters [2-4].

In addition, future RF systems such as frequency-agile systems and software-defined radios require high gain, high linearity, and low noise within the wide bandwidth. The GaN LNA with those RF characteristics is presented in this work. For wideband LNA design, common gate configuration and distributed architecture are among the most popular approaches. The transconductance of the common gate configuration is limited by input matching. The distributed architecture can achieve both wide bandwidth and high gain, but at the cost of large size and high power consumption [2]. In this work, the inductive peaking and resistive feedback techniques are employed to obtain a wideband characteristic.

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II. Circuit Analysis and Design

Fig. 1 shows a schematic of the GaN LNA. It consists of two stages. The degeneration inductor at the source (L_s) and the inductor at the gate (L_g) of M_1 are used to achieve low NF and return loss. The NF of the LNA without the resistive feedback can be expressed by [5]:

$$NF(\omega) \approx 1 + \frac{R_{par}}{R_{source}} + \frac{\gamma}{G_m R_{source}} \cdot \left| 1 - \left(\frac{\omega}{\omega_o} \right)^2 + j \frac{\omega}{\omega_o} \frac{1}{Q_{in}} \right|^2 \quad (1)$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_s)(C_{gs} + C_{gd})}}$$

$$Q_{in} = \frac{\omega_o (L_g + L_s)}{R_{source} + R_{par}}$$

where R_{source} is the output resistance of the source, R_{par} is the parasitic resistance at the input, C_{gs} is the gate-source capacitance, C_{gd} is the gate-drain capacitance, G_m is the transconductance of M_1, and γ is the process parameter. R_{source} is 50 Ω because antennas and filters with input and output impedances of 50 Ω are followed by LNAs in RF systems. Since L_g is designed with the lossy on-chip spiral inductor, R_{par} can be considered as the parasitic series resistance of L_g. All of the design parameters for noise and input matching were found with Eq. (1) as well as the circuit simulation: G_m = 81 mA/V, C_{gs} = 0.52 pF, C_{gd} = 0.04 pF, L_g = 0.6 nH, L_s = 0.24 nH, and γ = 0.6.

The resistive feedback network consisting of the feedback resistor (R_f) and DC blocking capacitor (C_f) between the input and output of the first stage is employed not only to broaden the input matching, but also to flatten the gain response to increase the 3-dB bandwidth. However, the resistive feedback also increases the overall NF by about 1 dB across the frequency range from 1 to 12 GHz in the simulation.

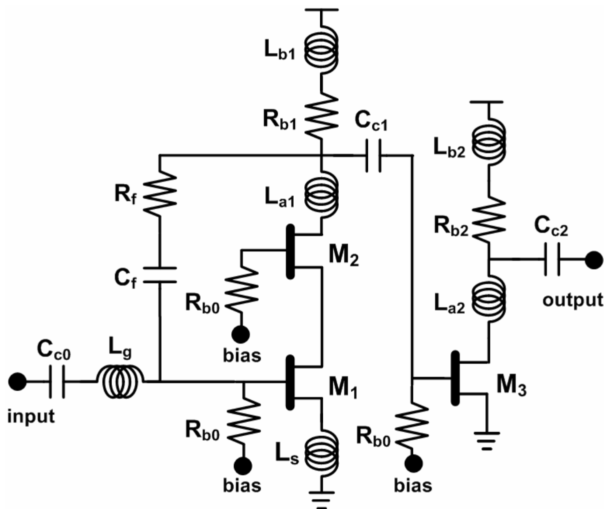

Fig. 1. Simplified schematic of the GaN LNA.

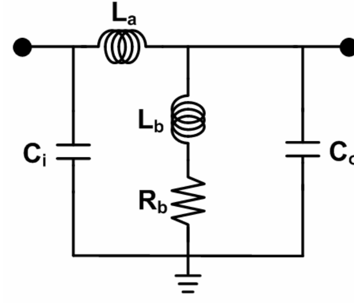

Fig. 2. Series and shunt inductive peaking circuit.

In addition to the resistive feedback, series and shunt inductive peaking techniques are used to increase the bandwidth. Fig. 2 shows a simplified circuit of the peaking techniques. Combined with C_i and C_o, the peaking responses are generated in series with L_a, and in shunt with L_b and R_b. The configuration can be modeled as an impedance system with four poles and one zero. The transfer function can be expressed by [6]:

$$Z_T = \frac{H(s+A)}{s^4 + As^3 + Bs^2 + Cs + D} \quad (2)$$

$$H = \frac{1}{[n(1-n)m_2]}, A = \frac{1}{m_1}, B = \frac{m_1 + (1-n)m_2}{[n(1-n)m_1 m_2]}$$

$$C = D = \frac{1}{[n(1-n)m_1 m_2]}$$

$$m_1 = \frac{L_a}{R_b^2 (C_i + C_o)}, m_2 = \frac{L_b}{R_b^2 (C_i + C_o)}, n = \frac{C_o}{C_i + C_o}$$

where the input and output capacitances (C_i and C_o) represent the output and input impedances of the previous and following stages, respectively.

Fig. 3 shows the peaking responses of the first and second stages. The normalized gain of a GaN unit device drops as the frequency increases, while those of the peaking circuits are boosted at high frequencies. The first stage peaking circuit design focuses mainly on the high-frequency peaking. A cascode configuration is employed not only to suppress the Miller effect, but also to reduce

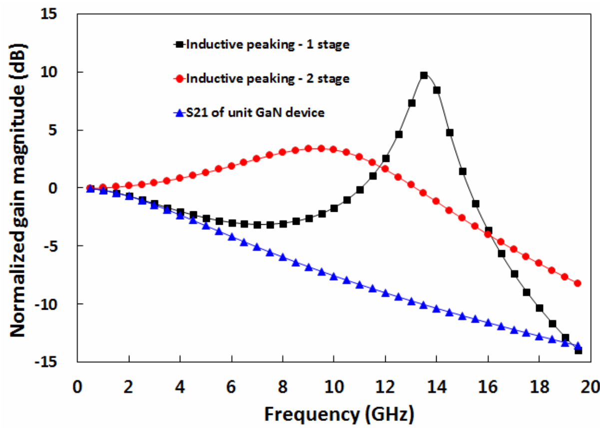

Fig. 3. Normalized gains of active GaN unit device, and those of passive inductive peaking circuits of the first stage and the second stage.

C_i to cause peaking at a higher frequency. The peaking circuit of the first stage is designed with the following parameters: C_i = 0.15 pF, C_o = 0.45 pF, L_{a1} = 0.2 nH, L_{b2} = 1.2 nH, and R_{b1} = 70 Ω. However, for the second stage peaking circuit design, the overall gain flatness and output matching with a load resistance of 50 Ω instead of C_o are critical issues. The peaking circuit of the second stage is designed with the following parameters: C_i = 0.3 pF, L_{a2} = 0.2 nH, L_{b2} = 0.7 nH, and R_{b2} = 120 Ω.

III. IMPLEMENTATION AND MEASUREMENTS

The GaN LNA is simulated with the Advanced Design System (ADS) circuit simulator and the Electro-Magnetic eXtractor (EMX) full-wave simulator, and implemented using a Triquint 0.25μm GaN IC process on a 100μm SiC substrate with three metal layers. The GaN device, which has a width of 75μm and eight fingers, is chosen as the unit device. The unity current gain frequency (f_T) of this FET is approximately 30 GHz. The RF models of the capacitors and inductors are provided by the design kit. The capacitors are metal-insulator-metal types and the inductors are rectangular spiral types. The initial LNA design starts out using the models in the design kit; however, EM simulations are performed for all of the passive elements, including the capacitors, inductors, interconnection lines and bonding pads in order to reduce the overall size. Fig. 4 shows a photograph of the GaN LNA MMIC chip in a 3×3 mm^2 QFN package. The chip size, including all of the bonding pads, is 1.1×0.9 mm^2.

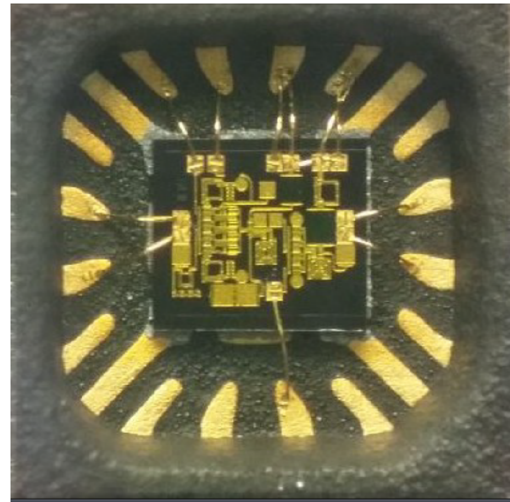

Fig. 4. Photograph of GaN LNA in QFN package.

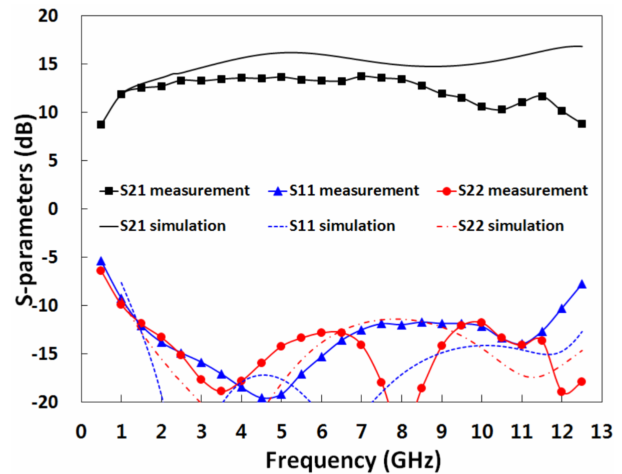

Fig. 5. Measurement and simulation results of S-parameters of GaN LNA.

Fig. 5 shows the small signal measurement results of the S-parameters obtained using an Agilent 8510C network analyzer. S_{11} and S_{22} are less than -10 dB from 1 to 12 GHz. The maximum value of S_{21} around the mid-band is 13.5 dB. The 3 dB-bandwidth is from 0.7 to 12 GHz. Inductive peaking is observed around 11.5 GHz, which was designed to be 14 GHz. The peaking frequency is reduced by 2.5 GHz due to the parasitic components of the layout. Fig. 6 shows the NF results measured using an Agilent N8975A noise figure analyzer and an N4002A noise source. The minimum NF of 3.5 dB is shown at 5 GHz, and it goes up by about 1.5 dB at the ends of the bandwidth. Compared with the simulation results, the measured NFs increase by 1.2−1.5 dB across

Table 1. Performance Comparison with Recently Published 0.25 MM GaN-Based LNA

Ref.	Freq. (GHz)	BW[1] (GHz)	NF (dB)	S_{21} (dB)	OIP3 (dBm)	P_{DC}[2] (mW)	Chip size (mm^2)	FoM (1/ mm^2)	Type
[2]	2 – 18*	16	3.3 – 4.7	22.5 – 24.1	29	1200	11.02	0.23	MMIC
[3]	0.5 – 3**	2.5	1.5 – 1.9	32 – 34	34 – 38	3000	8.75	0.45	Package (7×7 mm^2)
[4]	5 -10**	5	1.5 – 2.2	22.5 – 25.2	29 – 29.6	1000	3.12	0.81	Package (4×4 mm^2)
This work	1 – 12**	11	3.5 – 5.5	10.5 – 13.5	26 – 28	735	0.99	1.35	Package (3×3 mm^2)

*$S_{11}(S_{22})$<-8.5 dB, **$S_{11}(S_{22})$<-10 dB, [1]Bandwidth, [2]DC power consumption

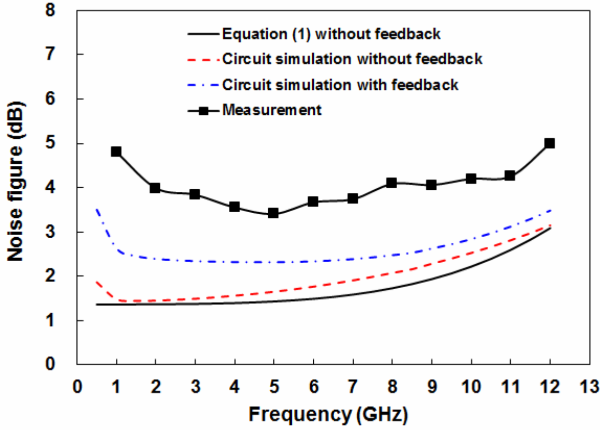

Fig. 6. Measurement, simulation, and calculation results of NFs of GaN LNA.

the bandwidth. The large signal characteristic, OIP3 (the output-referred third-order intercept point), is measured using a ROHDE & SCHWARZ SMBV 100A vector signal generator and a FSV signal analyzer with two tones having frequency difference of 10 MHz. The measured OIP3s across the bandwidth are between 26 and 28 dBm. Table 1 compares the results with those obtained using other GaN LNAs published in the literature. To make a fair comparison, the FoM (figure-of-merit) is defined as

$$\mathrm{FoM} = \frac{G_{max}[\mathrm{dB}] \cdot \mathrm{BW}[\mathrm{GHz}] \cdot \mathrm{OIP3}_{max}[\mathrm{mW}]}{\mathrm{NF}_{min}[\mathrm{dB}] \cdot f_T[\mathrm{GHz}] \cdot P_{DC}[\mathrm{mW}] \cdot \mathrm{size}[\mathrm{mm}^2]} \quad (3)$$

where G_{max}, $OIP3_{max}$, NF_{min} are maximum S_{21}, maximum OIP3, and minimum NF across the bandwidth. This proposed FoM is based on the FoMs in [5] and [7]. In LNA design, if devices have high unity current gain frequency (f_T), low NF can be easily achieved because NF is inverse proportional to f_T [8], so that f_T is at the denominator in the FoM. Because of the high cost of GaN IC technology, the size of chip die is added in the FoM. In this work, the FoM is improved to make fair comparison by including linearity parameter, OIP3, which was not considered in [5] and [7]. When small DC power is used, obviously FoM is high even if OIP3 is low. Therefore, the FoM formula Eq. (3) includes OIP3 as well as P_{DC}.

The GaN distributed amplifier in [2] provides extremely wide bandwidth with decent NFs, but its size and DC power consumption are very large. The size is 11 times larger, and the DC power consumption is 63% higher than in this work. Most GaN LNAs published in the literature are MMIC chips, not in a package. Even if the parasitics from packages and bondwires easily affect the wideband LNA performance, only a few GaN LNAs in a package have been reported [3, 4]. The GaN LNA in [3] shows low NF, high gain, and high OIP3, and it consumes a very large amount of DC power. The bandwidth is very narrow, and the sizes of the package and chip are much larger than in this work. Recently, Triquint (the GaN IC foundry provider for this work) has published their own GaN LNA, demonstrating high gain and low NF [4]. However, the bandwidth is 55% smaller, the DC power consumption is 36% larger, and the chip size is 3.2 times larger. Therefore, the FoM of this work is better than for other GaN LNAs with the same gate length.

IV. CONCLUSIONS

An ultra-compact wideband GaN LNA in a QFN package is presented. The inductors at the source and gate terminals are incorporated for input and noise matching at the same time. The inductive peaking technique, cascode configuration, and resistive feedback are employed to extend the bandwidth. The LNA shows the lowest DC power consumption, the smallest chip size, and very low NFs across a wide bandwidth as compared

with other published GaN LNAs with the same gate length.

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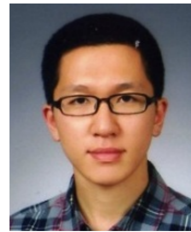

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