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A 40-W Flyback Converter with Dual-Operation Modes for Improved Light Load Efficiency

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***Abstract*—A flyback converter operates with either pulse width modulation (PWM) or pulse frequency modulation (PFM) control scheme depending on the load current. At light load condition, PFM control is employed to reduce the switching frequency and thereby minimize the switching power loss. For heavier load, PWM control is used to regulate the output voltage of the flyback converter. The flyback controller has been implemented in a 0.35 μm BCDMOS process and applied to a 40-W flyback converter. The light-load power efficiency of the flyback converter is improved up to 5.7-% comparing with the one operating with a fixed switching frequency.**

***Index Terms*—Flyback converter, frequency reduction, power efficiency, pulse width modulation (PWM), pulse frequency modulation (PFM), BCDMOS**

I. INTRODUCTION

When galvanic isolation is required for user safety, the flyback topology is widely used in various applications [1]. Like other switching converters, power efficiency is one of the most important performance metrics for a flyback converter. Power loss determining the power efficiency can be classified as either conduction or switching loss [2]. The conduction loss becomes larger and dominates the power efficiency for higher output current while the power efficiency at light load is dominated by the switching loss.

For better power efficiency at light load, the switching loss has to be reduced in some way. If power devices are switched on and off only when it is required to supply power to load, unnecessary switching can be avoided, reducing the switching loss [3-5]. This burst mode operation, however, may cause large ripple on the output voltage level. If the voltage swing of the driving signal of power transistors is reduced for smaller load current, the switching loss can be reduced at light load [6-8]. However, the reduced swing of driving signal results in larger on-resistance of power transistors and therefore higher conduction loss. Then, the light load power efficiency may not be improved at all. With pulse frequency modulation (PFM), the switching frequency is decreased at light load condition, meaning lower switching power loss and improved light load power efficiency [9, 10]. At heavy load condition with PFM control, however, the switching frequency may be too large, which results in excessively large switching power loss.

This paper describes a flyback converter which adaptively employs either PFM or pulse width modulation (PWM) control according to the load condition. The operation principle of the proposed flyback converter is described in Section II and the circuit implementation details are given in Section III. The experimental results are provided in Section IV and Section V concludes this paper.

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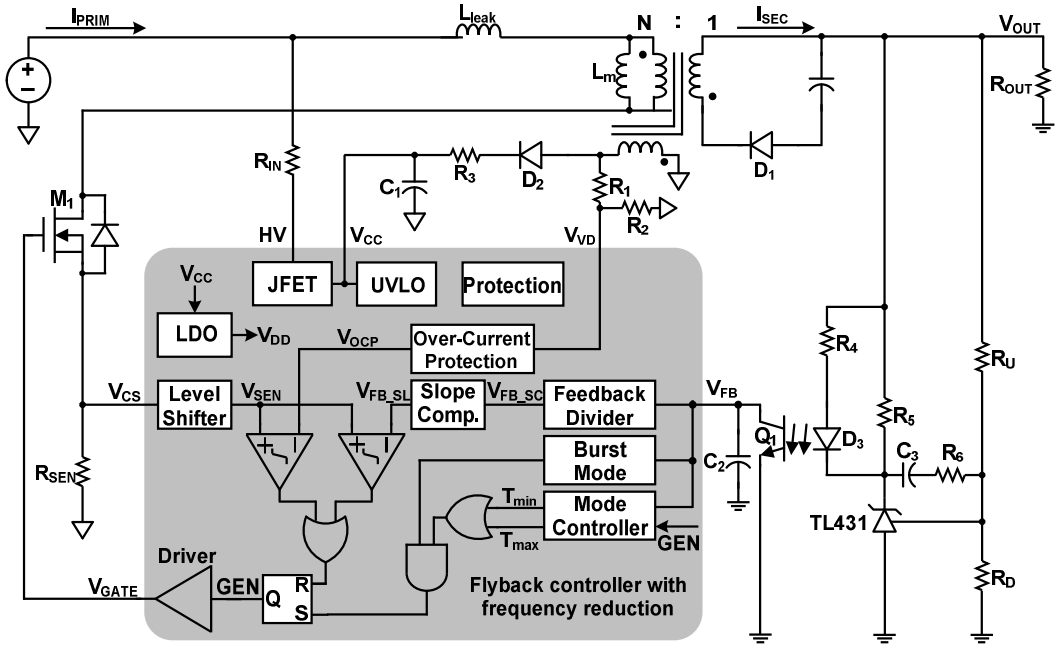


Fig. 1. Flyback converter with dual-mode PFM and PWM controller.

II. OPERATION PRINCIPLE

Fig. 1 shows the block diagram of the flyback converter which may operate with either the PFM or PWM control. When the input V_{IN} is applied, the supply voltage V_{CC} is initially charged through the junction field effect transistor (JFET). Once the supply voltage V_{CC} becomes sufficiently high, its voltage level is maintained by the switching operation of the flyback converter instead of the JFET.

The operation mode of the flyback converter is determined based on the feedback voltage V_{FB} which is controlled by the feedback network consisting of the opto-coupler and the shunt regulator (TL431). For smaller load current, the output voltage V_{OUT} rises and therefore the current flowing through the diode D_3 increases as well. Large current flowing through the diode D_3 is reflected to the optically coupled transistor Q_1, which pulls down the feedback voltage V_{FB}. Therefore, the feedback voltage V_{FB} is proportional to the load current.

Fig. 2 shows the switching frequency versus the feedback voltage. For heavy load, V_{FB} is larger than V_{FR_S} and the switching frequency is fixed to be 65-kHz while the output voltage is regulated by the PWM control. For lighter load ($V_{FR\_E} < V_{FB} < V_{FR\_S}$), the switching

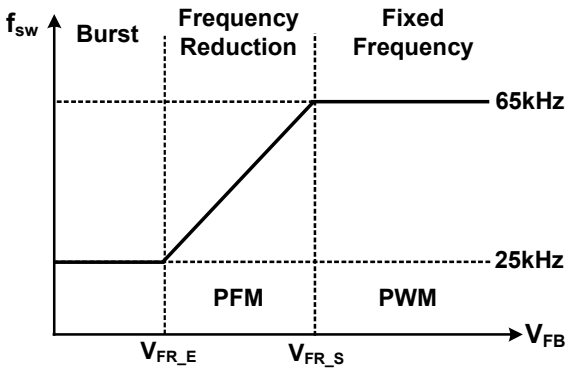


Fig. 2. Operation mode of the flyback converter.

frequency is reduced depending on the feedback voltage V_{FB} to reduce the switching power loss, that is, the output voltage is regulated by PFM control while the switch on-time is constant. For extremely light load, V_{FB} becomes smaller than V_{FR_E} and the converter operates with burst-mode.

It is to be noted that the switching of the operation mode to and from the PWM and PFM mode is performed softly without any switch being turned on or off depending on the operation mode. Therefore, we do not need to provide any hysteresis at the boundary of the two operation modes. Even if there is any fluctuation on the feedback voltage V_{FB}, the switching frequency is continuously controlled between 25-kHz and 65-kHz as

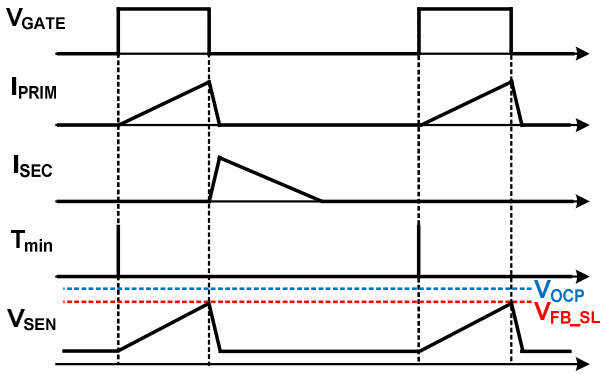


Fig. 3. Operational waveforms of the flyback converter.

shown in Fig. 2.

The operation waveforms are shown in Fig. 3. The primary side transistor M_1 is turned on by the pulse T_{min} and therefore the switching frequency is determined by T_{min}. When the primary side transistor M_1 is turned on, that is, V_{GATE} is HIGH, the primary side current I_{PRIM} increases linearly and therefore the current sensor output V_{CS} increases linearly as well. The current sensor output V_{CS} is level-shifted to V_{SEN} which is compared with V_{FB_SL} and V_{OCP} to determine the turn-off timing of the primary side transistor M_1 and to prevent over-current flow, respectively. If V_{SEN} reaches V_{FB_SL}, the switch is turned off. At PWM mode, the voltage level of V_{FB_SL} is linearly proportional to the feedback voltage V_{FB}. Therefore, for higher V_{FB} and thus for higher load current, the turn-on time of the primary side transistor M_1 becomes longer and PWM regulation is performed because the period of the signal T_{min} turning on M_1 is fixed. At PFM mode, the voltage of V_{FB_SL} is fixed and independent of the load current. Because V_{FB_SL} is fixed, the turn-on time of the primary side transistor is constant. For PFM, the frequency of the signal T_{min} is controlled according to the feedback voltage V_{FB}. If the period of T_{min} becomes too long, the primary side transistor is turned on by the T_{max} signal to force the switching frequency to be higher than 25-kHz.

III. Circuit Implementation

All the circuit blocks of the flyback controller except the driver are powered by the linear regulator output V_{DD} which is 5-V. The driver is powered by both V_{DD} and V_{CC} as will be described below.

1. Mode Controller

The operation mode of the flyback converter is controlled by the mode controller shown in Fig. 4 which generates the T_{min} and T_{max} signals appropriately. Based on the feedback voltage V_{FB}, the reference generator provides V_{Tmin} whose voltage level determines the frequency of the oscillator. For small V_{FB}, the transistor M_1 is turned on while the transistor M_2 is turned off, activating only the loop 1. Then, V_{Tmin} is given as;

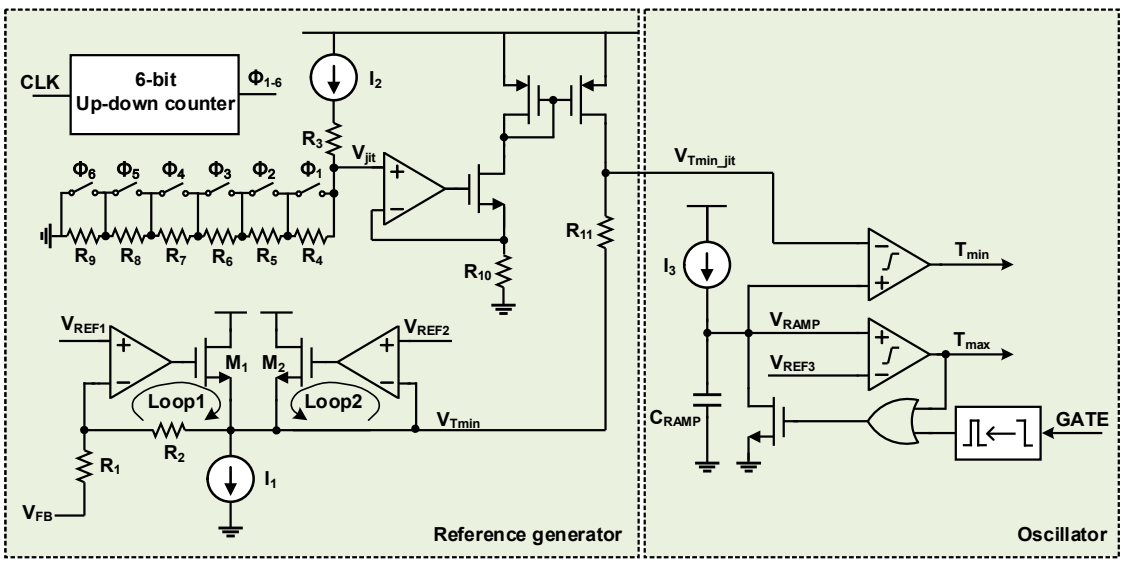


Fig. 4. Mode controller.

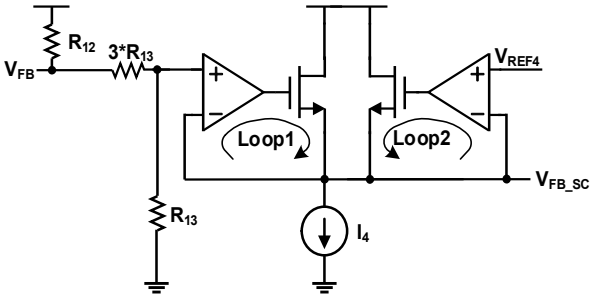


Fig. 5. Feedback divider.

$$V_{T\min} = \left(1+\frac{R_2}{R_1}\right)V_{REF1} - \frac{R_2}{R_1}V_{FB} \quad (1)$$

$$V_{FR\_S} = \left(1+\frac{R_1}{R_2}\right)V_{REF1} - \frac{R_1}{R_2}V_{REF2} \quad (2)$$

In the Eq. (1), we can see V_{Tmin} decreases as the feedback voltage V_{FB} and thus the load current increase. Therefore the frequency of the oscillator varies according to the load current, allowing the PFM operation of the flyback converter. If V_{FB} becomes larger than V_{FR_S} whose value is given in the Eq. (2), the transistor M_2 is turned on and the loop 2 is activated. Then, V_{Tmin} is clamped to V_{REF2}, which results in the fixed frequency of the oscillator and the PWM control of the converter. Therefore, V_{Tmin} is changed or clamped by the loop 1 or loop 2, respectively according to the feedback voltage V_{FB}, which enables the soft transition between the two operation modes, that is, PFM and PWM.

In order to reduce electro-magnetic interference (EMI), the oscillation frequency is jittered by modulating V_{Tmin}. With the 6-bit up-down counter and switchable resistor network, a 280-Hz triangular profile is added to V_{Tmin} to get V_{Tmin_jit}.

2. Feedback Divider

The feedback divider shown in Fig. 5 generates the divided-by-four value of the feedback voltage V_{FB} and fixed voltage level in the PWM and PFM operation modes, respectively. When V_{FB} is smaller than $4\times V_{REF4}$, the loop 1 is deactivated and V_{FB_SC} is equal to V_{REF4}. Then, the peak value of V_{SEN} is independent of the load current and the switch on-time becomes constant. With the constant switch on-time, the PFM control regulates the output voltage. For V_{FB} larger than $4\times V_{REF4}$, the loop

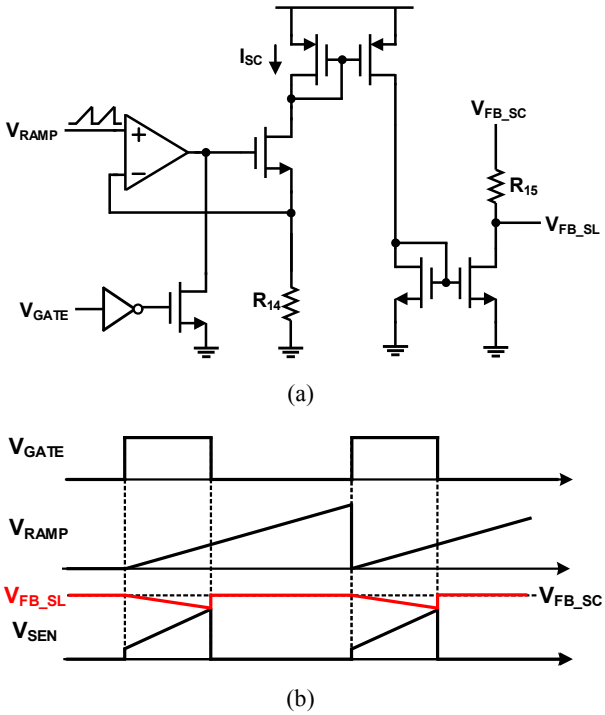


Fig. 6. Slope compensation (a) circuit, (b) its timing diagram.

1 becomes activated and V_{FB_SC} is $0.25\times V_{FB}$. With V_{FB_SC} proportional to V_{FB}, the peak value of V_{SEN} is controlled by the load current and the PWM control regulates the output voltage. Because the boundary value of V_{FB} between the PWM and PFM operation modes has to be equal for the mode controller and feedback divider, the reference voltages V_{REF1}, V_{REF2}, and V_{REF4} have the following relationship;

$$(1+\frac{R_1}{R_2})V_{REF1} - \frac{R_1}{R_2}V_{REF2} = 4V_{REF4} \quad (3)$$

3. Slope Compensation

In order to avoid the instability of the current-mode control for over 50-% duty cycle, the slope compensation circuit shown in Fig. 6(a) is employed. The ramp signal V_{RAMP} from the oscillator in Fig. 4 is utilized to get the slope compensating current I_{SC}. From the output V_{FB_SC} of the feedback divider, the slope compensating IR-drop $I_{SC}\times R_{15}$ is subtracted to generate V_{FB_SL}. When V_{GATE} is HIGH, V_{FB_SL} ramps down and is compared with V_{SEN} and therefore the slope is compensated as shown in Fig. 6(b). When V_{GATE} is LOW, V_{FB_SL} returns to V_{FB_SC}

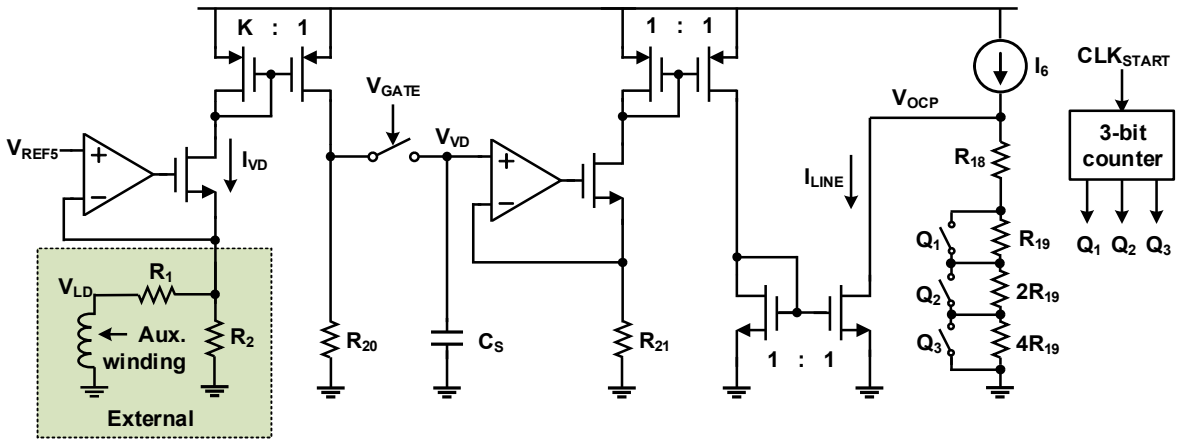


Fig. 7. Over-current protection circuit with soft-start capability.

because the current I_{SC} is forced to be zero.

4. Over-Current Protection

The input voltage of the flyback converter ranges from 90-V_{RMS} to 230-V_{RMS} and the over-current protection (OCP) level has to be controlled according to the input voltage level to limit the maximum deliverable power. Fig. 7 shows the OCP circuit that controls the OCP level according to the line input level. When the primary side transistor is turned on, the voltage level V_{LD} across the auxiliary winding becomes negative whose absolute value is proportional to the line input level. Because the current I_{VD} is proportional to the difference between V_{REF5} and V_{LD}, the voltage V_{VD} sampled on the capacitor C_S by the gate driving signal V_{GATE} is also proportional to the line input level. The voltage V_{VD} is converted to the current I_{LINE} which is subtracted from I_6 to generate the OCP reference level V_{OCP}. Therefore, the OCP level is inversely proportional to the line input level, ensuring the same maximum deliverable power regardless of the line input level. For the soft start, the OCP level is slowly increased at power-up by the switchable resistor network controlled by the 3-bit counter clocked by the 300-Hz clock CLK_{START}.

5. Driver

Fig. 8 shows driver which generates the gate driving signal V_{GATE} for the primary side transistor. When the *GEN* becomes HIGH, the gate voltage of the transistor M_3 is boosted from its bias level because of the coupling

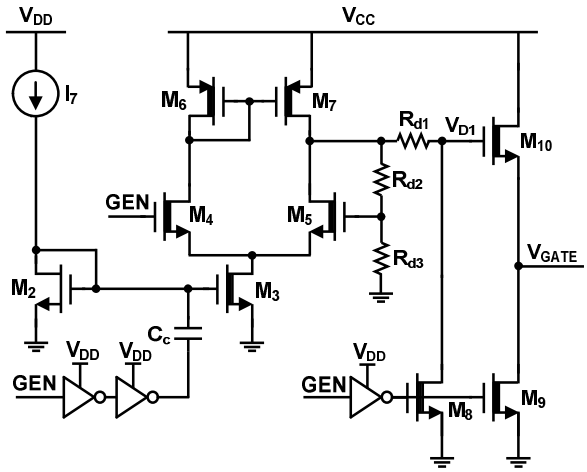


Fig. 8. Dirver.

capacitor C_C. It improves the rising time of V_{GATE} by temporarily increasing the current of M_3. When *GEN* is LOW, the transistor M_9 is turned on and V_{GATE} is pulled down. The transistors M_3~M_{10} are high voltage devices while the other transistors are normal devices. The nMOS-nMOS driver structure is used here because the supply voltage V_{CC} of the final driving transistors M_9 and M_{10} can rise up to 25-V. With conventional pMOS-nMOS driver structure, the pull-up pMOS transistor will be exposed to an excessive over-voltage stress.

IV. Experimental Results

The flyback controller has been implemented in a 0.35-μm BCDMOS process and the chip microphotograph is shown in Fig. 9. The size of the flyback controller IC is 2.21-mm^2. The flyback controller is

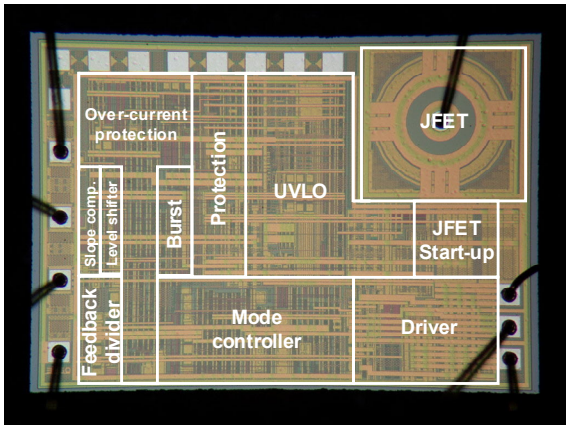


Fig. 9. Chip microphotograph of the flyback controller.

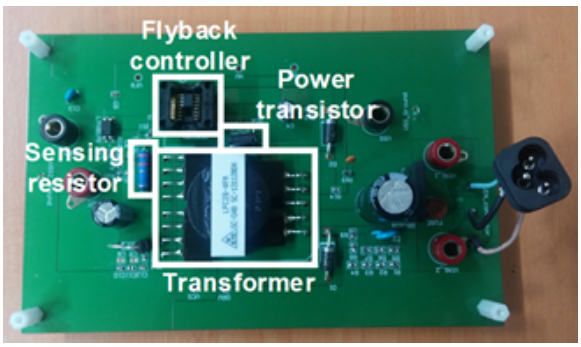


Fig. 10. Flyback converter employing the proposed flyback controller.

applied to the 40-W flyback converter shown in Fig. 10 which has 90~230-V_{RMS} input and 12-V output.

Fig. 11 shows the measured switching frequency of the flyback converter with the proposed controller as a function of the load current. The flyback converter operates with 66.2-kHz switching frequency for the load current larger than 1.3-A load current. For smaller load current, the switching frequency decreases and is fixed to be 25.6-kHz for the load current smaller than 0.5-A. Fig. 12 shows the measured waveforms when the line input is 90-V_{RMS}. It can be seen the switching frequency is reduced from 66.2-kHz to 25.6-kHz when the load current is decreased from 1.3-A to 0.3-A, showing the frequency reduction is working properly.The power efficiency of the flyback converter is measured for different line input. In order to see the effectiveness of the proposed flyback controller, the same devices are used to build a flyback converter with the conventional fixed frequency PWM controller. The conventional fixed

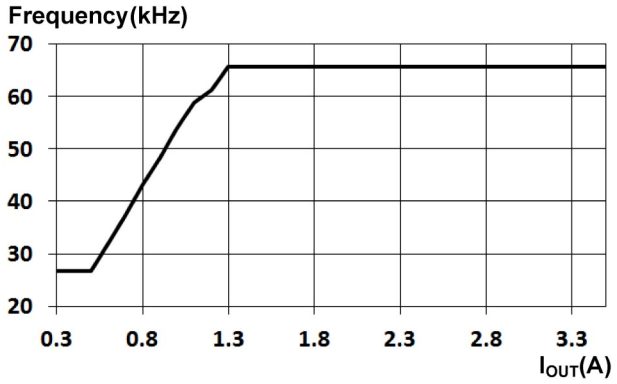
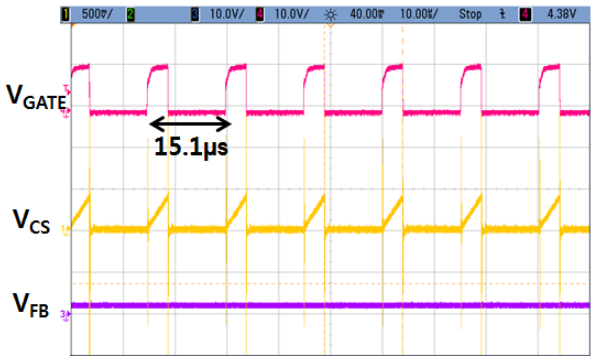
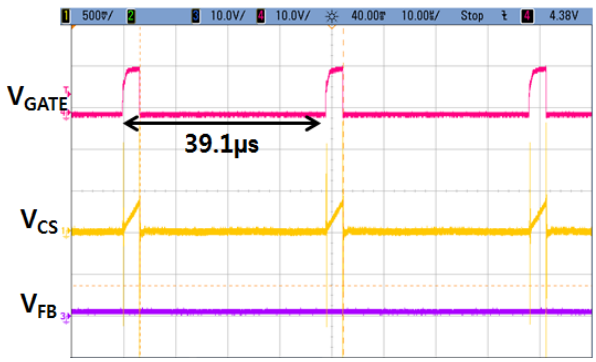


Fig. 11. Switching frequency of the flyback converter according to the load current.



(a)



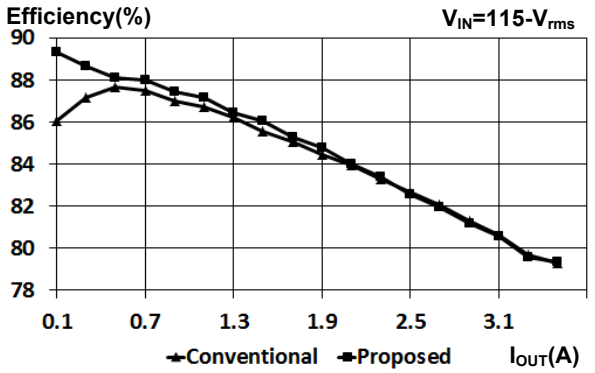
(b)

Fig. 12. Measured waveforms of the flyback converter with the Proposed controller for (a) I_{OUT}=1.3-A and V_{IN}=90-V_{RMS}, (b) I_{OUT}=0.3-A and V_{IN}=90-V_{RMS}.

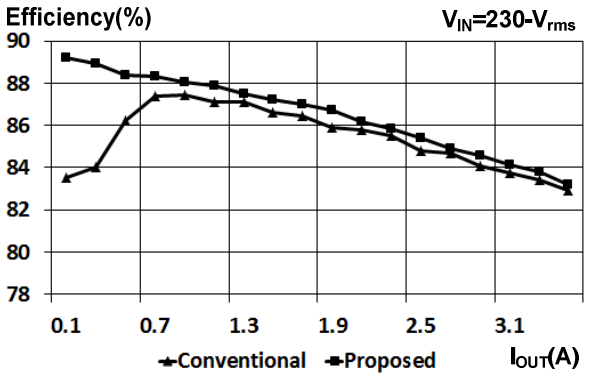
frequency PWM controller has 65-kHz fixed switching frequency and enables the burst mode function at light load condition. The maximum power level is set to be same for both the conventional and proposed controllers to ensure the fair comparison. Fig. 13 compares the power efficiency of the flyback converters with the

Table 1. Performance summary of the flyback converter

	This work	[3]	[4]	Unit
Input voltage	90~230	400	90~265	V_{RMS}
Output voltage	12	47	16.5	V
Maximum output current	3.5	1.6	3.6	A
Switching frequency	25~65	60	65	kHz
Primary side inductance	500	-	-	μH
Primary winding turns	33	-	-	
Secondary winding turns	7	-	-	
Auxiliary winding turns	10	-	-	
Power efficiency	89.2 (3-% load condition)	84 (6-% load condition)	83.5 (3.3%-load condition)	%



(a)



(b)

Fig. 13. Efficiency of the flyback converter when V_{IN} is (a) 115-Vrms, (b) 230-V_{RMS}.

conventional and proposed flyback controllers. Because the proposed controller forces the flyback converter to operate with the PFM mode at light load condition, it shows 5.7-% higher power efficiency when the load current is 0.1-A at 230-V_{RMS} input.

Table 1 summarizes the performance of the flyback converter with the proposed controller and compares it with previous works.

V. CONCLUSION

A flyback converter is described whose light load efficiency is improved by reducing the switching frequency with PFM control for light load. For heavier load, the output of the flyback converter is regulated by PWM control. The proposed flyback controller has been implemented in a 0.35-μm BCDMOS process and applied to a 40-W flyback converter. The experimental results show the light load power efficiency is improved up to 5.7-%.

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