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Effect of Annealing Time on Electrical Performance of SiZnSnO Thin Film Transistor Fabricated by RF Magnetron Sputtering

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Thin film transistors (TFTs) with amorphous 2 wt% silicon-doped zinc tin oxide (a-2SZTO) channel layer were fabricated using an RF magnetron sputtering system, and the effect of post-annealing treatment time on the structural and electrical properties of a-2SZTO systems was investigated. It is well known that Si can effectively reduce the generation of oxygen vacancies. However, it is interesting to note that prolonged annealing could have a bad effect on the roughness of a-2SZTO systems, since the roughness of a-2SZTO thin films increases in proportion to the thermal annealing treatment time. Thermal annealing can control the electrical characteristics of amorphous oxide semiconductor (AOS) TFTs. It was observed herein that prolonged annealing treatment can cause bumpy roughness, which led to increase of the contact resistance between the electrode and channel. Thus, it was confirmed that deterioration of the electrical characteristics could occur due to prolonged annealing. The longer annealing time also decreased the field effect mobility. The a-2SZTO TFTs annealed at 500℃ for 2 hours displayed the mobility of 2.17 cm^2/Vs. As the electrical characteristics of a-2SZTO annealed at a fixed temperature for long periods were deteriorated, careful optimization of the annealing conditions for a-2SZTO, in terms of time, should be carried out to achieve better performance.

Keywords: RF magnetron sputtering, Roughness, Contact resistance, Prolong annealing treatment, Amorphous structure

1. INTRODUCTION

Amorphous hydrogenated silicon (a-Si:H) is currently the representative material used in thin film transistors (TFTs) technology. However, this material exhibits several drawbacks. Perhaps significantly, the a-Si:H channel mobility is restricted to approximately 1 cm^2/Vs. Another drawback is that it is difficult to apply large-area display, as a-Si:H is not uniform over a large area. On the other hand, TFTs fabricated using amorphous oxide semiconductors (AOSs) have shown high performance for high functional electrical devices. Amorphous oxide semiconductor-based TFTs have been studied as next generation channel materials because of their high mobility and transparency.

Recently, indium-gallium-zinc-oxide (IGZO) has been considered as one of the most promising channel materials because of its high carrier mobility, low processing temperature, and excellent transparency compared with a-Si based TFTs [1-3]. However, the large amount of indium in the IGZO channel has the disadvantages of high cost and toxicity. Thus, indium-free amorphous oxide-based channel materials have been examined, such as zinc-tin-oxide (ZTO). However, the stability of ZTO TFT must be improved for application to electronic devices because the threshold voltage is changed after bias stress. The instability of the ZTO TFTs is mainly attributed to the carrier trapping in the trap state on the interface of the active layer. This behavior can cause degradation of the electrical properties. A recent report determined that doping with group

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IV elements that have high oxygen binding energy in ZTO semiconductor materials, such as Hf, Zr and Si, can allow improvement of the stability under bias stress [4,5]. These materials are considered to play important roles in the passivation of defects by binding with oxygen [6].

In the present study, amorphous 2 wt% Si-doped ZnSnO (a-2SZTO) TFTs were fabricated by RF magnetron sputtering. Silicon can change the carrier concentration and easily be combined with oxygen in Zn-based TFTs [7]. Silicon was used as an oxygen vacancy suppressor in order to improve the stability. However, it is interesting to note that high temperature annealing made the a-2SZTO systems worse. In this paper, we observed degradation of the performance of a-2SZTO thin film transistors depending on annealing time and investigated the mechanism of the degradation, which was found to be related to increase of the roughness of the a-2SZTO thin films with increasing thermal annealing treatment time, resulting in increase of the contact resistance [8].

2. EXPERIMENTS

Herein, a-2SZTO TFTs were fabricated on SiO_2 gate insulators on highly doped Si. A schematic diagram of the bottom gate a-2SZTO TFTs is shown in Fig.1. A highly doped p-type Si substrate served as the bottom-gate electrode. An RF magnetron sputtering system was used to deposit the a-2SZTO active layer at room temperature. The sputtering of the a-2SZTO target was carried out with the Ar/O_2 gas mixing ratio of 49:1, RF power of 50 W, and process pressure of 5 mTorr. Photolithography and wet-etching were used to pattern the layers. A lift-off process was then employed to define the channel length (L) of 50 μm and width (W) of 250 μm. Au/Ti was used as the source/drain electrodes. Ti was deposited by electron beam evaporation, while Au was deposited by thermal evaporation. The annealing process was performed at 500℃ for 2 hours to improve the electrical properties. In addition, to confirm the effect of the annealing process, the annealing was performed for different times, ranging from 2 to 4 hours, in air conditions. The TFT I-V characteristics were measured at room temperature using a semiconductor analyzer. In addition, the structural properties of the 2SZTO thin films were confirmed using an AFM (atomic force microscope) analyzer, while the contact resistance was determined using a transmission line method (TLM) analyzer.

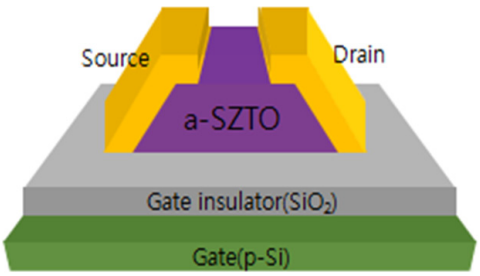

Fig. 1. Schematic view of an a-2SZTO(Si-Zn-Sn-O) thin film transistor.

3. RESULTS AND DISCUSSION

The measured electrical properties are summarized in Table 1. The electrical properties could be calculated as follows:

Table 1. The properties of a-2SZTO TFTs according to annealing time.

Annealing time	Mobility (μ_{FE})	S.S	On/Off ratio	V_{TH}
2 hours	2.170	2.96	2.2E+06	9.8
3 hours	0.412	5.56	9.3E+04	13.2
4 hours	0.018	6.00	3.1E+03	14

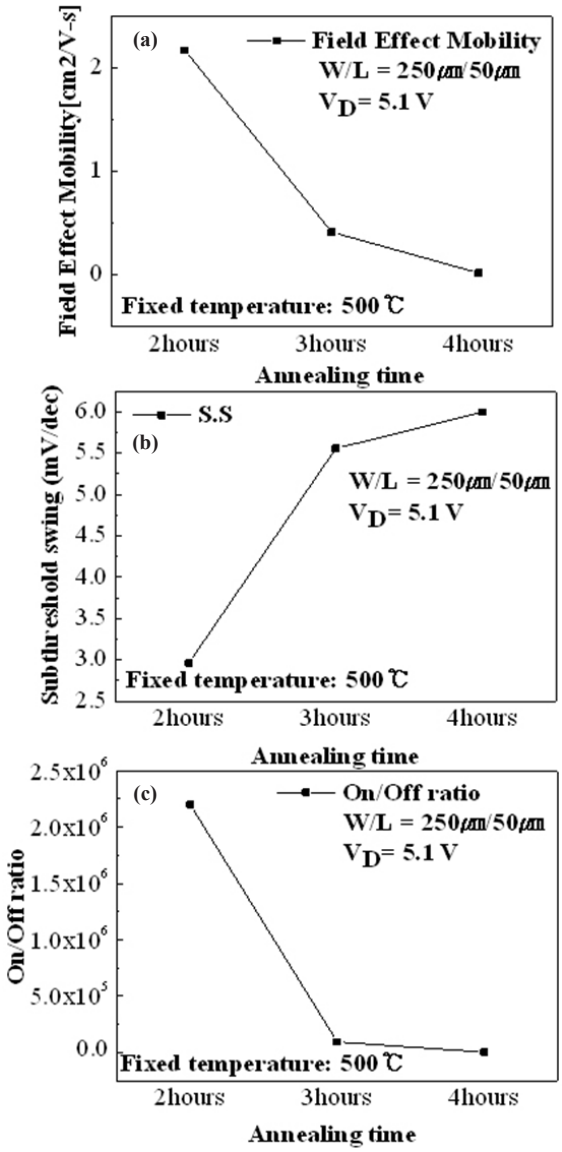

Fig. 2. Field effect mobility, S.S and On/Off ratio of a-2SZTO TFTs annealed for various times.

$$I_D = \frac{WC_i}{2L}\mu_{FE}(V_G - V_{TH})^2$$

Where W is the channel width, L is the channel length, and C_i is the capacitance per unit area of the gate-insulator. I_D is the measured drain current at V_D = 5.1 V, and V_{TH} is the threshold voltage.

The mobility, S.S, and On/Off ratio of the a-2SZTO TFTs at various annealing times are displayed in Figure 2. The mobility, S.S, and On/Off ratio were rapidly deteriorated by increase of the annealing exposure time. This confirmed that increased anneal-

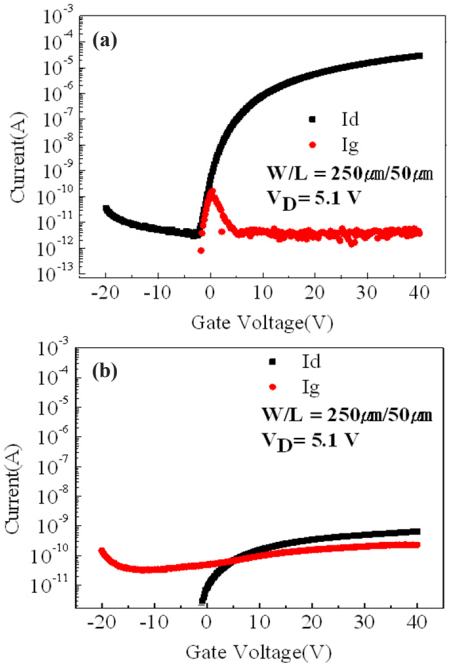

Fig. 3. Transfer curve of a-2SZTO TFTs annealed at 500℃ (a), and without annealing treatment (b).

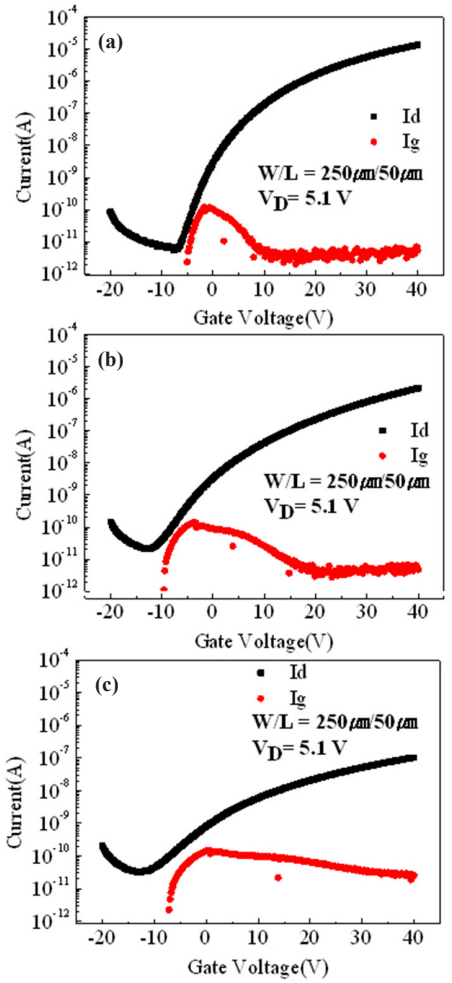

Fig. 4. Transfer curve of 2SZTO TFTs as a function of the annealing time: (a) 2 hours, (b) 3 hours, and (c) 4 hours.

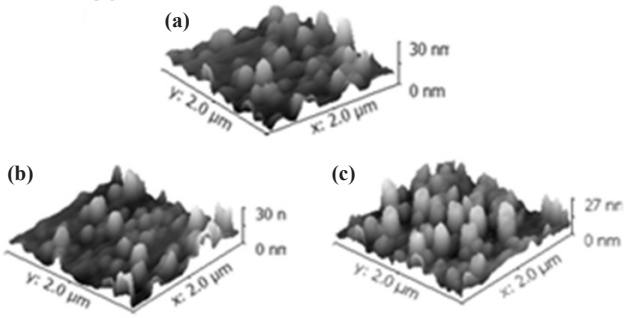

Fig. 5. AFM surface image with different thermal annealing treatment times: (a) 2 hours, (b) 3 hours, and (c) 4 hours.

Table 2. RMS roughness of a-2SZTO thin films prepared with different thermal annealing treatment times.

Annealing time	2 hours	3 hours	4 hours
RMS roughness	4.15 nm	4.68 nm	4.95 nm

ing time resulted in deterioration of the electrical characteristics, which was mainly due to increase of the surface roughness, which in turn can cause increase of the contact resistance.

The transfer characteristics of the a-2SZTO TFTs are shown in Fig. 3. The transfer curve of the a-2SZTO TFTs annealed at 500℃ for 2 hours displayed the field effect mobility of 3.61 cm^2/Vs, and the subthreshold swing (S.S) of about 1. In contrast, those without annealing treatment showed the field effect mobility of 2.94. E-5 cm^2/Vs and on current of 6.48.E-10, as can be seen in Fig. 3(b). Therefore, the a-2SZTO TFTs definitely require thermal annealing treatment for better performance [9].

Figure 4 shows the transfer curves of a-2SZTO TFTs fabricated under the same conditions as those in Fig. 3, except with variation of the annealing time. The longer the exposure of a-2SZTO thin films to high temperature annealing treatment, the worse the electrical properties of the thin films became. This degradation of the electrical properties with increase of the high temperature annealing time was mainly due to the increased roughness of the a-2SZTO thin films.

Therefore, we next investigated the relationship between the increase of annealing time and the surface roughness. Figure 5 shows the AFM surface images for samples prepared under different thermal annealing times. The RMS roughness values are summarized in Table 2. Generally, the surface roughness of most AOS thin films decreases with increasing thermal annealing treatment [9]. However, the a-2SZTO thin film of Si-doped ZTO is sensitive to both temperature and time [10]. The a-2SZTO thin film annealed at 500℃ for 2 hours displayed the RMS roughness of 4.15 nm, while the RMS roughness was increased to about 4.95 nm after 4 hours of annealing at 500℃. Thus, it can be seen that the RMS roughness was rapidly increased with increasing annealing treatment time.

This being so, the deterioration of the electrical characteristics by the time and temperature of annealing treatment was confirmed. As the electrical characteristics of a-2SZTO thin films annealed at high temperature for long periods become deteriorated, careful optimization of the annealing conditions to achieve better performance of a-2SZTO should be undertaken.

It is very important to investigate the relationship between the surface roughness and the contact resistance. The relation of contact resistance with the roughness can be measured systematically using the conventional transmission line method (TLM). The TLM was adopted herein for evaluation of the contact re-

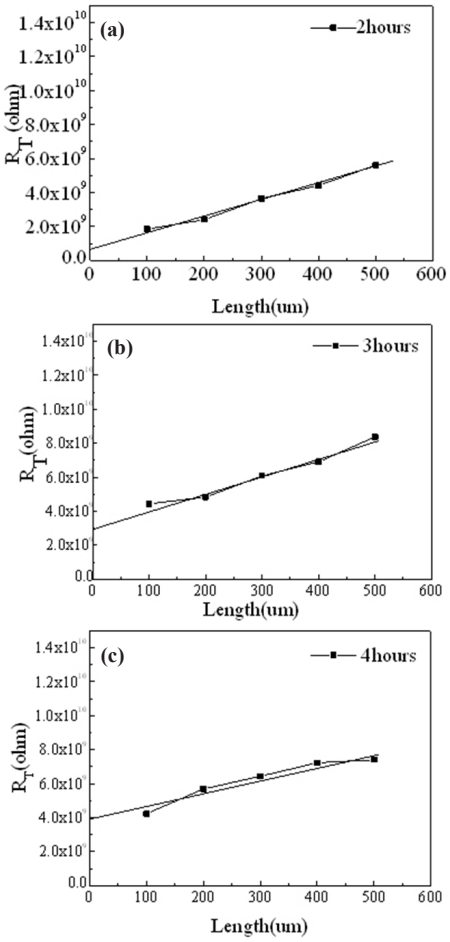

Fig. 6. Total resistance as a function of the TFT channel length with different thermal annealing treatment times for a-2SZTO thin films: (a) 2 hours, (b) 3 hours, and (c) 4 hours.

sistance of the thin films for differing thermal annealing times. By defining the total resistance (R_T) as $R_T=V_{DS}/I_{DS}$, R_T can be expressed as:

$$R_T = \frac{V_{DS}}{I_{DS}} = r_{ch}L + R_{S/D}$$

Where r_{ch} is the channel resistance per unit channel length, and RS/D is the series resistance at the S/D contacts [11].

The total resistance as a function of the TFT channel length for a-2SZTO thin films fabricated with different thermal annealing times is shown in Figure 6. In order to derive contact resistance on the graph, only the y-intercept is required. The contact resistances are summarized in Table 3. It could clearly be observed that the contact resistance was increased with increasing annealing treatment time and roughness. Therefore, it was confirmed that deterioration of the electrical characteristics of a-2SZTO thin films by thermal annealing treatment was related to the increased surface roughness, leading to increased contact resistance. Thermal annealing treatment can cause bumpy roughness, which translates to increase of the contact resistance. For this reason, the electrical characteristics of a-2SZTO annealed at high temperature for a long time become deteriorated, making it necessary to carefully optimize the annealing process

Table 3. Contact resistance of a-2SZTO thin films with different thermal annealing treatment times.

Annealing time	2 hours	3 hours	4 hours
contact resistance (MΩ)	0.6	2.9	3.9

of a-2SZTO, in terms of time and temperature, to achieve better performance.

4. CONCLUSIONS

In summary, we fabricated a-2SZTO thin films and examined the properties according to thermal annealing treatment time. Thermal annealing can control the electrical characteristics of the AOS TFTs. However, a-2SZTO thin films of Si-doped ZTO are sensitive to temperature. It was found that thermal annealing treatment at high temperature for long periods can cause bumpy roughness, which leads to increase of the contact resistance between the electrode and channel. This being so, the on current of the a-2SZTO TFTs was rapidly decreased with increasing thermal annealing time. Deterioration of the electrical characteristics according to the time and temperature of annealing treatment was also confirmed. The a-2SZTO TFTs annealed at 500℃ for 2 hours showed the mobility of 2.17 cm^2/Vs, while longer annealing time decreased the mobility. For these reasons, the electrical characteristics of a-2SZTO annealed at high temperature for long periods are deteriorated, thus the annealing conditions should be carefully optimized to achieve better performance of a-2SZTO.

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