

A Single-ended Simultaneous Bidirectional Transceiver in 65-nm CMOS Technology

Min-Ki Jeon and Changsik Yoo

Abstract—A simultaneous bidirectional transceiver over a single wire has been developed in a 65 nm CMOS technology for a command and control bus. The echo signals of the simultaneous bidirectional link are cancelled by controlling the decision level of receiver comparators without power-hungry operational amplifier (op-amp) based circuits. With the clock information embedded in the rising edges of the signals sent from the source side to the sink side, the data is recovered by an open-loop digital circuit with 20 times blind oversampling. The data rate of the simultaneous bidirectional transceiver in each direction is 75 Mbps and therefore the overall signaling bandwidth is 150 Mbps. The measured energy efficiency of the transceiver is 56.7 pJ/b and the bit-error-rate (BER) is less than 10^{-12} with 2^7-1 pseudo-random binary sequence (PRBS) pattern for both signaling directions.

Index Terms—Simultaneous bidirectional transceiver, echo cancellation, blind oversampling, data recovery, CMOS

I. INTRODUCTION

Simultaneous bidirectional link allows devices to send data without waiting for a communication channel to become available and can maximize the data bandwidth for a given number of signaling wires [1-6]. Because transmitted signals from two devices co-exist on the

channel, the receiver circuit of a device has to be capable of cancelling the signal component sent by itself from the signals present on the channel, which is called the echo cancellation. The echo cancellation is usually performed by subtracting the echo signal with precise analog circuits such as operational amplifier (op-amp) based circuits [5, 6], which may result in large power consumption. The clock and data recovery (CDR) is usually performed by a phase-locked loop (PLL) based closed loop circuit which may occupy large silicon area and consume substantial power as well. To save power, it is desirable to cancel the echo signal without relying on op-amp based precise analog circuits and perform the CDR without PLL.

This paper describes a simultaneous bidirectional transceiver (75 Mbps in each direction) with voltage-mode single-ended signaling for an auxiliary command and control bus for a 6 Gbps unidirectional data link. The echo cancellation is performed by deliberately controlling the decision level of the receiver circuit. In order to allow the open-loop CDR without PLL, the clock information is delivered from the source device to the sink device (forward link) over the same single wire with the data signal by employing a duty modulated signaling. The data is recovered by an open-loop digital circuit with 20 times oversampling and majority voting.

Section II describes the architecture and the circuit implementation of the simultaneous bidirectional transceiver. The experimental results of the simultaneous bidirectional transceiver realized in a 65 nm CMOS technology are given in Section III and finally, Section IV concludes this paper.

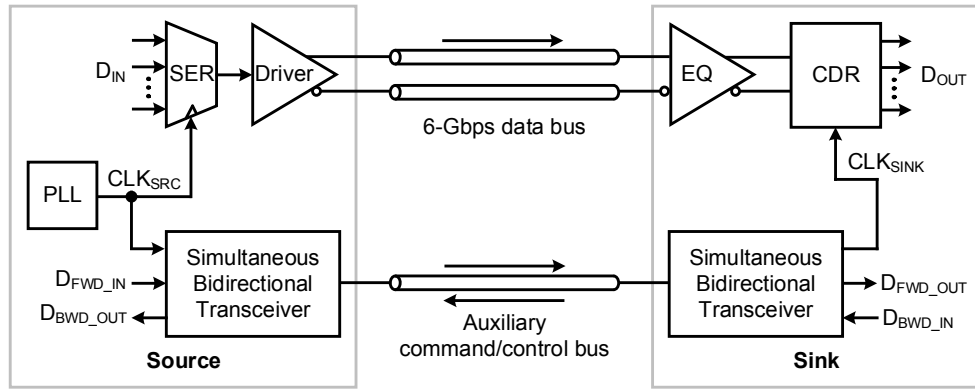


Fig. 1. System architecture with the simultaneous bidirectional link on the auxiliary command/control bus.

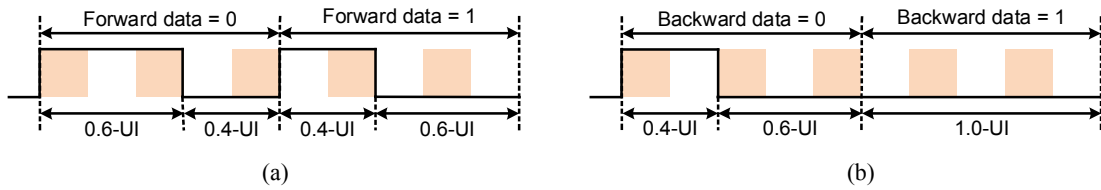


Fig. 2. Signaling schemes for (a) the forward link, (b) the backward link of the auxiliary command and control bus.

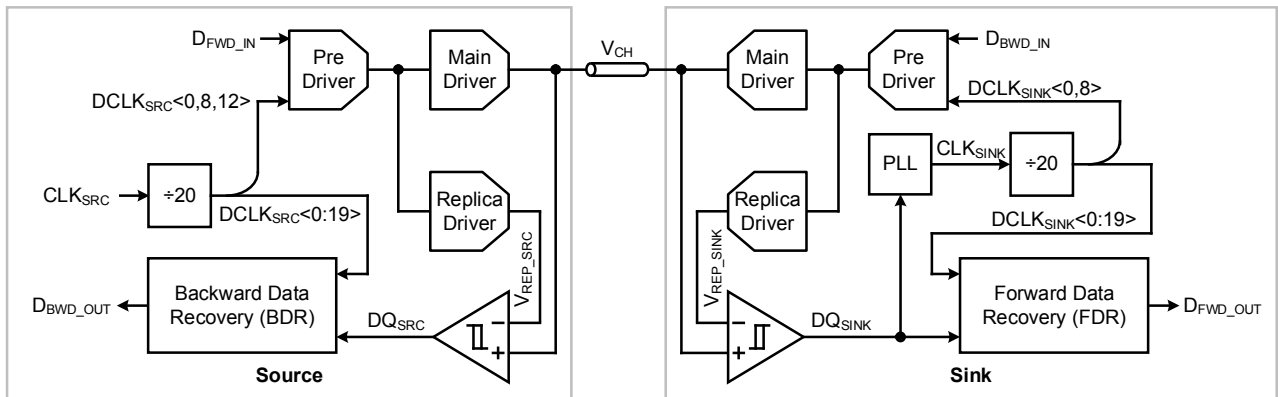


Fig. 3. Proposed simultaneous bidirectional transceiver.

II. SIMULTANEOUS BIDIRECTIONAL TRANSCEIVER

The simultaneous bidirectional link is used to deliver command and control data through an auxiliary bus of the system shown in Fig. 1 where the data link is 6 Gbps and unidirectional from the source to the sink. Another key function of the auxiliary bus is to send a clock information from the source to the sink. With this clock information, the sink device recovers the clock and data from the incoming 6 Gbps data stream.

The auxiliary bus uses different signaling formats for the forward link (from the source to the sink) and backward link (from the sink to the source). The duty-

modulated signaling of the forward link shown in Fig. 2(a) allows the clock information to be delivered from the source to the sink by having the rising edges at every bit of the forward data. If the duty is 60%, the forward data is “0” and if it is 40%, the forward data is then “1” as shown in the figure. Because the source device already has the clock information, there is no need to send a clock from the sink to the source. In addition, non-return-to-zero (NRZ) signaling scheme can’t be used with proposed backward data recovery circuit as will be explained later. Therefore, the backward link uses the return-to-zero (RZ) signaling scheme as shown in Fig. 2(b). The transceiver architectures of the simultaneous bidirectional command and control bus are shown in Fig.

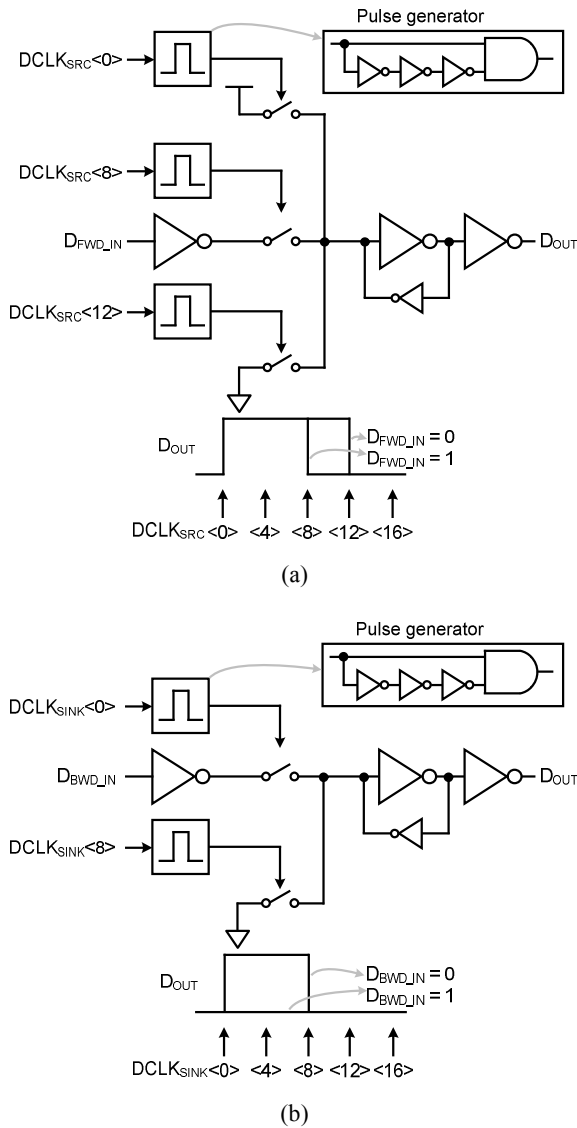


Fig. 4. Pre-driver of (a) the source device, (b) sink device.

3 for the source and sink devices.

1. Transmitter of Source Device

From the 1.5 GHz source clock CLK_{SRC} , the multi-phase clocks $DCLK_{SRC}<0:19>$ are generated to be used for both the transmitter and receiver circuits of the source device. Because the data rate is low, there is no serializer in the transmitter, that is, the data input D_{FWD_IN} has 75 Mbps data rate. The pre-driver shown in Fig. 4(a) generates the duty-modulated signal with the data input D_{FWD_IN} . At the rising edge of $DCLK_{SRC}<0>$, the pre-driver output D_{OUT} becomes “1” regardless of the data input D_{FWD_IN} . If the data input D_{FWD_IN} is “1”, the output

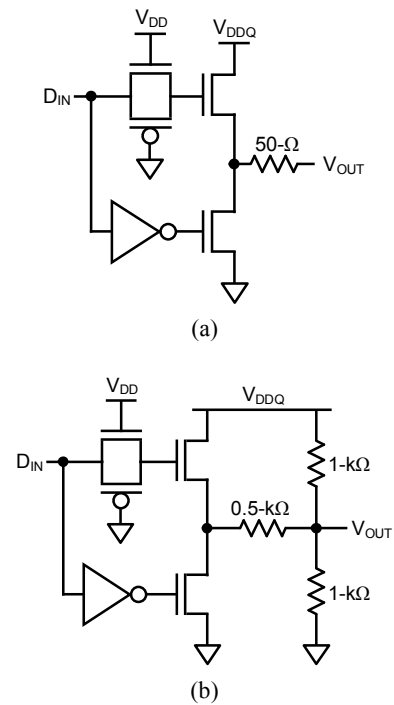


Fig. 5. (a) Main driver, (b) replica driver.

D_{OUT} is set to “0” by the rising edge of $DCLK_{SRC}<8>$, which provides the 40% duty. If the data input D_{FWD_IN} is “0”, the output D_{OUT} is set to “0” by the rising edge of $DCLK_{SRC}<12>$, which provides the 60% duty.

The output of the pre-driver is applied to the voltage-mode main driver shown in Fig. 5(a). The voltage-mode driver employs the nMOS-nMOS type architecture to save silicon area and the swing is determined by the supply voltage V_{DDQ} which is generated by a linear regulator [7, 8].

2. Transmitter of Sink Device

In the sink device, the echo-cancelled output DQ_{SINK} of the receiver comparator has rising edges at every bit and thus can be used as the reference clock of the PLL generating the multi-phase clock $DCLK_{SINK}<0:19>$ used for both the transmitter and receiver circuits of the sink device. As in the source device, there is no serializer and the data input D_{BWD_IN} has 75 Mbps data rate. The pre-driver shown in Fig. 4(b) provides the modulated signal in the RZ format with the data input D_{BWD_IN} .

At the rising edge of $DCLK_{SINK}<0>$, the pre-driver output D_{OUT} becomes “0” or “1” depending on the input D_{BWD_IN} . The pre-driver output D_{OUT} becomes “0” at the

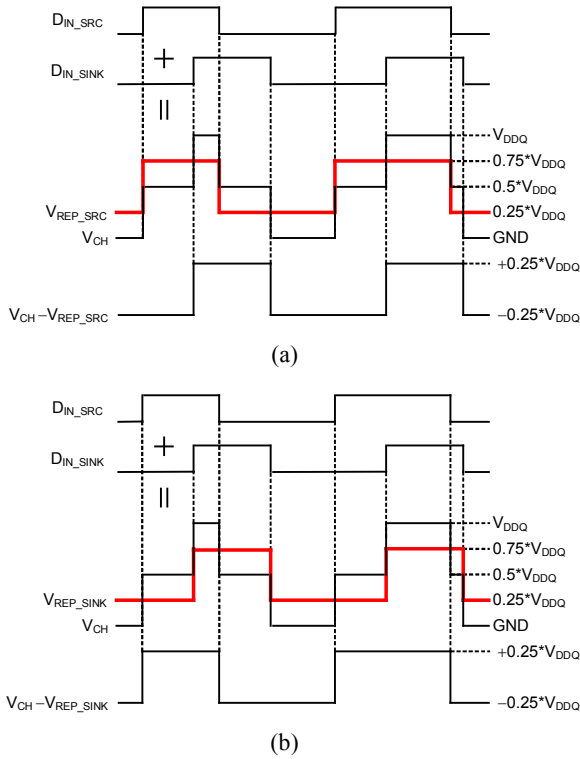


Fig. 6. Echo-cancellation at (a) the source, (b) sink side with the replica driver output as the reference for input receiver.

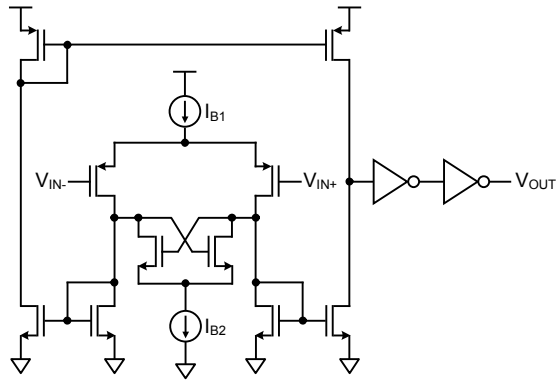


Fig. 7. Input comparator with hysteresis.

rising edge of $DCLK_{SINK} \langle 8 \rangle$, which provides the RZ signal. The main driver of the sink device has the same architecture shown in Fig. 5(a) as the source device.

3. Echo Cancellation

The receiver has to be capable of cancelling the signal component driven by itself. For this, the replica driver shown in Fig. 5(b) is driven by the same driving signal as the main driver and generates a replicated signal which is subtracted from the signal present on the simultaneous

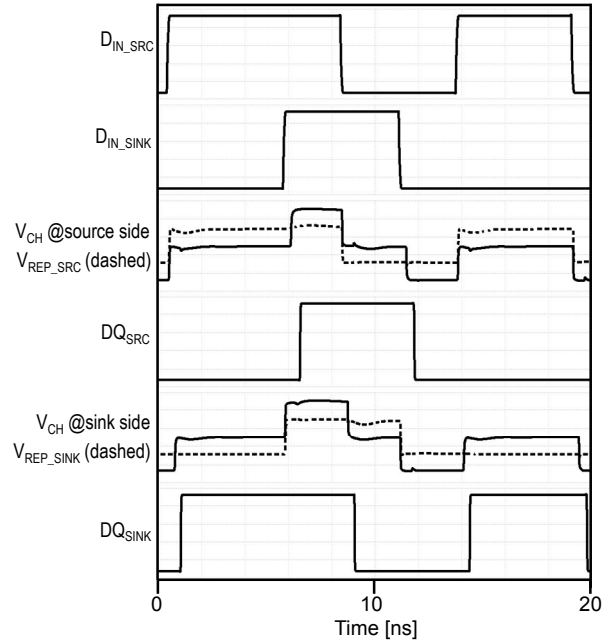


Fig. 8. Simulated waveforms of the echo-cancellation at the source and sink side.

bidirectional bus. In order to minimize the additional power consumption by the replica driver, the sizes of the transistors are scaled to be 1/10 of those of the main driver while the output resistance ($0.5 \text{ k}\Omega$) of the replica driver is 10 times larger than that ($50 \text{ }\Omega$) of the main driver. When $D_{IN} = \text{“1”}$ or “0” , $0.5 \text{ k}\Omega$ resistor is connected to the V_{DDQ} or ground, respectively. Therefore, with the two $1 \text{ k}\Omega$ resistors, the output voltage level of the replica driver is $0.75 \times V_{DDQ}$ and $0.25 \times V_{DDQ}$ for $D_{IN} = \text{“1”}$ and “0” , respectively. The output of the replica driver is used as the reference voltage for the receiver comparator.

As shown in Fig. 6, the voltage level V_{CH} of the simultaneous bidirectional bus can be 0 , $0.5 \times V_{DDQ}$, or V_{DDQ} depending on D_{IN_SRC} and D_{IN_SINK} . If the output voltage level (V_{REP_SRC} for the source device and V_{REP_SINK} for the sink device) of the replica driver is subtracted from the bus voltage level V_{CH} , we can get the desired result as shown in Fig. 6. Because the data rate of the proposed simultaneous bidirectional link is not high, the linearity of the echo signal subtraction is not a concern and the echo-cancellation with the comparator shown in Fig. 7 is sufficient. In order to provide an immunity to possible glitch or noise on V_{CH} , a finite hysteresis window is given to the comparator.

The simulated waveforms of the echo cancellation are

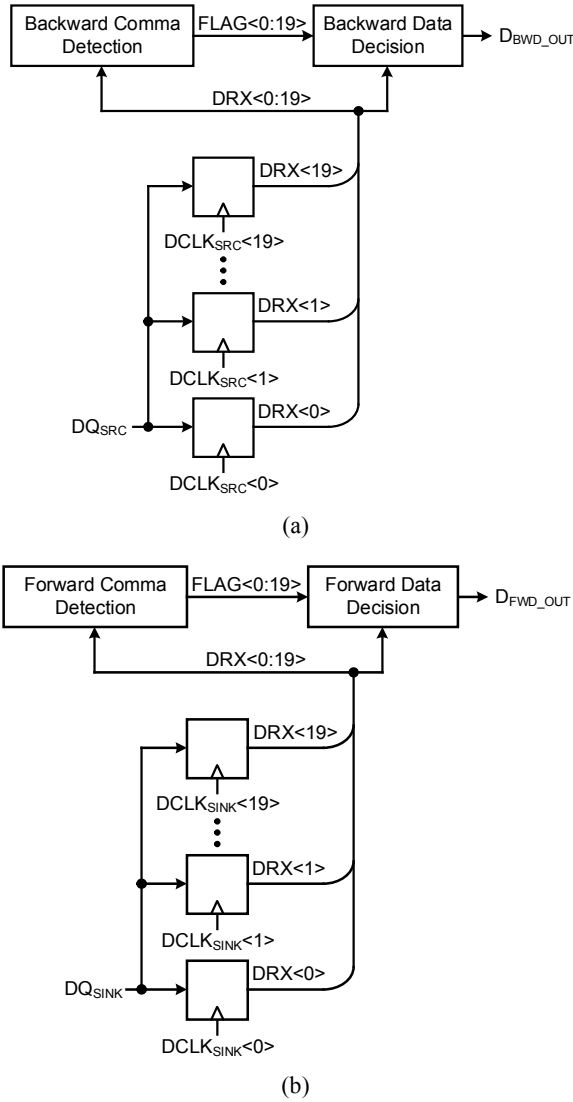


Fig. 9. (a) Backward, (b) forward data recovery circuits.

shown in Fig. 8. We can see the outputs V_{REP_SRC} and V_{REP_SINK} of the replica drivers are following the inputs of the main driver D_{IN_SRC} and D_{IN_SINK} , respectively and the receiver comparators are providing the echo-cancelled outputs DQ_{SRC} and DQ_{SINK} .

4. Receiver of Source Device

The output DQ_{SRC} of the receiver comparator is applied to the backward data recovery (BDR) circuit to provide the data output D_{BWD_OUT} . The block diagram and the operation timing of the BDR are shown in Fig. 9(a) and 10(a), respectively. In order to find the comma which is the starting position of a bit, the 20 times oversampled outputs $DRX<0:19>$ are applied to the backward comma

detection block. Initially, the flag signals $FLAG<0:19>$ are all set to “0” and the backward comma detection block sets $FLAG< i >$ to “1” if $DRX< i >$ is “1” at least once. For the case shown in Fig. 10(a), the flag bits $FLAG<1:8>$ are “1” and the flag bits $FLAG<0, 9:19>$ are “0”. Then, we can know that the rising edge of the input signal DQ_{SRC} lies between the rising edges of the clocks $DCLK_{SRC}<0>$ and $DCLK_{SRC}<1>$. Then, the data sampled by the clocks $DCLK_{SRC}<1:19, 0>$ correspond to the 20 times oversampled data for a bit of the backward data input DQ_{SRC} .

Ideally, the 20 samples have to be all “0” when DQ_{SRC} is “1”. With finite clock jitter, however, there might be more than “1” samples even when DQ_{SRC} is “1”. In order for the BDR to have good immunity to the clock jitter, the data decision block determines the data is “0” only when there are more than two “1” samples among the 20 samples per bit.

5. Receiver of Sink Device

The forward data recovery (FDR) circuit of the sink device has similar architecture to the BDR circuit of the source device as shown in Fig. 9(b). The forward comma detection block operates with the same principle as the backward comma detection block. For the case shown in Fig. 10(b), the flag bits $FLAG<1:12>$ are “1” and the flag bits $FLAG<0, 13:19>$ are “0”. Then, we can know that the rising edge of the input signal DQ_{SINK} lies between the rising edges of the clocks $DCLK_{SINK}<0>$ and $DCLK_{SINK}<1>$. Then, the data sampled by the clocks $DCLK_{SINK}<1:19, 0>$ correspond to the 20 times oversampled data for a bit of the forward data input DQ_{SINK} .

For the recovery of the forward link data, the FDR performs the majority voting with the 20 samples per bit. If there are more “1” samples than “0” samples, the data is “0” and vice versa.

III. EXPERIMENTAL RESULTS

The proposed simultaneous bidirectional transceivers for the source and sink devices have been implemented in a 65 nm CMOS technology. The chip microphotograph is shown in Fig. 11. The transceiver occupies 0.0285 mm² silicon area. The transceivers operate with 1.2 V supply

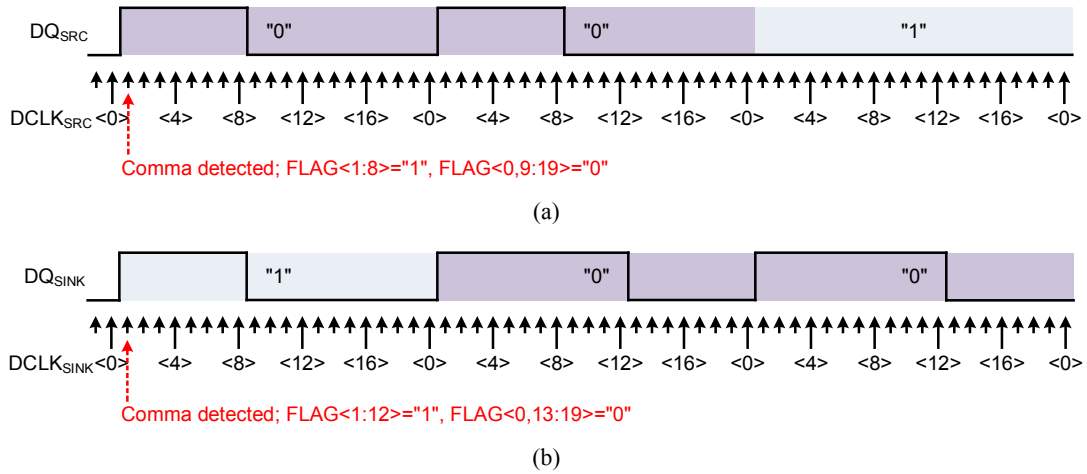


Fig. 10. Timing diagram of the (a) backward, (b) forward data recovery.

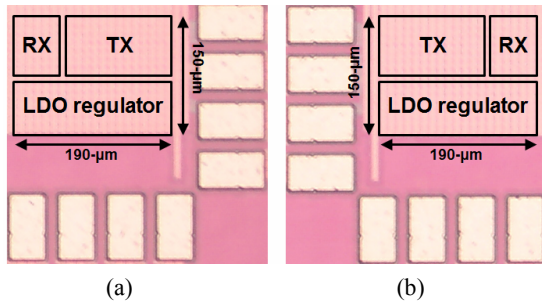


Fig. 11. Chip microphotograph of the transceiver for (a) source, (b) sink device.

while the supply V_{DDQ} of the main driver is 0.6 V which is generated by a low-drop-out (LDO) regulator. The transceivers of the source and sink consume 5.4 mW and 3.11 mW, respectively. Because the forward link uses the duty-modulated signaling, the main driver of the source device has higher transition probability and therefore consumes more power than that in the sink device. The energy efficiency of the proposed simultaneous bidirectional transceiver is 56.7 pJ/bit.

The source and sink devices are connected with a 3 meter coaxial cable. At 75 MHz, the cable shows only 0.38 dB channel loss which has a negligible effect on the performance of the simultaneous bidirectional link. Even when the output impedance of the main driver is varied from 30 Ω to 70 Ω , the bit-error-rate (BER) of the transceiver is less than 10^{-12} with 2^7-1 PRBS pattern for the both signaling directions.

Fig. 12(a)-(c) show the measured eye-diagrams of the bus signal V_{CH} , the receiver comparator output DQ_{SRC} at the source, and the receiver comparator output DQ_{SINK} at

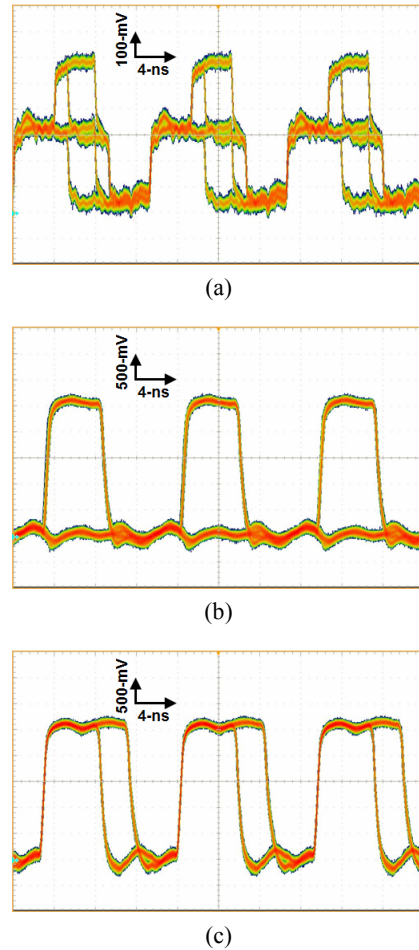


Fig. 12. Measured eye diagram of (a) bus signal V_{CH} , (b) echo-cancelled DQ_{SRC} at source, (c) echo-cancelled DQ_{SINK} at sink.

the sink, respectively. We can see the echo components are cancelled at the receiver comparator outputs DQ_{SRC} and DQ_{SINK} and the rising edges of DQ_{SINK} are available at

Table 1. Performance comparison of simultaneous bidirectional transceiver

	This work	[1]	[2]	[3]	[4]
Data bandwidth [Gbps]	0.15	4	8	3.6	8
Power consumption [mW]	8.51	28	112	70	316
Energy efficiency [pJ/bit]	56.7	7	14	19.4	39.5
Circuit area [mm ²]	0.0285	0.0218	0.055	0.2016	0.13
Bit error rate (BER)	<10⁻¹²	-	<10 ⁻⁹	-	<10 ⁻¹¹
CMOS process [μ m]	0.065	0.1	0.35	0.1	0.18

every bit which can be used as the clock reference for the operation of the sink device.

Table 1 compares the performance of the proposed simultaneous bidirectional link with other works. The other works are targeted for multi-Gbps data bus while the simultaneous bidirectional link of this work is for command and control bus. Therefore it is not easy to directly compare the performance but the energy efficiency of this work seems to be poor compared with others. The low energy efficiency of this work is mainly due to the low data rate of the proposed simultaneous bidirectional link. More than 80% of the total power is consumed by the main drivers of the source and sink devices, which is not scaled with the data rate because it is static power.

In order to operate properly at multi-Gbps data rate, proposed simultaneous bidirectional link require some modifications. First, multi-phase clock generation scheme should be modified because it will be difficult to generate several Gbps multi-phase clock from simple frequency divider. Second, as explained in the above Section II, backward data recovery circuit requires some modification because amount of the clock jitter will increase compared to the period of the clock.

Although the proposed simultaneous bidirectional link has relatively poor energy efficiency compared with multi-Gbps high-speed wireline links, this work provides a novel approach for the realization of a simultaneous bidirectional command and control bus over single wire with minimum analog circuitry in a small silicon area.

IV. CONCLUSION

A simultaneous bidirectional transceiver has been described which is targeted for a command and control bus over a single wire. The clock information is embedded in the rising edges of the signals sent from the source side to the sink side, which greatly simplifies the

clock and data recovery of the sink side. The effects of the echo signals are compensated for by adaptively controlling the decision level of receiver comparators without any power-hungry operational amplifier based circuits. The measured energy efficiency of the transceiver implemented on a 65 nm CMOS technology is 56.7 pJ/b and bit-error-rate (BER) is less than 10⁻¹² with 2⁷-1 PRBS pattern for both signaling directions.

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