JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.16, NO.6, DECEMBER, 2016
https://doi.org/10.5573/JSTS.2016.16.6.847

ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

Si CMOS Extension and Ge Technology Perspectives Forecast Through Metal-oxide-semiconductor Junctionless Field-effect Transistor

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***Abstract*—Applications of Si have been increasingly exploited and extended to More-Moore, More-than-Moore, and beyond-CMOS approaches. Ge is regarded as one of the supplements for Si owing to its higher carrier mobilities and peculiar band structure, facilitating both advanced and optical applications. As an emerging metal-oxide device, the junctionless field-effect transistor (JLFET) has drawn considerable attention because of its simple process, less performance fluctuation, and stronger immunity against short-channel effects due to the absence of anisotype junctions. In this study, we investigated lateral field scalability, which is equivalent to channel-length scaling, in Si and Ge JLFETs. Through this, we can determine the usability of Si CMOS and hypothesize its replacement by Ge. For simulations with high accuracy, we performed rigorous modeling for μ_n and μ_p of Ge, which has seldom been reported. Although Ge has much higher μ_n and μ_p than Si, its saturation velocity (v_{sat}) is a more determining factor for maximum I_{on}. Thus, there is still room for pushing More-Moore technology because Si and Ge have a slight difference in v_{sat}. We compared both *p*- and *n*-type JLFETs in terms of I_{on}, I_{off}, I_{on}/I_{off}, and swing with the same channel doping and channel length/thickness. I_{on}/I_{off} is inherently low for Ge but is invariant with V_{DS}. It is estimated that More-Moore approach can be further driven if Si is mounted on a JLFET until Ge has a strong possibility to replace Si for both *p*- and *n*-type devices for ultra-low-power applications.**

***Index Terms*—Si CMOS, low power consumption, junctionless field-effect transistor, Ge channel, device simulations**

I. INTRODUCTION

Recently, Si CMOS technology has encountered limitations so that it is no longer feasible to fabricate More-Moore and More-than-Moore devices. Therefore, both the material and structure of devices must be substituted. We simulated a device with Ge being regarded regarded as one of the supplements for Si owing to its higher carrier mobilities and peculiar band structure, thus facilitating both advanced logic and optical applications for improved current characteristics and other DC parameters.

Metal-oxide-semiconductor field-effect transistors (MOSFETs) are struggling with short-channel effects (SCEs) [4]. As an emerging MOSFET, the junctionless FET (JLFET) has a simple process, minimal performance fluctuation, and stronger resistivity against SCEs because of the absence of anisotype junctions. These features are closely related with increased throughput and yield. Regarding device reliability, lower DC leakages are expected in the operation of JLFETs because no metallurgical junctions are formed due to counter-doping [5, 6]. In general, researchers have fabricated JLFETs on a silicon-on-insulator (SOI) platform to decouple the

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Manuscript received Jun. 4, 2016; accepted Aug. 28, 2016
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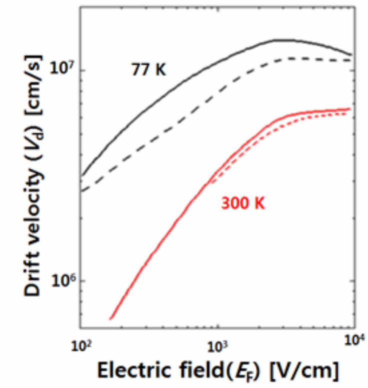


Fig. 1. Drift velocity with respect to electric field of Ge [1, 2].

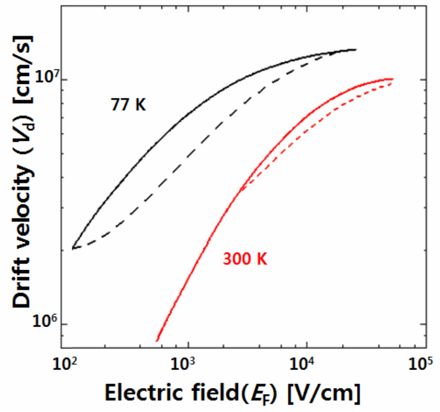


Fig. 2. Drift velocity with respect to electric field of Si [3].

channel from the substrate and minimize the leakage currents [7, 8].

Fig. 1 and 2 show the drift velocity (v_d) with respect to electric field of Ge and Si, respectively. Despite the higher mobility of Ge compared with that of Si, the current drivability of Ge itself does not explicitly excel that of Si in the high electric field region because Ge has lower v_{sat} of electron [1-3].

In this study, we investigated lateral field scalability, which is equivalent to channel length scaling, in Si and Ge JLFETs [9], by which we can determine the usability of Si CMOS and hypothesize its replacement by Ge. For simulations with high accuracy, we performed rigorous modeling for μ_n and μ_p of Ge. Although Ge has much higher μ_n and μ_p than Si, v_{sat} is a more determining factor for maximum I_{on}.

II. SIMULATION APPROACH

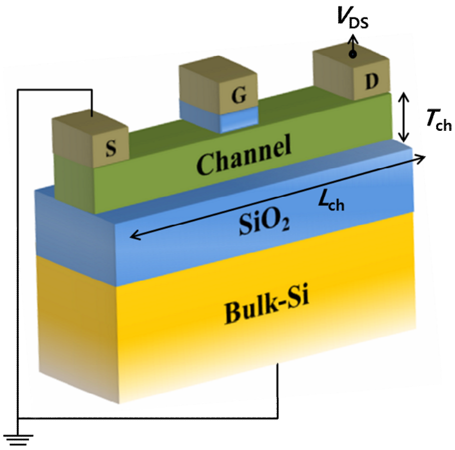


Fig. 3. Schematic of the simulated JLFET device.

Fig. 3 shows the schematic of the simulated JLFET device. To prepare an SOI-like environment on bulk-Si substrate, a 200-nm-thick insulator (SiO_2) was assumed to be deposited on the Si substrate. Hafnium oxide (HfO_2) was used as the gate oxide ($\varepsilon_r = 22.0$) with thickness t_{ox} = 3 nm to reflect the most recent technology roadmap, suggesting that the equivalent oxide thickness (EOT) be 0.54 nm for the near-year low-power (LP) application [10, 11]. The n-type channel concentration of 1×10^{17} cm^{-3} was selected because the difference between the work function of p^+ poly-Si gate and that of n^+ Si and Ge channel depletes the channel so that JLFET is operated in the normally-off mode [12]. Furthermore, n^+ poly-Si gate is used for p-type channels [13, 14]. Accordingly, the channel materials were changed between Ge and Si for comparing current characteristics and other DC parameters as functions of drain voltage (V_{DS}). We used the simulation tool provided by Silvaco, Inc.

For higher accuracy and credibility of 2-D simulation results, various models were used jointly. These include lateral electric field-dependent mobility model, bandgap-narrowing model, recombination accounting for high-level injection effects model, Shockley–Read–Hall two-carrier recombination model, band-to-band tunneling model, density gradient model, and quantum tunneling model for accurate gate leakage check. However, the lateral electric field-dependent mobility model is used for Si-based devices only. $\mu(E)$ is modeled as:

$$\mu_n(E) = \mu_{n0}\left[\frac{1}{1+\left(\frac{\mu_{n0}E}{v_{\mathrm{sat,n}}}\right)}\right]^{\frac{1}{\beta_n}} \quad \mu_p(E) = \mu_{p0}\left[\frac{1}{1+\left(\frac{\mu_{p0}E}{v_{\mathrm{sat},p}}\right)}\right]^{\frac{1}{\beta_p}}$$

where $\mu(E)$ is defined as the effective mobility, which is a function of electric field and μ_0 is the doping concentration-dependent mobility at zero field. In this study, the values of zero-field electron and hole mobilities of Ge are μ_{n0} = 2400 cm^2/V·s and μ_{p0} = 850 cm^2/V·s, respectively, at channel doping = 1 × 10^{17} cm^{-3}, and have seldom been reported [15, 16]. E is the latter electric field and β is the fitting parameter of Si, with β_n = 2 and β_p = 1. This is unsuitable for a Ge JLFET: the corrected parameters for Ge are β_n = 2 and β_p = 2. Moreover, for Ge, $v_{sat,n}$ = 7 × 10^6 cm/s and $v_{sat,p}$ = 6.3 × 10^6 cm/s [17-19].

The density gradient model was used to study the effect of quantization by increasing the effective bandgap of Si. Because of the formation of discrete energy levels in a 2-D system, the minimum energy for an electron or hole no longer coincides with the conduction or valence band edge. This can be modeled by assuming that the effective bandgap is increased by an amount ΔE over the conventional bandgap. ΔE is modeled as:

$$\begin{aligned}&\Delta E = \beta\left(\frac{\varepsilon_{Si}}{4kTq}\right)^{1/3}(|E_s| - 100\,kV/cm)^{2/3}\\&E_s > 100\,kV/cm\\&\Delta E = 0 \quad E_s < 100\,kV/cm\end{aligned}$$

where E_s is the surface electric field, β = 6.1 × 10^{-8} eV/cm, which is constant and was obtained from fitting the simulation data from the aforementioned model to the experimental data and the data obtained from the self-consistent calculations [20].

III. RESULTS AND DISCUSSION

We simulated Si JLFETs for comparison. Fig. 4 shows the transfer curves of the n-type Si JLFET having different L_{ch} and T_{ch} values at V_{DS} = 0.85 V. This suggests that JLFET should be suitable for ultra-LP (ULP) applications, in which the management of I_{off} is particularly important. However, the subthreshold swing (S) worsens as L_{ch} is scaled. Fig. 5 shows the transfer curves of the p-type Si JLFET having different L_{ch} and T_{ch} values at V_{DS} = 0.85 V. Both n- and p-type JLFETs have the same channel doping, that is, 1 × 10^{17} cm^{-3}. As T_{ch} reduces, the off-current (I_{off}) decreases. Moreover, the on-current (I_{on}) does not vary significantly as function of L_{ch} and T_{ch}. In addition, the on/off current ratio (I_{on}/I_{off}) is satisfactorily maintained in the order of 10^{10} even at L_{ch} = 10 nm and T_{ch} = 10 nm.

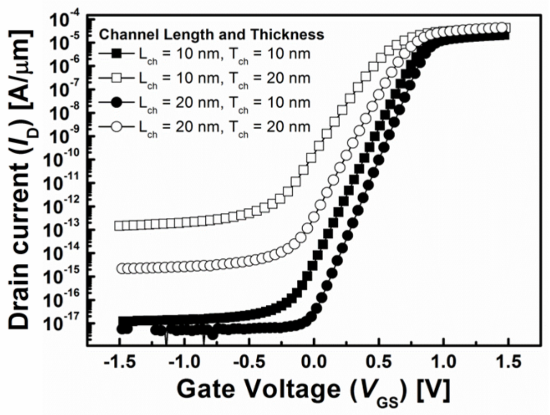


Fig. 4. Transfer curves of n-type Si JLFETs at V_{DS} = 0.85 V.

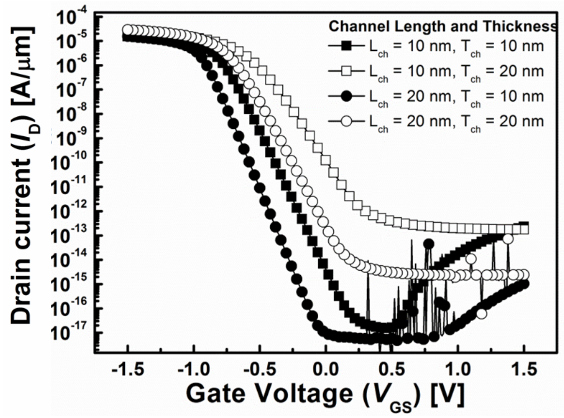


Fig. 5. Transfer curves of p-type Si JLFETs at V_{DS} = 0.85 V.

We also simulated Ge JLFETs for comparison. Fig. 6 and 7 respectively show the transfer curves of the n- and p-type Ge JLFETs, both having different L_{ch} and T_{ch} values at V_{DS} = 0.85 V. The Ge JLFET has a smaller difference between the on and off voltages and is suitable for ULP applications. However, I_{on} is lower in the n-type Ge JLFET compared with that in the n-type Si JLFET. Moreover, I_{on} and I_{off} in the p-type Ge JLFET are higher than I_{on} and I_{off} in the p-type Si JLFET. The Ge JLFET demonstrates higher I_{off} at the off-state according to hole current density because it mostly consists of minority carriers, as shown in Fig. 8.

In the simulation work, band-to-band tunneling model and quantum tunneling model were activated in order to get higher accuracy in evaluating the off-state current. However, it turned out that the off-state leakage mainly

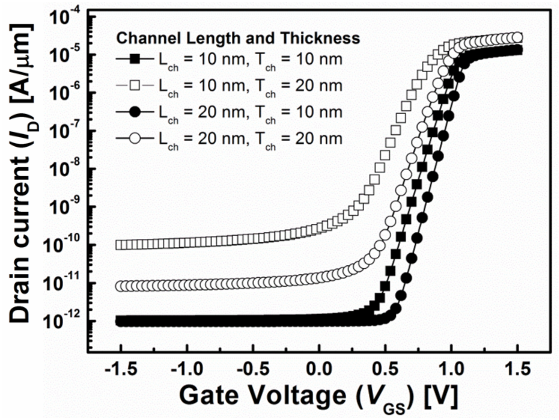


Fig. 6. Transfer curves of *n*-type Ge JLFETs at V_{DS} = 0.85 V.

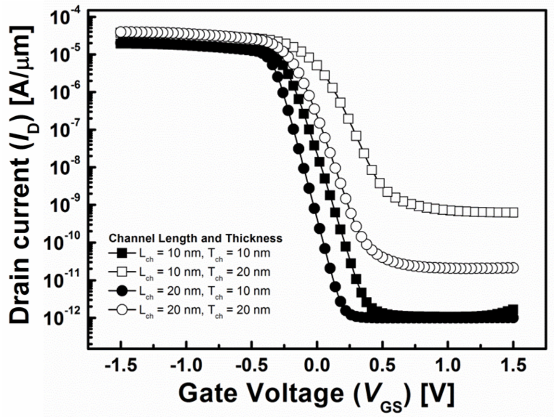


Fig. 7. Transfer curves of *p*-type Ge JLFETs at V_{DS} = 0.85 V.

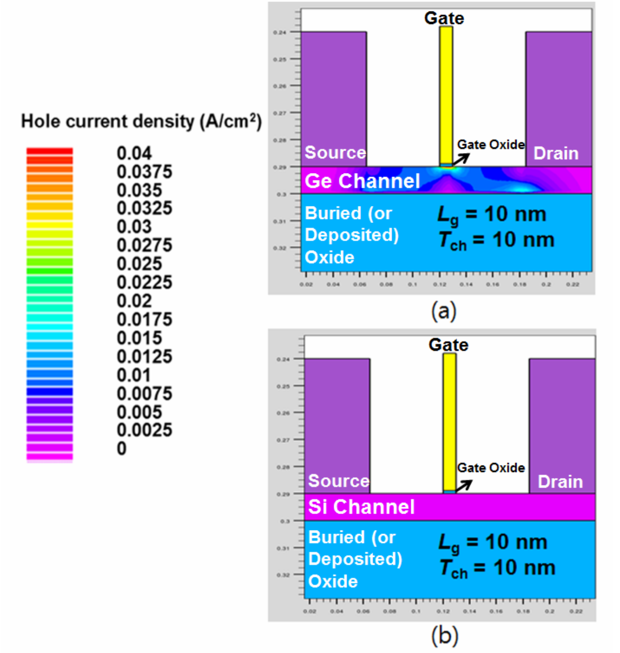


Fig. 8. Hole current density of *n*-type (a) Ge, (b) Si JLFETs in the off-states.

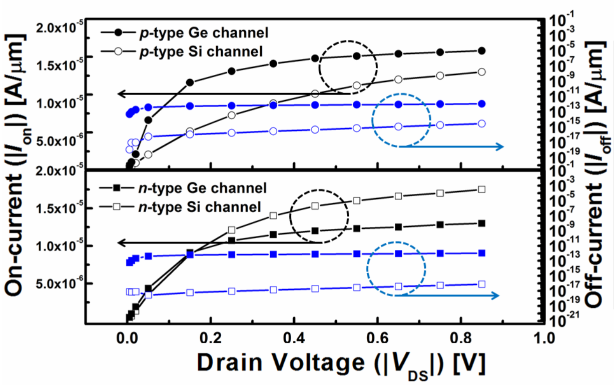
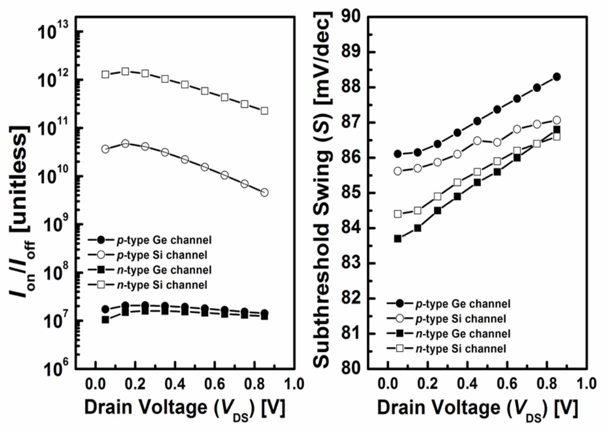


Fig. 9. On-state currents of *p*-type (upper) and *n*-type (lower) Ge and Si JLFETs as a function of V_{DS}.

comes from the drift and diffusion of minority carriers by switching on and off the tunneling models. No significant difference is found in case of *n*-type JLFETs. On the other hand, hole tunneling is clearly observed in case of *p*-type Si JLFET when the model is turned on. The tunneling current in the Ge device is not clearly distinguished since the tunneling component is buried in the drift-diffusion current of minority carriers. Thus, it can be judged that Ge JLFET is not superior in terms of off-state current due to its smaller energy bandgap, higher intrinsic carrier concentration, and higher minority carrier concentration, which leads to the higher off-state current by drift-diffusion of minority carriers. This is not as threatening as the leakage current by band-to-band tunneling in the off-state of the conventional MOSFET devices having anisotype junctions but surely needs to be controlled by more precisely prepared set of processing conditions.

Fig. 9 compares I_{on} and I_{off} of Si and Ge JLFETs as functions of V_{DS}. The I_{on} and I_{off} values were extracted not from fixed V_{GS} locations but from moving V_{GS} points, depending on device conditions for fair comparisons. This is because the gate work function is not tuned device-wisely for obtaining the same V_{th}; thus, V_{th} values from different JLFETs were not adjusted to a fixed value. Further, I_{on} and I_{off} were not measured at a set of fixed V_{GS} values, instead have been read at $V_{GS} = V_{th} + 0.5$ V and $V_{GS} = V_{th} - 0.7$ V, respectively. V_{th} was extracted by the constant-current method at the reference current $I_D = 10^{-6}$ A/μm. The *n*-type Si JLFET shows higher I_{on} for V_{DS} values than the Ge device because of its higher v_{sat} for electron (10^7 cm/s versus 6.3×10^6 cm/s). In contrast, the *n*-type Ge JLFET demonstrates higher I_{on} with $V_{DS} < 0.2$



(a) (b)

Fig. 10. DC parameters. (a) I_{on}/I_{off} ratio. (b) Subthreshold swing (S) of Ge and Si JLFETs as a function of V_{DS}.

V by using a higher μ_n.

For p-type junctionless FET, Ge device is superior to Si one in terms of I_{on} over the entire V_{DS} below 0.85 V. On the other hand, for n-type junctionless FET, Si device shows higher current drivability over most of the considered V_{DS} region than Ge one due to its higher saturation velocity of electron in spite of smaller electron mobility compared with Ge. However, I_{on} cross-over takes place at V_{DS} = 0.2 V. The absolute value of I_{on} drastically decreases below V_{DS} = 0.2 V, the Ge JLFET shows higher I_{on} than Si device. At this cross-over point, the higher electron mobility of Ge defeats the lower saturation velocity of electron in Ge, and the higher low-field electron velocity of Ge becomes the dominant factor in determining the I_{on}. The allowable current drivability needs to be further discussed in various aspects but it is revealed that Ge JLFET becomes more suitable for sub-0.5-V low-voltage operation than Si device.

Fig. 10(a) shows the I_{on}/I_{off} in comparison between Ge and Si JLFETs with different channel types. The n-type Si JLFET demonstrates the highest I_{on}/I_{off} ratio owing to higher saturation velocity of electron in Si and effectively suppressed I_{off} by the lower minority carrier concentration. Although I_{on}/I_{off} ratio of Ge JLFET is relatively low, it is insensitive to change in V_{DS}, which beneficially provides higher processing tolerance in the device-level implementation and stronger robustness against the electrical interference in the circuit-level operation. Si JLFET shows relatively smaller slopes in the S vs. V_{DS} as shown in Fig. 10(b). However, the deviations over either the entire V_{DS} region in consideration or the device types do not notably differ. Thus, including S in the respective of bias sensitivity may not be considered in designing the Ge JLFETs.

IV. CONCLUSION

In this work, we performed rigorous device design based on semiconductor-on-insulator platform and JLFET device structure, with a particular interest in Ge. The simulation results show that Ge JLFET has the strong potential in extending the Si CMOS technology for 10-nm-and-beyond nodes. For the CMOS extension, employing JLFET as the new vehicle will make a way out of the More-Moore technology track, and Ge will intimately cooperate with Si for ultra-low-power applications in both p- and n-type JLFETs. The proper time for active introduction of Ge depends not only on the mature low-temperature thin-film preparation and interface passivation techniques but also on the successful operation voltage scaling below 0.5 V.

ACKNOWLEDGMENTS

This work was supported by the National Research Foundation of Korea (NRF) and funded by the Korean Ministry of Science, ICT & Future Planning (NRF-2014R1A1A1003644).

REFERENCES

[1] R. Quay, C. Moglestue, V. Palankovski, and S. Selberherr, “A temperature dependent model for the saturation velocity in semiconductor materials,” *Mater. Sci. Semicond. Process.*, vol. 3, no. 1, pp. 149-155, Mar. 2000.

[2] C. Jacoboni, F. Nava, C. Canali, and G. Ottaviani “Electron drift velocity and diffusivity in germanium,” *Phys. Rev. B: Condens. Matter*, vol. 24, no. 2, pp. 1014-1026, Jul. 1981.

[3] C. Canali, G. Ottaviani and A. Quaranta, “Drift velocity of electrons and holes and associated anisotropic effects in silicon.” *J. Phys. Chem. Solids*, vol. 32, no. 8, pp. 1707-1720, Nov. 1970.

[4] S. Lee and S. Lee, “Accurate RF C-V method to extract effective channel length and parasitic capacitance of deep-submicron LDD MOSFETs,” *J.*

Semicond. Technol. Sci., vol. 15, no. 6, pp. 653-657, Dec. 2015.

[5] S. Kim, J. Seo, Y. Yoon, G. Yoo, Y. Kim, H. Eun, H. Kang, J. Kim, S. Cho, J. Lee, and I. Kang, "Design and Analysis of Sub-10 nm Junctionless Fin-Shaped Field-Effect Transistors," *J. Semicond. Technol. Sci.*, vol. 14, no. 5, pp. 508-517, Oct. 2014.

[6] F. Jazaeri, L. Barbut, A. Koukab, and J. Sallese, "Analytical model for ultra-thin body junctionless symmetric double gate MOSFETs in subthreshold regime," *Solid-State Electron.*, vol. 82, pp. 103-110, Apr. 2013.

[7] G. K. Celler and S. Cristoloveanu, "Frontiers of silicon-on-insulator," *J. Appl. Phys.*, vol. 93, no. 9, pp. 4955-4978, May 2013.

[8] J. Feng, Y. Liu, P. B. Griffin, and J. D. Plummer, "Integration of germanium-on-insulator and silicon MOSFETs on a silicon substrate," *IEEE Trans. Electron Devices*, vol. 27, no. 11, pp. 911-913, Nov. 2006.

[9] C. Sun, R. Liang, L. Liu, J. Wang, and J. Xu, "Effect of channel doping profiles on performance of germanium-on-insulator based junctionless transistors." *Proc. 2015 IEEE International Symposium on Next-Generation Electronics* (*ISNE*), Taipei, Taiwan, May 4-6, 2015, pp. 1-3.

[10] *International Technology Roadmap for Semiconductors* (*ITRS*), 2013 Edition, Online available at http://www.itrs2.net.

[11] S. Lee, H. Kim, J. Lee, I. Yu, J. Lee and C. Hwang, "Effects of O_3 and H_2O as oxygen sources on the atomic layer deposition of HfO_2 gate dielectrics at different deposition temperatures," *J. Mater. Chem. C*, vol. 24, no. 2, pp. 2558-2568, Jan. 2014.

[12] J. P. Colinge, C. W. Lee, N. Dehdashti, R. Yan, I. Ferain, P. Razavi, A. Kranti, and R. Yu, *Junctiobnless Transistors: Physics and Properties*, Springer-Verlag, Berlin, Germany, 2011.

[13] C. W. Lee, F. Isabelle, A. Aryan, Y. Ran, D. Nima, R. Pedram, and J. P. Colinge, "Performance estimation of junctionless multigate transistors," *Solid-State Electron.*, vol. 54, no.2, pp. 97-103, Feb. 2010.

[14] J. P. Colinge, C. W. Lee, A. Afzalian, N. Dehdashti, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A. Kelleher, B. McCarthy, and R. Murphy, "SOI gated resistor: CMOS without junctions," *Proc. 2009 IEEE International SOI Conference*, Foster City, USA, Oct. 5-8, 2009, pp. 1-2.

[15] S. M. Sze and J. C. Irvin, "Resistivity, mobility and impurity levels in GaAs, Ge, and Si at 300°K," *Solid State Electron.*, vol. 11, no. 6, pp. 599-602, Jan. 1968.

[16] P. P. Debye and E. M. Conwell, "Electrical properties of n-type germanium," *Phys. Rev. Appl*, vol. 93, no. 4, pp. 693-706, Feb. 1954.

[17] D. M. Caughey and R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *Proc. IEEE*, vol. 55, no. 12, pp. 2192-2193, Sep. 1967.

[18] G. Hellings, G. Eneman, R. Krom, B. D. Jaeger, J. Mitard, A. D. Keersgieter, T. Hoffmann, M. Meuris, and K. D. Meyer, "Electrical TCAD simulations of a Germanium pMOSFET technology," *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2539-2546, Oct. 2010.

[19] L. Reggiani, C. Canali, F. Nava, and G. Ottaviani, "Hole drift velocity in germanium," *Phys. Rev. B: Condens. Matter*, vol. 16, no. 6, pp. 2781-2791, Sep. 1977.

[20] S. A. Hareland, S. Jallepalli, G. Chindalore, W. K. Shih, A. F. Tasch, Jr., and C. M. Maziar, "A Simple Model for Quantum Mechanical Effects in Hole Inverson Layers in Silicon PMOS Device," *IEEE Transactions On Electron Devices*," vol. 44, no. 7, pp. 1172-1173, Jul. 1997.

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