

Effective Channel Mobility of AlGa_N/Ga_N-on-Si Recessed-MOS-HFETs

Hyun-Seop Kim, Seoweon Heo, and Ho-Young Cha*

Abstract—We have investigated the channel mobility of AlGa_N/Ga_N-on-Si recessed-metal-oxide-semiconductor-heterojunction field-effect transistors (recessed-MOS-HFET) with SiO₂ gate oxide. Both field-effect mobility and effective mobility for the recessed-MOS channel region were extracted as a function of the effective transverse electric field. The maximum field effect mobility was 380 cm²/V·s near the threshold voltage. The effective channel mobility at the on-state bias condition was 115 cm²/V·s at which the effective transverse electric field was 340 kV/cm. The influence of the recessed-MOS region on the overall channel mobility of AlGa_N/Ga_N recessed-MOS-HFETs was also investigated.

Index Terms—AlGa_N/Ga_N heterojunction field-effect transistor, SiO₂, Mobility, Recessed gate, MOS-HFET

I. INTRODUCTION

Gallium nitride (Ga_N) is an attractive material for use in high-power switching applications due to its high breakdown field and fast switching capability [1-3]. The biggest technical challenge in Ga_N power switching devices is the difficulty to achieve normally-off characteristics because of the polarization induced high carrier density at AlGa_N/Ga_N interface [4, 5]. One of common methods to achieve the normally-off characteristics is the recessed-MIS gate configuration where the AlGa_N barrier layer under the MIS gate region

was recessed either partially or completely [5-7]. Typically, the on-resistance values of recessed-MIS gate devices are much higher than that of conventional normally-on AlGa_N/Ga_N HFETs due to the limited carrier density and lower channel mobility. When the AlGa_N barrier layer is partially recessed maintaining a 2DEG channel at the interface between AlGa_N and Ga_N, it is difficult to achieve a high threshold voltage due to the high density of positive polarization charges at the AlGa_N/Ga_N interface; threshold voltages reported for this type of device are typically lower than 1 V [8-10]. In addition, the remaining AlGa_N layer thickness is only a few nm and thus the channel mobility will be influenced by scattering with MIS interface and fixed charges located very near the AlGa_N/Ga_N 2DEG channel. Such mobility degradation becomes even worse when the AlGa_N barrier layer is completely removed to ensure a high threshold voltage. In this case, the channel mobility will be significantly decreased due to the absence of 2DEG channel and strong scattering effects with interface charges existing at the recessed MIS channel itself. While great efforts have been made to improve the channel mobility of AlGa_N/Ga_N recessed-MIS devices [7, 11, 12], careful investigation on mobility characteristics have not been reported yet. In this work, we have investigated the channel mobility characteristics of normally-off AlGa_N/Ga_N-on-Si recessed-MOS-HFETs with SiO₂ gate oxide.

II. DEVICE FABRICATION

AlGa_N/Ga_N-on-Si epitaxial structure used in this work consisted of a 8 nm in-situ Si_N_x passivation layer, a 3.6 nm Ga_N capping layer, a 23.7 nm Al_{0.23}Ga_{0.77}N

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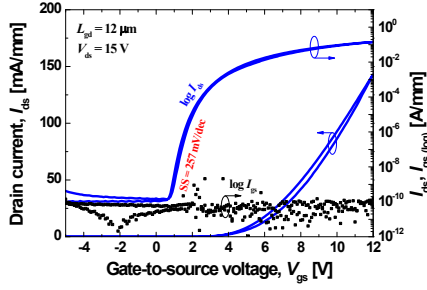


Fig. 1. Current-voltage characteristics of AlGaN/GaN-on-Si recessed-MOS-HFET.

barrier layer, a 1 nm AlN spacer, a 490 nm i-GaN layer, and a 4.4 μm GaN buffer layer on a Si (111) substrate. After solvent cleaning, recessed ohmic contacts [13] were formed using Cl₂/BCl₃ plasma etching followed by Ti/Al/Ni/Au (=20/120/25/50 nm) metal stack and rapid thermal annealing (RTA) at 800°C for 1 min in N₂ ambient. Both MESA isolation and gate recess were performed by Cl₂/BCl₃-based inductively coupled plasma reactive ion etch. The contact resistance measured after MESA isolation was 0.9 Ω·mm with the sheet resistance of 290 Ω/sq. A low power of 5 W was used for the gate recess to minimize the plasma induced damage and precisely control the etch depth. The AlGaN barrier layer was completely removed to ensure normally-off operation. After the sample was cleaned by solvent, a sacrificial oxidation process was carried out where the surface was oxidized by O₂ plasma treatment and thereafter etched back using diluted HF (1:10) prior to gate oxide deposition. A 20 nm SiO₂ gate oxide film was deposited using plasma enhanced chemical vapor deposition [14]. A Ni/Au (=20/200 nm) gate stack was deposited by e-beam evaporation. Finally, the post-metallization-annealing was carried out at 400°C for 10 min in O₂ ambient to improve the interface conditions [13].

III. RESULTS AND DISCUSSION

The current-voltage characteristics of a fabricated AlGaN/GaN recessed-MOS-HFET are shown in Fig. 1. The device had a source-to-gate distance of 3 μm, a recessed channel length of 2 μm, and a gate-to-drain distance of 12 μm. The recessed-MOS configuration resulted in a threshold voltage of > 2 V with negligible hysteresis. The ON/OFF current ratio was > 10⁹. The

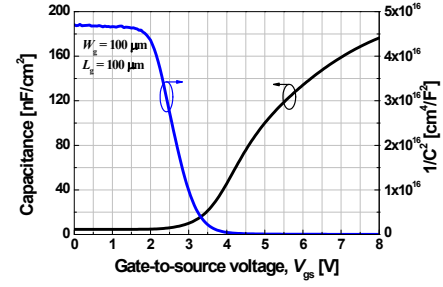


Fig. 2. Capacitance (C) and 1/C² versus gate bias voltage for a recessed-MOS-HFET.

subthreshold slope was 257 mV/dec from which the extracted interface state density was $\sim 2.21 \times 10^{12} \text{ cm}^{-2} \cdot \text{eV}^{-1}$.

A Fat FET device with a large channel length (100 × 100 μm²) was used to investigate the mobility characteristics for the recessed-MOS channel. The capacitance-voltage characteristics were measured to estimate the doping concentration of the GaN region under the recessed-MOS channel and the accumulation charge density at the MOS interface between SiO₂ and GaN as a function of the gate bias voltage. The bias dependent capacitance characteristics are shown in Fig. 2 along with 1/C² characteristics to derive the doping concentration of the recessed GaN layer. The derived doping concentration was $\sim 6 \times 10^{14} \text{ cm}^{-3}$. The channel charge density with a gate voltage of V_G for the accumulation MOS channel can be calculated by

$$Q_{G,n} = \int_{V_{TH}}^{V_G} C_{G,MOS} dV \quad (1)$$

where V_{TH} is the threshold voltage and $C_{G,MOS}$ is the MOS gate capacitance. The calculated channel carrier density $Q_{G,n}/e$ was $3.48 \times 10^{12} \text{ cm}^{-2}$ at the gate voltage of 8 V.

The current-voltage characteristics of the same device were measured to extract the mobility. The field-effect mobility (μ_{FE}) can be derived from the transconductance (dI_D/dV_G) whereas the effective mobility (μ_{eff}) is related to the drain conductance (dI_D/dV_D) as follows [15].

$$I_D = \frac{W \mu_{FE} C_{G,MOS}}{2L} [2(V_G - V_{TH})V_D - V_D^2] \quad (2a)$$

$$\mu_{FE} = \frac{(L/W)}{C_{G,MOS} V_D} \left. \frac{dI_D}{dV_G} \right|_{V_D \rightarrow 0} \quad (2b)$$

$$\mu_{eff} = \frac{(L/W)}{Q_{G,n}} \left. \frac{dI_D}{dV_D} \right|_{V_D \rightarrow 0} \quad (2c)$$

where I_D is the drain current, W is the channel width, L is the channel length, and V_D is the drain bias voltage.

The extracted μ_{FE} and μ_{eff} as a function of V_G is shown in Fig. 3(a) along with the corresponding current-voltage characteristics. Both μ_{FE} and μ_{eff} values decreased with increasing V_G because of the increased transverse electric field applied in the perpendicular direction from the channel. The maximum μ_{FE} was $380 \text{ cm}^2/\text{V}\cdot\text{s}$ at $V_G = 3 \text{ V}$ whereas the maximum μ_{eff} values were varied from 254 to $357 \text{ cm}^2/\text{V}\cdot\text{s}$ depending on how to define V_{TH} values. It should be noted that the sharp decrease in mobility values near threshold indicates strong scattering effects at MOS interface [16]. The dependency of μ_{eff} on V_{TH} at the gate bias voltage near the threshold condition was due to the different values of $Q_{G,n}$ calculated with different V_{TH} values. Such uncertainty, however, disappeared when V_G was sufficiently higher than V_{TH} . We selected the on-state gate bias voltage of 8 V from the gate oxide reliability point of view. It should be noted that μ_{eff} was higher than μ_{FE} at the on-state condition ($\mu_{FE} = 80 \text{ cm}^2/\text{V}\cdot\text{s}$ and $\mu_{eff} = 115 \text{ cm}^2/\text{V}\cdot\text{s}$ at $V_G = 8 \text{ V}$). While μ_{FE} is for simpler interpretation of experimental data that can be derived without knowing the threshold voltage, μ_{eff} would give more accurate prediction for current-voltage relationship [15, 17]. Therefore, attention should be paid more to μ_{eff} at the on-state condition than μ_{FE} near the threshold voltage. In order to investigate the effects of transverse electric field on effective mobility degradation, the effective transverse electric field (E_{eff}) was calculated by [15]

$$E_{eff} = \frac{Q_{G,n}}{2\epsilon_s} \quad (3)$$

where ϵ_s is the permittivity of semiconductor ($9.7 \times 8.85 \times 10^{-14} \text{ F/cm}$ for GaN). Since the MOS channel between SiO_2 and n-GaN is not an inversion channel but an accumulation channel, no depletion charge is considered to calculate the effective transverse electric field. The extracted mobilities versus effective transverse electric field are plotted in Fig. 3(b).

A bulk mobility of $\sim 1000 \text{ cm}^2/\text{V}\cdot\text{s}$ at room temperature was reported for unintentionally doped GaN [18]. Main scattering mechanisms to account for the mobility behavior are phonon scattering due to lattice vibration, Coulomb scattering due to various charge centers

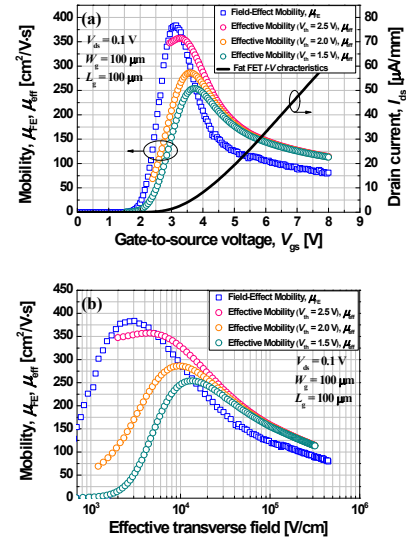


Fig. 3. Field-effect and effective mobilities extracted from Fat FET as a function of (a) gate bias voltage and (b) transverse electric field.

including fixed oxide charges, interface charges, ionized impurity charges, etc., and surface roughness scattering. According to the empirical mobility model used for Si, the maximum mobility has a hyperbolic form as a function of substrate doping concentration and fixed oxide and interface charges [16]. It was reported that the fixed oxide and interface charges near the MOS interface have strong influence on mobility; for example, significant mobility degradation was observed in Si MOSFET as the charge density increased beyond $\sim 10^{11} \text{ cm}^{-2}$ [15]. Based on Si empirical model, the mobility values extracted from AlGaIn/GaN recessed-MOS-HFET are within reasonable range because of its relatively higher interface state density. According to the conductance method, the interface state density for the fabricated device was estimated to be low $10^{12} \text{ cm}^{-2}\cdot\text{eV}^{-1}$, which is in agreement with the value extracted from subthreshold slope characteristics. Therefore, it is suggested that the significant degradation in mobility for AlGaIn/GaN recessed-MOS-HFET in comparison with bulk GaN was largely attributed to Coulomb scattering. It is expected that the mobility of the recessed-MOS channel region will be comparable to the bulk GaN mobility if the interface state density is decreased below $10^{11} \text{ cm}^{-2}\cdot\text{eV}^{-1}$.

Although the mobility of the recessed-MOS channel region is significantly lower than that of AlGaIn/GaN heterojunctions, it should be noted that the recessed-

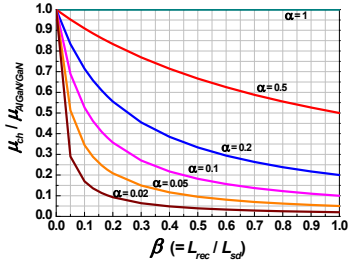


Fig. 4. Channel mobility degradation in AlGaIn/GaN recessed-MOS-HFET as functions of α ($= \mu_{MOS}/\mu_{AlGaIn/GaN}$) and β ($= L_{rec}/L_{sd}$).

MOS channel region occupies only a small fraction of the source-to-drain distance of MOS-HFET and thus the influence on the overall mobility and on-resistance will be mitigated. The overall effective channel mobility μ_{ch} between source and drain with the recessed-MOS gate can be expressed by

$$\frac{L_{sd}}{\mu_{ch}} = \frac{L_{sd} - L_{rec}}{\mu_{AlGaIn/GaN}} + \frac{L_{rec}}{\mu_{MOS}} \quad (4a)$$

$$\mu_{ch} = \mu_{AlGaIn/GaN} \left(\frac{\alpha}{\alpha + \beta(1 - \alpha)} \right) \quad (4b)$$

where $\mu_{AlGaIn/GaN}$ and μ_{MOS} are the mobilities for AlGaIn/GaN heterojunction and recessed-MOS channel, respectively, L_{sd} is the source-to-drain distance, L_{rec} is the recessed-MOS channel length, α is the ratio of the recessed-MOS channel mobility to AlGaIn/GaN heterojunction mobility ($\mu_{MOS}/\mu_{AlGaIn/GaN}$), and β is the ratio of the recessed-MOS channel length to the source-to-drain distance (L_{rec}/L_{sd}). Decrease in overall channel mobility as functions of α and β is plotted in Fig. 4. For example, when $\alpha = \beta = 0.1$, the overall channel mobility μ_{ch} will be decreased by $\sim 50\%$. If the recessed-MOS channel mobility were improved close to the bulk GaN mobility ($\sim 1000 \text{ cm}^2/\text{V}\cdot\text{s}$, i.e., $\alpha \sim 0.5$), the overall mobility will approach $\sim 90\%$ of AlGaIn/GaN heterojunction mobility when $\beta = 0.1$.

IV. CONCLUSIONS

While a recessed-MOS gate configuration enables a high threshold voltage of AlGaIn/GaN HFETs, the absence of 2DEG channel and scattering with fixed and interface charges near and at the MOS channel significantly degrade the recessed-MOS channel mobility.

The mobility for the recessed-MOS channel with SiO₂ gate oxide was investigated as a function of transverse electric field. The maximum field-effect mobility was $380 \text{ cm}^2/\text{V}\cdot\text{s}$ near the threshold voltage and the effective mobility was $115 \text{ cm}^2/\text{V}\cdot\text{s}$ at the on-state condition. Since the recessed-MOS channel mobility is a strong function of scattering centers existing near the channel, great care must be taken of processing technology to minimize the fixed and interface charges and the influence of the recessed-MOS channel mobility on the overall channel mobility of AlGaIn/GaN MOS-HFET must be taken carefully into account for device modeling.

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REFERENCES

- [1] U. K. Mishra, et al, "AlGaIn/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE*, Vol. 90, No. 6, pp. 1022-1031, Jun., 2002.
- [2] J. -G. Lee, et al, "State-of-the-Art AlGaIn/GaN-on-Si Heterojunction Field Effect Transistors with Dual Field Plates," *Applied Physics Express*, Vol. 5, No. 6, p. 066502, Jun., 2012.
- [3] S. -W. Han, et al, "Dynamic on-resistance of normally-off recessed AlGaIn/GaN-on-Si metal-oxide-semiconductor heterojunction field-effect transistor," *Applied Physics Express*, Vol. 7, No. 11, p. 111002, Nov., 2014.
- [4] O. Ambacher, et al, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaIn/GaN heterostructures," *Journal of Applied Physics*, Vol. 87, No. 1, pp. 334-344, Jan., 2000.
- [5] B. -R. Park, et al, "High-Quality ICPCVD SiO₂ for Normally Off AlGaIn/GaN-on-Si Recessed

- MOSHFETs," *IEEE Electron Device Letters*, Vol. 34, No. 3, pp. 354-356, Mar., 2013.
- [6] W. Choi, et al, "Improvement of V_{th} instability in normally-off GaN MIS-HEMTs employing PEALD-SiN_x as an interfacial layer," *IEEE Electron Device Letters*, Vol. 35, No. 1, pp. 30-32, Jan., 2014.
- [7] Y. Wang, et al, "High-Performance Normally-Off Al₂O₃/GaN MOSFET Using a Wet Etching-Based Gate Recess Technique," *IEEE Electron Device Letters*, Vol. 34, No. 11, pp. 1370-1372, Nov., 2013.
- [8] Q. Zhou, et al, "High-Performance Enhancement-Mode Al₂O₃/AlGaN/GaN-on-Si MISFETs With 626 MW/cm² Figure of Merit," *IEEE Transactions on Electron Devices*, Vol. 62, No. 3, pp. 776-781, Mar., 2015.
- [9] K. Ota, et al, "A normally-off GaN FET with high threshold voltage uniformity using a novel piezo neutralization technique," *2009 IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, Dec., 2009.
- [10] T. -L. Wu, et al, "Time dependent dielectric breakdown (TDDb) evaluation of PE-ALD SiN gate dielectrics on AlGaN/GaN recessed gate D-mode MIS-HEMTs and E-mode MIS-FETs," *2015 IEEE International Reliability Physics Symposium (IRPS)*, pp. 6C.4.1-6C.4.6, Apr., 2015.
- [11] S. Liu, et al, "Al₂O₃/AlN/GaN MOS-Channel-HEMTs With an AlN Interfacial Layer," *IEEE Electron Device Letters*, Vol. 35, No. 7, pp. 723-725, Jul., 2014.
- [12] Z. Xu, et al, "Fabrication of Normally Off AlGaN/GaN MOSFET Using a Self-Terminating Gate Recess Etching Technique," *IEEE Electron Device Letters*, Vol. 34, No. 7, pp. 855-857, Jul., 2013.
- [13] J. -G. Lee, et al, "Investigation of flat band voltage shift in recessed-gate GaN MOSHFETs with post-metallization-annealing in oxygen atmosphere," *Semiconductor Science and Technology*, Vol. 30, No. 11, p. 115008, Nov., 2015.
- [14] J. -G. Lee, et al, "High quality PECVD SiO₂ process for recessed MOS-gate of AlGaN/GaN-on-Si metal-oxide-semiconductor heterostructure field-effect transistors," *Solid-State Electronics*, Vol. 122, pp. 32-36, Aug., 2016.
- [15] S. C. Sun, et al, "Electron Mobility in Inversion and Accumulation Layers on Thermally Oxidized Silicon Surfaces," *IEEE Transactions on Electron Devices*, Vol. ED-27, No. 8, pp. 1497-1508, Aug., 1980.
- [16] F. Gámiz, et al, "Effects of bulk-impurity and interface-charge on the electron mobility in MOSFETs," *Solid-State Electronics*, Vol. 38, No. 3, pp. 611-614, Mar., 1995.
- [17] J. S. Kang, et al, "Effective and field-effect mobilities in Si MOSFETs," *Solid-state Electronics*, Vol. 32, no. 8, pp. 679-681, 1989.
- [18] V. W. L. Chin, et al, "Electron mobilities in gallium, indium, and aluminum nitrides," *Journal of Applied Physics*. Vol. 75, No. 11, pp. 7365-7372, 1994.



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