Analysis of an Active Superconducting Current Controller (ASCC) Considering the Transient Stability and OCR Operation in Transmission and Distribution Systems

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Abstract – The Active Superconducting Current Controller (ASCC) is a new type of Superconducting Fault Current Limiters (SFCL) which can limit the fault current in different modes. It also has the particular abilities of compensating active and reactive powers for electrical networks. In this paper, it is confirmed that the performance of ASCC in different operating modes introduces a limiting impedance in series with the network which can even degrade the transient stability and the operation of the Over-Current Relays (OCR) employed in a power system. In addition, the model of a three-phase ASCC is simulated, and the effect of descriptive modes on the current limiting level is investigated. For the transient stability analysis, a single machine-infinite bus system is tested, and the effect of operation modes is studied based on an equal area criterion obtaining the critical time and the critical angle. Modifying the setting parameters of OCR such as time dial and pick-up current, the protective coordination is also studied in different operating modes.

Keywords: Active superconducting current controller, Fault current limiters, Over-current relay, Transient stability, Distribution system.

1. Introduction

The recent growth of power generation capacity and the interconnections of networks have brought about an increase of short circuit capacity in the power system. The application of Fault Current Limiters (FCLs) can be an effectual solution for this problem [1]. Many researches have introduced different types of FCLs. These equipments have a low resistance against the line current in the normal states and suddenly represent a large resistant against the current when a fault is occurred. In the past two decades, discovering High-Temperature Superconductors (HTS), several circuits for limiting the fault current such as the resistive HTS FCL, inductive FCLs, asymmetric flux, and saturated-core have been presented [2-3].

The combination of superconductive technology and power electronics has introduced a new generation of series compensation as ASCC, which can descend the fault current in different levels and also compensate active and reactive powers. [4-8].

Several researches have presented ASCC for reducing the fault current. In [1, 4-7], just modeling and advantages of ASCC in a simple three-phase circuit have been described, although its negative effects have not been studied. In [9],

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just positive effects of ASCC on transient stability have been studied. However, the negative effects of ASCC on the transient stability have not been considered so far. Moreover, in [12-15], protective coordination of fixed impedance type FCLs with OCR has been evaluated, and as far as the authors are aware, the protective coordination of different operating modes of ASCC and OCRs has not been reported yet.

In consideration of above-mentioned, the main contribution of the current study is to evaluate ASCC effects on transient stability of a single-machine infinite bus system and protective coordination of ASCC with OCR in a typical distribution system. In addition, the simulation results from MATLAB confirm the presented method.

2. Description and Modeling

Fig. 1 shows a structure of an ASCC, which is employed in a typical three-phase circuit. According to Fig. 1, the ASCC consists of three superconducting transformers and one three-phase voltage source inverter [4]. In normal conditions, the primary voltage should be compensated to zero. In case of a short circuit, the limiting impedance can be controlled to decrease the fault current in different levels through controlling the compensation current (second current of superconducting transformer) [6-7].

2.1 ASCC MODELING

In Fig. 1, L_{s1} , L_{s2} , and M_S are self-inductance and

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Fig. 1. The structure of a three-phase ASCC.

mutual-inductance of the superconducting windings. In addition, Z_1 and Z_2 are the circuit and load impedances, and C_1 and C_2 are DC link capacitors. Moreover, L_d and C_d have been designed for filtering the high order harmonics. The three-phase PWM converter with the DC link capacitors is connected in parallel with the secondary winding of each superconducting transformer. In this paper, phase A is studied for the sake of the simplicity. The primary voltage of the superconducting transformer is expressed as follow [5-7]:

$$U_A = j\omega L_{S1}I_A - j\omega M_S I_a \tag{1}$$

$$L_{S1} = L_1 + M_S \tag{2}$$

To neutralize the effect of ASCC in normal conditions, I_a should be adjusted as:

$$I_{a} = \frac{L_{s1}}{M_{s}} I_{A} = \frac{L_{s1}}{M_{s}} \left(\frac{U_{sA}}{Z_{1} + Z_{2}} \right)$$
(3)

When a fault occurs, the fault current without ASCC, with ASCC, and the limiting impedance (Z_{ASCC}) is defined as:

$$I_{Af-noASCC} = \frac{U_{SA}}{Z_1} \tag{4}$$

$$I_{Af-withASCC} = \frac{U_{SA} + j\omega M_S I_a}{Z_1 + j\omega L_{S1}}$$
(5)

$$Z_{ASCC} = \frac{U_{Af}}{I_{Af}} = j\omega L_{S1} - \frac{j\omega M_S I_a (Z_1 + j\omega L_{S1})}{U_{SA} + j\omega M_S I_a}$$
(6)

According to (5), by adjusting the secondary winding current (I_a) , three different modes are obtained from the operation of ASCC under fault conditions [6-8].

Mode 1: I_a is kept at the original setting:

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$$I_{Af-1} = \frac{U_{SA} + j\omega L_{S1}I_{A}}{Z_{1} + j\omega L_{S1}}$$
(7)

$$Z_{ASCC-1} = \frac{Z_2(j\omega L_{s1})}{Z_1 + Z_2 + j\omega L_{s1}}$$
(8)

Mode 2: the amplitude of I_a is set at zero:

$$Z_{ASCC-2} = j\omega L_{S1} \tag{9}$$

Mode 3: I_a is regulated so that the angle difference between U_{SA} and $j \omega M_S I_a$ is measured 180°, which is obtained by setting $j \omega M_S I_a = -KU_{SA}$. In this mode, the fault current and the ASCC impedance are defined as follows:

$$I_{Af-3} = \frac{U_{SA} - \omega M_S \left| I_a \right|}{Z_1 + j\omega L_{S1}} \tag{10}$$

$$Z_{ASCC-3} = \frac{K}{1-K} Z_1 + \frac{1}{1-K} j\omega L_{S1}$$
(11)

2.2 Control strategy

In this section, a double-loop control strategy is briefly described, and the reader is referred to [7] for more details. According to Fig. 1, current and voltage equations are obtained as follows:

$$\begin{cases}
L_d \frac{di_{sa}}{dt} = u_{sa} - u_a \\
L_d \frac{di_{sb}}{dt} = u_{sb} - u_b \\
L_d \frac{di_{sc}}{dt} = u_{sc} - u_c \\
\end{cases}$$

$$\begin{cases}
C_d \frac{du_a}{dt} = i_{sa} - i_a \\
C_d \frac{du_b}{dt} = i_{sb} - i_b \\
C_d \frac{du_c}{dt} = i_{sc} - i_c
\end{cases}$$
(12)

Further, the mathematical equations in dq0 reference frame can be achieved by:

$$\begin{cases}
L_d \frac{di_{sd}}{dt} = \omega L_d i_{sq} + u_{sd} - u_d \\
L_d \frac{di_{sq}}{dt} = -\omega L_d i_{sd} + u_{sq} - u_q \\
L_d \frac{di_{s0}}{dt} = u_{s0} - u_0
\end{cases}$$
(14)

$$\begin{cases} C_d \frac{du_d}{dt} = \omega C_d u_q + i_{sd} - i_d \\ C_d \frac{du_q}{dt} = -\omega C_d u_d + i_{sq} - i_q \\ C_d \frac{du_0}{dt} = i_{s0} - i_0 \end{cases}$$
(15)

According to (14) and (15), after dq0 transformation, control system of the converter is composed of coupling dq0 axes. Since the injected currents (i_a, i_b, i_c) will be unbalanced under unsymmetrical fault, not only the sum of U_{dc1} and U_{dc2} should be controlled to remain the same, but also the voltage balance control for the DC link capacitors should be considered. The DC link voltage equation can be obtained by:

$$\begin{cases} u_{dc1} + u_{dc2} = u_{dc} \\ C_2 \frac{du_{dc2}}{dt} - C_1 \frac{du_{dc1}}{dt} = 3(i_0 + C_d \frac{du_0}{dt}) \end{cases}$$
(16)

Based on (14-16), control system of a three-phase converter can be shown in Fig. 2.



Fig. 2. Control strategy for a three-phase PWM converter.

The current reference signals $(I_{abc-ref})$ are determined based on operating state of the main circuit and currentlimiting mode of the ASCC. Consequently, the reference currents and voltages are calculated. Finally, the voltage reference signals of the converter can be obtained by dq0abc transformation.

3. Transient Stability Analysis

The operation of ASCC in different modes creates a limiting impedance in series with the network, influencing the transient stability as a result. When the ASCC increases transfer power during the fault, transient stability is improved, and if the limiting impedance increases the total equivalent reactance, the power-angle curve during a fault will come down. Under such conditions, ASCC will have a negative effect on the transient stability.



Fig. 3. System diagram for transient stability analysis

In other words, to study the effects of ASCC on transient stability in more details, the model shown in Fig. 3 has been created in which the ASCC is installed between the bus line and secondary side of the main transformer.

When the fault occurs at the point F1, the sending end of the line, the exported electromagnetic power will be zero, but when ASCC is employed, we have [9]:

$$P_{e} = \operatorname{Re} al(EI^{*}) = \frac{E^{2}R_{SCC}}{R_{ASCC}^{2} + (X_{d}^{'} + X_{T} + X_{ASCC})^{2}}$$
(17)

As shown in (17), ASCC increases the electromagnetic power during the fault, and so it improves the transient stability. Suppose now that the fault occurs at alongside of the lines (point F2). The power-angle equation, during the fault, can be obtained as shown in (18):

$$P_2 = \frac{\left| E' \right| \left| V \right|}{X_{AB}} \sin \delta \tag{18}$$

where

$$X_{AB} = \frac{(X_{d} + X_{T} + X_{ASCC})(X_{L})(1+P) + (X_{L})(PX_{L})}{(PX_{L})}$$
(19)

According to (19), the limiting impedance of ASCC increases the equivalent reactance. Therefore, ASCC has a negative effect on the transient stability in this case.

4. Analysis of Overcurrent Relay Operation

The structure of a distribution system with ASCC is shown in Fig. 4. An OCR is installed at the secondary-side of the main transformer to generate the trip signals for circuit breakers [11-13]. The limiting impedance of ASCC (Z_{ASCC}) can be obtained in (20):

$$Z_{ASCC} = \frac{u_{1af}}{i_{1af}} = j\omega L_{S1} - \frac{j\omega M_S i_{2a} (Z_S + Z_{Tr} + j\omega L_{S1})}{u_{SA} + j\omega M_S i_{2a}}$$
(20)

The limiting impedance in three modes is obtained according to (21-23):

$$Z_{ASCC-1} = \frac{(Z_{eq} j\omega L_{S1})}{(Z_{S} + Z_{Tr} + Z_{eq} + j\omega L_{S1})}$$
(21)



Fig. 4. Schematic configuration of distribution system [11].

$$Z_{ASCC-2} = j\omega L_{S1} \tag{22}$$

$$Z_{ASCC-3} = \frac{K}{1-K} (Z_S + Z_{Tr}) + \frac{1}{1-K} j\omega L_{S1}$$
(23)

The over current relays are considered as one of the most significant protection devices of the power distribution systems. The OCR's operations are divided into the instant time and delay time operations. The OCR sends the trip signal to the circuit breaker (CB) for removing the fault area from the power system. The operation time of the OCR is defined by the current ratio between the setting pick up current (Ipickup) and the input current (Iinput). Besides, time dial (TD) moves the curve to up or down for the protection coordination. Therefore, both the parameters, Ipickup and TD, can be adjusted to meet protection coordination. For modeling the OCR to protect the power distribution system, the operational equations of OCR can be obtained as follows:

$$Time_{trip} = \left(\frac{A}{M^P - 1} + B\right) * TD \tag{24}$$

$$M = \frac{I_{input}}{I_p}$$
(25)

In (24), A, B, and P are constants which are determined based on the type of relays. In this paper, the constants are decided by U.S. very inverse type, and they are shown in Table 1. According to (25), I_{input} is equal to the fault current, and Ip is one of the setting parameters of OCR. In addition,

 Table 1. Detailed specifications of distribution system and OCR.

Configuration components	Parameters	
Source	154 (KV), 1.75 (%)	
Transformer	154/22.9(KV), 100 (MVA), j20 (%)	
Distribution line	Z ₀ =8.68+j22.86(%), 100MVA Z ₁ =Z ₂ =3.48+j7.44(%) 100MVA	
	Feeder1: 10MVA, pf=0.95 Lag	
	Feeder2: 7MVA, pf=0.95 Lag Feeder3:9MVA,	
Loads	pf=0.95 Lag Feeder4:8MVA, <i>pf</i> =0.95	
	Lag Feeder5:8 (MVA), pf=0.95 Lag	
Over-current relay	Load Current=1.13(KA) _{rms} Full Load Current=	
	1.51(KA) _{rms} Pickup Current : 2.1(KA) _{rms}	
	A=3.88, B=0.0963, P=2, TD=0.4	
SFCL parameters	$L_{s1} = L_{s2} = 5 \text{ (mH)}, M_s = 4 \text{ (mH)}$	

TD which is another setting parameter of OCR is set for protective coordination. In order to provide a comparison of different operating modes of ASCC, the protection coordination of ASCC under the different current limiting modes is carried out by adjusting the TD and Ip through analysis on the TCC curves. The operational equations of OCR, without ASCC and in the presence of ASCC based on ASCC modes, are obtained as follows:

$$\left((Time_{trip})_{WTTHOUT-ASCC} = \left(\frac{A}{(\frac{U_{SA}}{Z_{1}I_{pickup}})^{P}-1} + B\right) * TD$$

$$\left((Time_{trip})_{ASCC-1} = \left(\frac{A}{(\frac{U_{SA}+j\omega L_{S1}I_{A}}{(Z_{1}+j\omega L_{S1})I_{pickup}})^{P}-1} + B\right) * TD$$

$$\left((Time_{trip})_{ASCC-2} = \left(\frac{A}{(\frac{U_{SA}}{(Z_{1}+j\omega L_{S1})I_{pickup}})^{P}-1} + B\right) * TD$$

$$\left((Time_{trip})_{ASCC-3} = \left(\frac{A}{(\frac{U_{SA}-\omega M_{S}|I_{a}|}{(Z_{1}+j\omega L_{S1})I_{pickup}})^{P}-1} + B\right) * TD$$

$$\left((Time_{trip})_{ASCC-3} = \left(\frac{A}{(\frac{U_{SA}-\omega M_{S}|I_{a}|}{(Z_{1}+j\omega L_{S1})I_{pickup}})^{P}-1} + B\right) * TD$$

Eq. (26) shows that reducing fault current increases the trip time of OCR so that ASSC with mode 3 provides the largest trip time of OCR. Consequently, the OCR setting parameters are fixed based on the mode that provides the most effect on current limiting.

5. Simulation Results

In this section, simulation results for evaluating the performance of the ASCC in different modes, based on fault current limiting, transient stability, and OCR operation, under the same conditions are carried out.

5.1 Current limiting test

At first, to assess the performance of three aforementioned modes on current limiting, the circuit shown in Fig. 1 along with control system shown in Fig. 2 with the parameters in Table 2 are simulated in MATLAB/ SIMULINK software. In order to evaluate and compare the

Table 2. Parameters of simulated system.

Parameter	Value
$[U_{SA}, U_{dc}]$	[220,600] (V)
Z_I	0.19 + 2.16 i (Ω)
Z_2	$15 + 2 i (\Omega)$
F	50 (Hz)
$Ls_1 = Ls_2$	10 (mH)
$[M_s, L_f]$	[9, 6] (mH)
$C_1 = C_2$	2000 (µF)
C_f	30 (µF)

effects of its different modes, the fault current waveforms, without ASCC and with ASCC are shown in Fig. 5. Based on Fig. 5, it can be observed that mode 3 has the best effect on reducing the fault current, as it is expected.

Fig. 6(a) shows reference currents of Fig. 1 in normal state of ASCC operation. According to (3), compensator currents are so that ASCC has no effect on the main circuit in normal state. Fig. 6(b) depicts the reference currents when a three-phase fault is occurred and ASCC operates in mode 3. Fig. 6(c) shows the reference currents for a single-phase fault, and they are asymmetrical currents. Fig. 6(d) shows the voltage of DC link capacitors under a single-phase fault, and it illustrates that AC components of U_{dc1} and U_{dc2} are opposite with each other, and total DC voltage can be kept 600 V.

Fig. 7 shows the effect of the magnitude and phase angle of compensating current (Ia) on current limiting. It is obvious that the best limiting effect is obtained for the



Fig. 5. The comparison of the fault current characteristics



Fig. 6. The reference currents for control system for (a): normal state; (b) three-phase fault; (c) single-phase fault, and (d) DC link voltage of converter in a single-phase fault.



Fig. 7. Relations between I_{A-peak} and phase of I_a



Fig. 8. (a): The power-angle curves for a fault at sending end, the first swing waveforms of power angle; (b): without the ASCC; (c): with the ASCC operated in Mode 1.

phase angle of Ia equal to 90°. Besides, increasing the magnitude of compensating current improves the effect of fault current limiting.

5.2 Transient stability test

To study the effect of ASCC on transient stability, the model shown in Fig. 3 is simulated. The self- and the mutual-inductances of ASCC are $L_1 = L_2 = 5$ (mH), $M_s = 5$ (mH), respectively. The power-angle curve and the first swing waveforms of power angle, based on different critical times, without the ASCC and with the ASCC operated in Mode 1 are shown in Fig. 8. According to Fig. 8(a), the critical clearing angle without the ASCC is 84.77°.



Fig. 9. The power-angle curves when a fault is occurred in the middle of the line and ASCC operates in (a) : mode 1 (b): mode 2 (c): mode 3.

According to (17), it can be reported that when the ASCC operates in mode 1, the electrical power during the fault rises to 0.2 (Pu). Therefore, the critical clearing angle increases to 92.390°. In Figs. 8(b) and 8(c), the critical clearing times without and with ASCC are 0.26 (Sec) and 0.32 (Sec), respectively. It verifies that the transient stability is improved with the ASCC when a fault is occurred at the sending-end. In the second case, that is related to a fault occurred in the middle of lines, the equivalent reactance is 1.8 (Pu), and the power-angle equation during the fault is defined as: $Pe = 0.65 \sin \delta$. The power-angle curves for this case study are shown in Fig. 9. Based on Fig. 9(a), the critical clearing angle and time without ASCC are, respectively, equal to 98.83 ° and 0.4 Sec. If it operates in mode1, the limiting impedance is equal to $Z_{ASCC1} = 0.074 +$ 0.089 i (Pu), in which case the equivalent reactance rises to 2.07 (Pu), and consequently the power-angle curve during the fault is defined as: $Pe = 0.56 \sin \delta$. The critical clearing angle and time are decreased to 93.1° and 0.37 (Sec), respectively. In mode 2, as shown in Fig. 9(b), the limiting impedance is equal to $Z_{ASCC2} = 0.17$ i (Pu), and the equivalent reactance rises to 2.31 (Pu).

It results that the critical clearing angle and time in mode 2 are decreased to 89.7° and 0.34 (Sec), respectively. Therefore, the ASCC imposes a more degrading effect on transient stability rather than mode 1. Finally, when the ASCC operates in mode 3, Fig. 9(c) shows that by setting the limiting impedance to $Z_{ASCC3} = 0.029 + 0.311$ i (Pu), the equivalent reactance rises to 2.73 (Pu), and the critical angle and time are decreased to 85.9° and 0.31 Sec, respectively. It confirms that mode 3 has more negative effects on transient stability compared to modes 1 and 2, when the fault occurred in the middle of the line.

5.3 Over-current relay operation

The simulated parameters of the distribution systems for



Fig. 10. The TCC of OCR operation for the protective coordination with ASCC operation: (a) original setting of OCR; (b) only modifying the TD; (c) modifying both TD and Ip for mode 3; (d) modifying both TD and Ip for protective coordination in three modes.

 Table 3. The trip time of OCR based on different values of setting parameters of OCR.

OCR Parameters		Trip time Mode (1)	Trip time Mode (2)	Trip time Mode (3)
Ip=2.1 (KA) _{rms}	TD=0.5	1.34	1.53	2.86
	TD=0.4	1.07	1.22	2.28
	TD=0.3	0.807	0.92	1.71
	TD=0.2	0.54	0.61	1.14
	TD=0.1	0.27	0.305	0.57
Ip=1.9 (KA) _{rms}	TD=0.1	0.19	0.2	0.38
	TD=0.2	0.38	0.4	0.76

testing OCR operation are expressed in Table 1. In addition, The ASCC parameters for a fault occurred at the point F of Fig. 4 are stated. TCC of OCR by applying the ASCC in different operating modes are shown in Fig. 10(a). Fig. 10(b) shows the TCC with different values of TD when the ASCC operates in three modes. When the ASCC operates in mode 3, modifying the TD value to "0.1", the operation time of OCR is decreased to 0.57 (Sec), and thus in this mode, Adjusting the other setting parameter of OCR (Ip) is required. According to Fig. 10(c), when the TD value of the OCR is modified from "0.5" to "0.1" and the Ip is also modified from "2.1" to "1.9", the protection coordination in three operation modes is confirmed. Fig. 10(d) verifies the protective coordination by modifying both setting parameters of OCR in three operation modes. According to Fig. 10(d), by modifying TD and Ip values to "0.2" and "1.9", respectively, the protective coordination in mode 1 and mode 2 are confirmed as well. The coordination in mode 3 is confirmed through adjusting TD and Ip values to "0.1" and "1.9", respectively.

The trip time of OCR based on the different setting parameters (TD and Ip) are also expressed in Table 3.

Based on Table 3, by setting Ip = 2.1 (KA), for TD=0.2 the protective coordination can be obtained for modes 1 and 2, and for mode 3, the protective coordination is obtained by adjusting TD=0.1. In addition, by reducing Ip to 1.9, the trip time is more reduced.

6. Conclusion

In this paper, the effects of ASCC on current limiting, transient stability, and OCR operation are analyzed. Test results show that the ASCC rapidly suppresses the fault current to different levels by adjusting the amplitude and the phase angle of the compensation current. According to the case study, for the faults at the sending end of the line, ASCC improves transient stability. However, when the fault occurs at the alongside of a line, the equivalent reactance increases, and the critical clearing angle and time decrease. Therefore, the ASCC degrades the transient stability. The modified values of TD and IP for the protective coordination with OCR are also obtained through analysis of TCC in three operation modes of ASCC. For a suitable use, the limiting impedance of ASCC should be set so that the fault current is reduced to an appropriate level, the transient stability is less affected and the protective coordination of protective devices is obtained without changing the relay and only with adjusting the setting parameters of relay.

7. Symbols

- (L_1, M_s) : The self- and the mutual-inductances of ASCC.
- (Z_1, Z_2) : The line and load impedances.
- $(I_{Af-1}, I_{Af-2}, \text{ and } I_{Af-3})$: The fault current in modes 1, 2, and 3.
- ΔI : The amplitude of error between the instantaneous and steady-state current.
- $\Delta i_{threshold}$: The threshold of error between the instantaneous and steady-state current.
- (R_{ASCC}, X_{ASCC}) : The real and imaginary parts of ASCC impedance.
- X'_d : The transient reactance of generator.
- (X_T, X_L) : The transformer and line reactances.
- (X_{AB}, V) : equivalent reactance between sending end and infinitive bus and voltage of infinitive bus.
- Z_{Tr} : The distribution transformer impedance.
- Z_{eq} : The equivalent impedance in distribution system.
- M : multiple of current.
- (I_{input}, I_p) : The fault current and the pick-up current of OCR.

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