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# A Novel High Step-Up Converter with a Switched-Coupled-Inductor-Capacitor Structure for Sustainable Energy Systems

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#### **Abstract**

A novel step-up DC-DC converter with a switched-coupled-inductor-capacitor (SCIC) which successfully integrates three-winding coupled inductors and switched-capacitor techniques is proposed in this paper. The primary side of the coupled inductors for the SCIC is charged by the input source, and the capacitors are charged in parallel and discharged in series by the secondary windings of the coupled inductor to achieve a high step-up voltage gain with an appropriate duty ratio. In addition, the passive lossless clamped circuits recycle the leakage energy and reduce the voltage stress on the main switch effectively, and the reverse-recovery problem of the diodes is alleviated by the leakage inductor. Thus, the efficiency can be improved. The operating principle and steady-state analyses of the converter are discussed in detail. Finally, a prototype circuit at a 50 kHz switching frequency with a 20-V input voltage, a 200-V output voltage, and a 200-W output power is built in the laboratory to verify the performance of the proposed converter.

Key words: Coupled inductor, High step-up voltage gain, Low voltage stress, Switched capacitor

#### I. Introduction

In recent years, renewable energy sources have become more and more widely used to replace fossil fuel in many industrial applications. However, such applications include fuel-cell energy-conversion systems and solar-cell energy-conversion systems, where the voltage obtained from the fuel or PV cells is low, so that there is not enough DC voltage to feed the AC utility. In addition, the automobile high-intensity-discharge headlamp operating voltage is much higher than that provided by a battery [1]-[5]. Therefore, it is necessary to step up from a low voltage to a high voltage.

In the conventional converter, a boost converter is used for voltage step-up applications. This is due to the fact that a boost converter can provide a high step-up voltage gain with an extreme duty cycle in theory. However, in practice, the boost converter voltage gain is usually restricted by the effects of the power switch, rectifier diode, and equivalent series resistance (ESR) of the inductor and capacitor. Moreover, extremely high duty ratio operation will result in serious reverse-recovery problems, low efficiency, high voltage stress of the switch, and electromagnetic interference (EMI) problems [6]-[8]. Thus, a high step-up converter is used for these applications.

Many topologies have been proposed to improve conversion efficiency and to achieve a high step-up voltage gain [7]-[21]. A high step-up voltage gain can be obtained by a switched capacitor technique [7], [8]. Unfortunately, the main switch has a high surge current, the conduction loss is increased, and the cost is increased. Switched inductor technology also extends the voltage gain [7], [9]. Unfortunately, the voltage stresses of the switches of converters are still higher. Therefore, high-voltage rated switches induce serious conduction losses. The voltage-lift technique [10]-[12] developed by Luo can also achieve a high step-up voltage gain. The voltage-lift technique is similar to the Cuk converter, and is based on an energy transfer from

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one inductor via an intermediate capacitor to the output. However, the main switch suffers from a high transient current, and the conduction loss is increased.

Converters can achieve a high step-up voltage gain by adjusting the turns ratio of the coupled inductor [13]. Unfortunately, the leakage inductance of the coupled-inductor causes a high voltage spike on the active switches when the switches are turned off [13]-[16]. As a result, converters using a coupled-inductor with an active-clamp circuit and a passive-clamp circuit have been proposed [17]-[21]. Moreover, the leakage energy can be recycled with the help of the clamp circuit.

In this paper, two novel voltage-lift cells are proposed. These cells integrate three-winding coupled inductors technology and switched-capacitor technology, and further extend the voltage gain. At the same time, this paper proposes a novel high step-up voltage gain and a clamp-mode converter which uses a SCIC to achieve a high step-up voltage gain and to reduce the voltage stress of the main switch. The SCIC shares its capacitor with a clamping circuit. Additionally, two capacitors can be charged in parallel and discharged in series via the coupled inductor. However, the leakage inductor of the coupled inductor may cause a high power loss and a voltage spike. Thus, a passive clamping circuit can recycle the leakage-inductor energy of the coupled inductor and clamp the voltage across the main switch. Thus, the reverse-recovery problems in the diodes are alleviated, and the performance of the proposed converter is improved.

### II. VOLTAGE-LIFT-TYPE SWITCHED-COUPLED-INDUCTOR-CAPACITOR CELLS

The basic step-up switched-capacitor cells (SC) are constituted with two capacitors and two diodes as shown in Fig. 2. The following are for the discussion about Fig. 1(a), and Fig. 1(b) is similar to Fig. 1(a). When the switching is turned on,  $D_1$  and  $D_2$  turn off, while  $C_1$  and  $C_2$  are discharged in series. When the switching is turned off,  $D_1$  and  $D_2$  turn on, while  $C_1$  and  $C_2$  are charged in parallel.

Converters with switched capacitor (SC) cells can improve the voltage gain when compared to the classic boost converter. Unfortunately, [22] and [23] have a higher components count, their cost is increased, and their output voltages are not continuously adjustable. In recent years, converters with coupled inductors have become more and more widely used in order to solve these problems. These converters can achieve a higher step-up voltage gain by adjusting the turns ratio of the coupled inductor, which can reduce the number of the active switches when compared with converters with SC cells. Unfortunately, the leakage inductance of a coupled-inductor results in a high voltage spike on active switches when the switches are turned off.

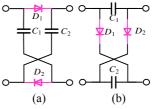


Fig. 1. Step-up basic switching structures. (a) Up I. (b) Up II.

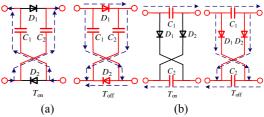


Fig. 2. Switching topologies of the step-up structures. (a) Up I. (b) Up II.

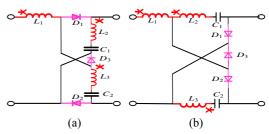


Fig. 3. The proposed basic step-up switching structures. (a) Up I. (b) Up II.

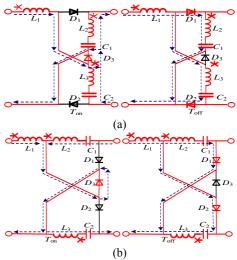


Fig. 4. The current-flow path with the proposed step-up structures. (a) Up I. (b) Up II.

[24] and [25] with coupled inductors can achieve a high step-up voltage gain and the leakage-inductor energy can be recycled to the load. However, in [24] the voltage gain is only equal to 8 and the voltage stress of the output diode is beyond  $0.5V_o$  when n=2 and D=0.5. In [25] the voltage gain is only equal to 2 and the voltage stress of the output diode is equal to  $0.5V_o$  when n=2 and D=0.5. In order to further

improve the voltage gain, reduce the number of active switches, and reduce the voltage stress of the output diode, the SCICs are proposed in this paper.

The voltage-lift technique is then applied to basic SC cells, which can generate new voltage-lift-type SCIC structures with a higher voltage transfer gain. The basic step-up SCIC structures formed with windings-coupled inductors, diodes and capacitors are shown in Fig. 3. For the convenience of analysis, the switching operations of the proposed SCIC structures are shown in Fig. 4. As shown in Fig. 3(a), the secondary-sides of the windings-coupled inductor are inserted into two branches with the capacitor. The current-flow path is shown in Fig. 4(a). When the switching topologies  $T_{on}$ ,  $D_3$ turns on,  $D_1$  and  $D_2$  turn off, and  $L_2$ ,  $L_3$ ,  $C_1$  and  $C_2$ are discharged in series. When the switching topologies are turned off,  $D_1$  and  $D_2$  turn on,  $D_3$  turns off, and the voltage-lift branch ( $L_2$  and  $C_1$ ) is charged with the voltage-lift branch ( $L_3$  and  $C_2$ ) in parallel. Fig. 3(b) is similar to Fig. 3(a) in terms of operating principle, and the current-flow path is shown in Fig. 4(b).

## III. PROPOSED CONVERTER AND OPERATIONAL PRINCIPLE

Basic step-up switched-capacitor cells (SC) are constituted with two capacitors and two diodes as shown in Fig. 2. The converter with the SCIC led in Fig. 3(b) has not been discussed due to its similarity to Fig. 5(a). The proposed converter with the SCIC Up I is illustrated in Fig. 5(a), which contains an active switch S, three-winding-coupled inductors, three rectifier diodes  $D_1$ ,  $D_2$  and  $D_0$ , and three capacitors  $C_1$ ,  $C_2$  and  $C_0$ . It is clear that the leakage inductance of the coupled-inductor will cause a high voltage spike on switch S when the switch is turned off.

In order to suppress the voltage spike by the leakage inductor, clamping circuits composed of diodes  $D_3$  and  $D_4$  and capacitors  $C_1$  and  $C_2$  are shown in Fig. 5(b).Diodes  $D_3$  and  $D_4$  are used to clamp switch S to and prevent the problem of the same time conduction between  $D_1$  and  $D_0$ .

The equivalent circuit is shown in Fig. 7. The coupled inductor is modeled as a magnetizing inductor  $L_{\rm m}$ , a primary leakage inductor  $L_{\rm k}$ , and ideal transformers with turns ratios of  $N=N_2:N_1=N_3:N_1\left(N>1\right)$ , where  $N_1$ ,  $N_2$  and  $N_3$  are the primary-side turns and the secondary-side turns, respectively.  $V_{L2}$  is equal to  $V_{L3}$ , and capacitor  $C_{\rm s}$  is the parasitic capacitor of switch S. To simplify the circuit analysis of the proposed converter, the following conditions are assumed. First, all of the components are ideal. The

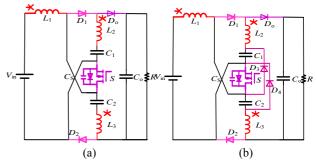


Fig. 5. Circuit configure of the proposed converter.

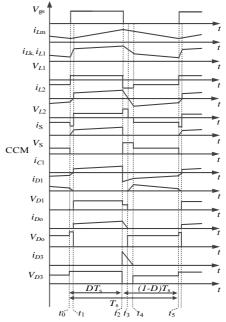


Fig. 6. Some typical waveforms of proposed converter at CCM operation.

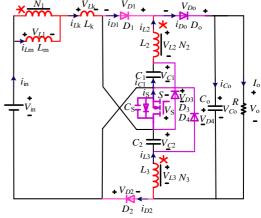
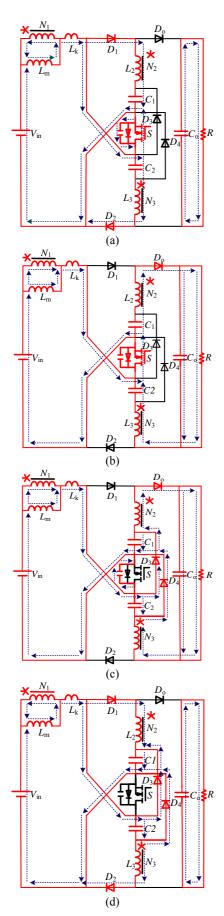


Fig. 7. Equivalent circuit model of the proposed converter.

ON-state resistance RDS of the active switches, the forward voltage drop of the diodes and the ESR of the coupled inductor and all of the capacitors are ignored. Second, capacitors  $C_{\rm o}$ ,  $C_{\rm l}$  and  $C_{\rm l}$  are sufficiently large, the voltages  $V_{C1}$  and  $V_{C2}$  are equal to  $V_{CC}$ , and the voltages across the



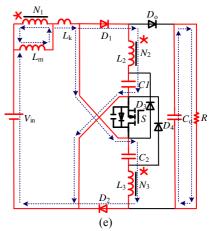


Fig. 8. Current-flow path of the operating modes during one switching period at CCM operation. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V.

capacitors are considered to be constant during one switching period. Fig. 6 shows typical waveforms during one switching period in continuous-conduction-mode (CCM) operation. The operating principle is described as follows:

- 1) Mode I  $[t_0, t_1]$ : At  $t = t_0$ , The active switch S is turned on.  $D_o$ ,  $D_3$  and  $D_4$  are turned off. The current-flow path is shown in Fig. 8(a). During this time interval, the magnetizing inductor  $L_{\rm m}$  and the leakage inductor  $L_{\rm k}$  are charged by the input source and the currents  $i_{\rm Lm}$  and  $i_{\rm Lk}$  are increased. At the same time, the energy of the input source is released to capacitors  $C_1$  and  $C_2$  via the secondary winding  $L_2$  and  $L_3$  of the coupled inductor, respectively, and the currents  $i_{\rm L2}$  and  $i_{\rm L3}$  are increased. The output capacitor  $C_{\rm o}$  provides energy to the load R. The voltages across  $V_{\rm L2}$  and  $V_{\rm L3}$  are clamped at  $V_{\rm CC}$ . The voltage  $V_{\rm Do}$  is equal to  $V_{\rm o}$ . Moreover, the energy stored in  $C_{\rm S}$  is rapidly and completely discharged. This operating mode ends when the currents  $i_{\rm L2}$  and  $i_{\rm L3}$  are equal to zero at  $t = t_1$ .
- 2) Mode II  $[t_1,t_2]$ : During this time interval, the active switch S is still turned on.  $D_1$   $D_4$  are turned off. The current-flow path is shown in Fig. 8(b). The dc-source  $V_{\rm in}$  energy is transferred to  $L_{\rm m}$  and  $L_{\rm k}$  through switch S. Therefore, the currents  $i_{L\rm m}$  and  $i_{L\rm k}$  are increased. Meanwhile,  $C_1$ ,  $C_2$ ,  $L_2$  and  $L_3$  are series connected to transfer their energies to  $C_{\rm o}$  and the load R via  $D_{\rm o}$ . The currents  $i_{L2}$ ,  $i_{L3}$  and  $i_{C1}$  are increased. This operating mode ends when switch S starts to turn off at  $t=t_2$ .

3) Mode III  $[t_2,t_3]$ : At  $t=t_2$ , switch S is turned off. The current-flow path is shown in Fig. 8(c). During this mode, the voltage across switch S increases rapidly. The voltages across  $L_2$  and  $L_3$  are clamped at  $(V_o-V_{cc})/2$ , and the voltage across the active switch S is clamped at  $V_{cc}$ , because the clamping diodes  $D_3$  and  $D_4$  are turned on. The voltages across  $D_1$  and  $D_2$  are clamped at  $V_{L2}$  and  $V_{L3}$ , respectively. As a result, they are reverse-biased. The energies of inductors  $L_2$  and  $L_3$  with capacitors  $C_1$  and  $C_2$  are released to the output capacitor  $C_0$  and the load R. The voltage  $V_{L1}$  is equal to  $V_{in}$  - $V_{cc}$ . This operating mode ends when the current  $I_{L2}$  becomes zero at  $t=t_3$ .

4) Mode IV  $[t_3, t_4]$ : At  $t=t_3$ , the output diode is turned off, and the rectifier diodes  $D_1$  and  $D_2$  are turned on. The current-flow path is shown in Fig. 8(d). The voltage across  $L_1$  is still equal to  $V_{\rm in}$  - $V_{cc}$ , and the voltages across  $L_2$  and  $L_3$  are clamped at - $V_{cc}$ . However, the voltage across switch S is clamped at  $V_{cc}$ . The primary side of the coupled inductor is in series with the input source and the secondary side  $L_2$  of the coupled inductor to release their energies to the capacitor  $C_1$  via the diode  $D_1$ . At the same time, the primary side of the coupled inductor is in series with the input source and the secondary side  $L_3$  to release their energies to the capacitor  $C_2$  via the diode  $D_2$ , and the currents  $i_{Lk}$ ,  $i_{Lm}$  and  $i_{L2}$  are reduced. Thus, the clamping diodes  $D_3$  and  $D_4$  are cut off at  $t=t_4$ , and this operating mode ends.

5) Mode V [ $t_4$ ,  $t_5$ ]: During this time interval, switch S is still turned off. The clamping diodes  $D_3$  and  $D_4$  are turned off, and the current-flow path is shown in Fig. 8(e). The primary side of the coupled inductor, the secondary side winding  $L_2$  and the input source are in series to transfer their energies to the capacitors  $C_1$  via the rectifier diode  $D_1$ . Meanwhile, the capacitor  $C_2$  is charged by the input source, the primary side of the coupled inductor and the secondary side winding  $L_3$  via the rectifier diode  $D_2$ . This mode ends at  $t = t_5$  when switch S is turned on at the beginning of the next switching period.

#### IV. STEADY-STATE ANALYSIS

#### A. CCM Operation

In CCM operation, the time durations of modes I, III and IV are very short when compared to one switching period.

Thus, only modes II and V are considered. In order to analyze the voltage gain of the proposed converter, the voltages across the capacitors  $C_1$  and  $C_2$  are assumed to be:

$$V_{C1} = V_{C2} = V_{CC} \tag{1}$$

The coupled-coefficient k and the turns ratio n of the coupled-inductor are assumed to be:

$$n = N_2 / N_1 = N_3 / N_1 \tag{2}$$

$$k = L_{\rm m} / (L_{\rm m} + L_{\rm k}) \tag{3}$$

During mode II, the following equations can be written based on Fig. 8(b):

$$V_{ii}^{II} = kV_{in} \tag{4}$$

$$2nkV_{II}^{II} = V_o - 2V_{CC} \tag{5}$$

Substituting (4) into (5), the voltages of the capacitors  $C_1$  and  $C_2$  are obtained as:

$$V_{C1} = V_{C2} = V_{CC} = (V_o - 2nkV_{in})/2$$
 (6)

During mode V, the following equations can be formulated based on Fig. 8(e):

$$V_{\rm in} + V_{L1}^{\rm V} + nV_{L1}^{\rm V} = V_{CC} \tag{7}$$

Where the voltage  $V_{L1}^{V}$  is found to be:

$$V_{L1}^{V} = (V_{in} - V_{CC}) / (n+1)$$
 (8)

Using the volt–second balance principle on  $L_1$  yields:

$$\int_{0}^{DT_{s}} V_{L1}^{II} dt + \int_{DT}^{T_{s}} V_{L1}^{V} dt = 0$$
 (9)

Substituting (4) and (8) into (9), the voltages across the capacitors  $C_1$  and  $C_2$  and the voltage gain are obtained as:

$$V_{C1} = V_{C2} = V_{CC} = (1 + Dk^2 + nDk^2 - D)V_{in} / (1 - D)$$
 (10)

$$M_{CCM} = 2(nDk^2 + Dk^2 + nk + 1 - nDk - D)/(1 - D)$$
 (11)

It can be seen that the voltage gain is influenced by the turns ratio and the leakage coefficient. The relationships between the voltage gain, the duty ratio and the coupling coefficients of the coupled inductor are shown in Fig. 9. It can be seen that the voltage gain is less sensitive to the coupling coefficient. Thus, if the impact of the leakage inductances of the coupled inductor is neglected, the coupled coefficient k is equal to 1. The ideal voltage gain can be simplified as:

$$M_{CCM} = V_o / V_{in} = 2(n+1)/(1-D)$$
 (12)

The voltage gain of a traditional boost converter is 1/(1-D). In [7], the basic switch-capacitor boost voltage gain is 1+D/(1-D). The voltage gain in [20] is (1+nD)/(1-D) and the voltage gain in [21] is (1+2n-nD)/(1-D). They have a lower voltage gain when compared with the proposed converter.

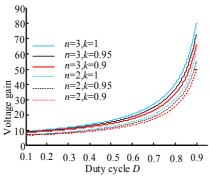


Fig. 9. Voltage gain versus duty ratio at CCM operation under n = 2 and various k.

#### B. Boundary Operating Condition

Since the time durations  $[t_0, t_1]$  and  $[t_2, t_4]$  are very short when compared to one switching period, these two time durations are not considered. When the proposed converter is operated in the boundary conduction mode, the peak value of the secondary side current of the coupled inductor is given as:

$$I_{L2n} = nkDT_{\rm s}V_{\rm in} / L_2 \tag{13}$$

Thus, the peak current of the output diode is given as:

$$I_{\text{Dop}} = nkDT_{\text{s}}V_{\text{in}} / L_2 \tag{14}$$

At the steady state, the average value of  $i_{\mathrm{Do}}$  is equal to  $I_{\mathrm{o}}$  . Thus:

$$I_{\text{Don}} = nkDT_{s}V_{\text{in}} / L_{2} = I_{a} = V_{a} / R$$
 (15)

Then, the time constant  $\tau_{L2}$  of the secondary side for the coupled inductor is derived as:

$$\tau_{L2} \equiv L_2 / RT_s = L_2 f_s / R$$
 (16)

Where  $f_s$  is the switching frequency.

Substituting (11) and (16) into (15), the boundary time constant  $\tau_{L2B}$  for the secondary side of the coupled inductor can be given as:

$$\tau_{L2B} = nD(1-D)/2(n+1) \tag{17}$$

If  $\tau_{L2}$  is larger than  $\tau_{L2B}$ , the proposed converter is operated in the CCM. The curved line of  $\tau_{L2B}$  is shown in Fig. 10.

#### C. Voltage and Current Stresses on Power Devices

According to the operating principle, the voltage and current stresses on power devices are discussed as follows. If the impact of the leakage inductor of the coupled inductor is ignored, the voltage stresses on switch S,  $D_1 - D_3$  and  $D_o$  are given as:

$$V_{\rm DS} = V_{\rm CC} = (1+nD)V_{\rm in}/(1-D) = (nD+1)V_{\rm o}/2(n+1)$$
 (18)

$$V_{D1} = V_{D2} = (1+n)V_{in}/(1-D) = V_{o}/2$$
 (19)

$$V_{D3} = V_{D4} = V_{CC} = \frac{1 + nD}{1 - D} V_{in} = \frac{nD + 1}{2(n+1)} V_{o}$$
 (20)

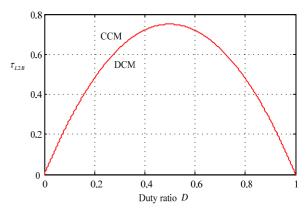


Fig. 10. Boundary condition of the proposed converter with n=2 and k=1

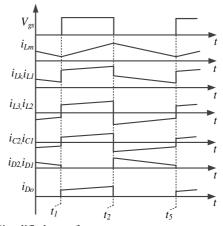


Fig. 11. Simplified waveforms.

$$V_{Do} = V_{o} \tag{21}$$

From (14) and (15)the current stresses that flow through  $D_1$ ,  $D_2$  and  $D_{\sigma}$  are found to be:

$$I_{D1} = I_{D2} = I_{D0} = I_0 + I_{D00} / 2 = V_0 / R + nkDT_sV_{in} / L_2$$
 (22)

In order to simplify the current calculation, the extremely short time intervals  $\begin{bmatrix} t_0 - t_1 \end{bmatrix}$ ,  $\begin{bmatrix} t_2 - t_3 \end{bmatrix}$  and  $\begin{bmatrix} t_3 - t_4 \end{bmatrix}$  are ignored. The magnetizing current is considered to be a constant since the magnetizing inductor  $L_{\rm M}$  is large enough. The simplified waveforms of the proposed converter are shown in Fig. 11.

According to the current balance law, the on-state average current of capacitor  $C_1$  can be expressed as:

$$I_{C_1(\text{on})} = I_0 / D \tag{23}$$

According to the current balance law, the off-state average currents of capacitor  $C_1$  and diodes  $D_1$  and  $D_2$  can be represented as:

$$I_{D_1(\text{off})} = I_{D_2(\text{off})} = I_{C_1(\text{off})} = I_o / (1 - D)$$
 (24)

Thus, based on Fig.11 and equation (24), the magnetic average current of the coupled inductor can be represented as:

$$I_{IM} = 2(N+1)I_0/(1-D)$$
 (25)

Topology	Converter	Converter	Converter	Converter	Converter	Proposed
	in [26]	in[27]	in[28]	in[29]	in[30]	converter
Numbers of Active switches	1	2	1	2	2	1
Numbers of diodes	5	3	3	6	2	5
Voltage gain	$\frac{2+n}{2-2D}$	$\frac{1+nD}{1-D}$	$\frac{2+nD}{1-D}$	$\frac{1+2nD+D}{1-D}$	$\frac{1+nD}{1-D}$	$\frac{2n+2}{1-D}$
Voltage stress of active switches	$\frac{2V_o}{2+n}$	$\frac{V_o}{1+nD}$	$\frac{V_o}{2+nD}$	$\frac{V_{\circ} + V_{\circ} ND}{1 + D + D2N}$	$\frac{V_o}{1+n}$	$\frac{(nD+1)V_{o}}{2(n+1)}$
Voltage stress of output diodes	$\frac{2V_o}{2+n}$	$\frac{V_o}{1+nD}$	$\frac{(n+1)V_o}{2+nD}$	$\frac{V_{\rm o} + V_{\rm o} ND}{1 + D + D2N}$	$V_{ m o}$	$\frac{V_o}{1+nD}$

TABLE I
PERFORMANCE COMPARISONS AMONG DIFFERENT CONVERTERS

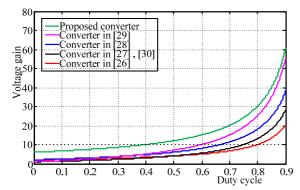


Fig. 12. Voltage gain comparison.

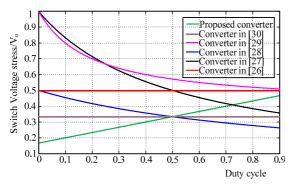


Fig. 13. Active switch voltage stress comparison.

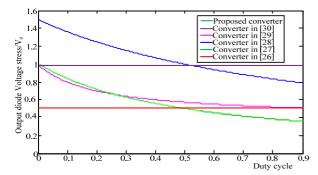


Fig. 14. Output diode voltage stress comparison.

#### D. Performance Comparison

To further demonstrate the performance of the proposed converter, table I shows a comparison of the performances between the voltage-clamped DC–DC converter in [26], the coupling inductor boost converter in [27], the coupled inductor voltage-lift converter in [28], the coupled inductor active-network converter in [29], the coupled inductor voltage doubler cell converter in [30],and the proposed converter.

The voltage gain of the proposed converter is compared with that of the step-up converters in Fig. 12 when N = 2 and K = 1. It is observed that the voltage gain of the proposed converter is higher than that of the others.

The relationship between the voltage stress of the active switch and variable duty cycle is described in Fig. 13 when N=2. The active switch stress of the proposed converter is lower to under D<0.5.

The relationship between the voltage stress of the output diode with a variable duty cycle is shown in Fig. 14 when the turns ratio is equal to 2. When the duty cycle is more than about 0.5, the output diode voltage stress of the proposed converter is lower.

Compared to the voltage-clamped DC–DC converter in [26], with the same component count, the voltage gain of the proposed converter has an advantage, and the output diode voltage stress of the proposed converter is lower when the duty cycle is beyond 0.5. When the duty cycle is less than 0.5, the output diode voltage stress of the converter in [26] is lower. Fortunately, the proposed converter has an obviously advantage in terms of the active switch voltage stress. Therefore, low  $R_{\rm DS}$  MOSFETs can be used. This is beneficial for improving the converter efficiency.

Comparing the coupling inductor boost converter in [27], the diode count of the presented converter is greater.

TABLE II
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

System parameters	Specifications		
Input voltage $V_{\mathrm{in}}$	20V		
Output voltage $V_{\rm o}$	200V		
Rated power $P_{o}$	200W		
Switching frequency $f_{\rm s}$	50kHz		

TABLE III
SYSTEM SPECIFICATIONS OF THE PROPOSED CONVERTER

Components	Specifications
MOSFET Switch S	SiHG73N60E
Diodes $D_{\rm o} - D_4$	IDH12S60C
Output capacitor $C_o$	$470\mu F$ , $0.1\mu F$
Capacitors $C_1, C_2$	$10\mu F$ ,0.1 $\mu F$
	Core-NPS306060,
Coupling inductors	$N = N_2 / N_1 = N_3 / N_1$ ,
	$L_{\rm p} = 137.6 \mu \text{H}, L_{\rm S} = 548.5 \mu \text{H}$

However, the active switch count is lower and the voltage gain of the presented converter has an advantage. The output diode voltage stress is equal to the presented converter. When the duty cycle is beyond about 0.72 the active switch voltage stress of the presented converter is more than the converter in [27]. When the duty cycle is lower than 0.72 the active switch voltage stress has an advantage especially when the duty cycle is lower than 0.5. In this paper, the duty cycle is about 0.4. Therefore, low  $R_{\rm DS}$  MOSFETs can be used.

Compared to the coupled inductor voltage-lift converter in [28], the proposed converter has more diodes. Fortunately, the voltage gain and the output diode voltage stress of the presented converter have advantages. When the duty cycle is more than about 0.5, the active switch voltage stress has no advantage. However, the active switch voltage stress is lower when the duty cycle is less than 0.5. In this paper, the duty

when the duty cycle is less than 0.5. In this paper, the duty cycle is about 0.4. Therefore, low  $R_{\rm DS}$  MOSFETs can be used

Compared to the coupled inductor active-network converter in [29], the voltage gain and active switch voltage stress of the proposed converter have advantages. In addition, the output diode voltage stress of the proposed converter is lower when the duty cycle is beyond about 0.27, and the proposed converter has fewer diodes and switches.

Compared to the coupled inductor voltage doubler cell converter in [30], the voltage gain and output diode voltage stress of the proposed converter have advantages. The active switch voltage stress is low when D < 0.5, and the active switch count of the proposed converter is lower.

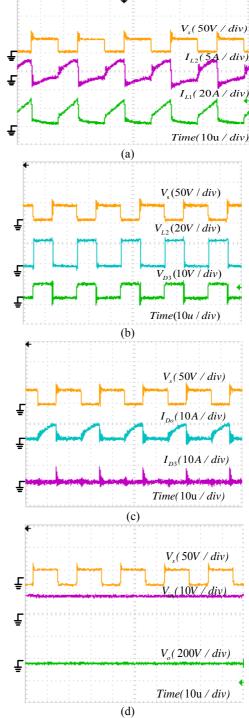


Fig. 15. Experimental waveforms of proposed converter under full-load 200W.

#### V. EXPERIMENTAL RESULTS

To verify the performance of the proposed converter, a prototype circuit is implemented in the laboratory. Table II shows the system specifications of the proposed converter, and Table III shows the component specifications used in the proposed converter. The specifications are as follows:

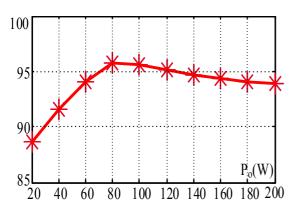


Fig. 16. Experimental conversion efficiency

#### A. The magnetizing inductance design

The magnetizing inductor can be designed by setting an acceptable current ripple on the magnetizing inductor, which is given by:

$$L_{\rm M} \ge V_{\rm in} D / K_{L_{\rm M}} I_{L_{\rm M}} f_s \tag{26}$$

By combining (25) and (26), and collecting the terms, the magnetizing inductance can be computed as:

$$L_{\rm M} \ge V_{\rm in} D(1-D)/2K_{L_{\rm M}}I_{\rm o}(N+1)f_{\rm s}$$
 (27)

Where  $K_{L_{tt}}$  is the current ripple coefficient.

Based the relative equation in section V, the numerical design of the magnetizing inductance of the coupled inductor, the output capacitor and the clamped capacitors are shown as:

$$L_{\rm M} \ge V_{\rm in} D(1-D)/2K_{L_{\rm M}} I_{\rm o} (N+1) f_{\rm s} \approx 80.6 \mu \text{H}$$
 (28)

#### B. Turns ratio design

Since the turns ratio of the coupled inductor determines the voltage stress of the switch and the operational duty-cycle of the converter, it is the key parameter in the circuit design. The turns ratio can be obtained when the duty-cycle is constant, which is given by:

$$N = (V_0 (1-D) - 2V_{in}) / 2V_{in}$$
 (29)

Some of the key figures are given as Fig. 15 under a full-load. Fig. 15 shows the measured waveforms for a full-load. The proposed converter is operated in the CCM. The waveforms demonstrate that the steady-state analysis is correct. In the measured waveforms, the duty cycle is 41% and the voltage stress on switch S is equal to 35V during the switch off and it is shortly clamped at 54V. Therefore, a low-voltage-stress switch is adopted to achieve high efficiency for the proposed converter. Fig. 15(a) shows the switch voltage  $V_{\rm S}$ , the coupled inductor currents  $i_{L1}$ , and  $i_{L2}$ . The waveforms agree with the theoretical analysis. Fig. 15(b) shows the switch voltage  $V_{\rm S}$ , the coupled inductor voltage  $V_{L1}$ , and the clamped diode reverse-biased voltage  $V_{D3}$ . Fig. 15(c) shows the switch voltage  $V_{\rm S}$ , the clamped diode

current  $i_{D3}$ , and the output diode current  $i_{D0}$ . Fig. 15(d) shows that the output voltage  $V_S$  is equal to 197V.

Fig. 16 shows the conversion efficiency of the proposed converter, where the maximum efficiency is around 95.8% at  $P_o = 80 \text{ W}$ , and the full-load efficiency is approximately 93.7% under 200W with a 20V input voltage.

#### VI. CONCLUSION

In this paper, a novel switched-coupled-inductor-capacitor topology with a high voltage ratio is proposed and the steady state analysis is given. A passive lossless clamping circuit is introduced to suppress voltage spikes across the switch. Compared to traditional high step-up DC-DC converters, it has following main advantages:

- (1) A high voltage gain can be achieved with a reduced magnetic size.
- (2) A single active switch is required, implying a very simple control circuit. The inrush current problem of the switched-capacitor circuit is well restrained by the leakage inductance of the coupled inductor.
- (3) A low voltage stress power switch can be selected, which can help reduce both the on-state resistance of the switch and the loss.

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