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Hardware-Based Implementation of a PIDR Controller for Single-Phase Power Factor Correction

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Abstract In a single-phase power factor correction (PFC), the standard cascaded control algorithm using a proportional-integral-derivative (PID) controller has two main drawbacks: an inability to track sinusoidal current reference and low harmonic compensation capability. These drawbacks cause poor power factor and high harmonics in grid current. To improve these drawbacks, this paper uses a proportional-integral-derivative-resonant (PIDR) controller which combines a type-III PID with proportional-resonant (PR) controllers in the PFC. Based on a small signal model of the PFC, the type-III PID controller was implemented taking into account the bandwidth and phase margin of the PFC system. To adopt the PR controllers, the spectrum of inductor current of the PFC was analyzed in frequency domain. The hybrid PIDR controller were simulated using PSCAD/EMTDC and implemented on a 3 kW PFC prototype hardware. The performance results of the hybrid PIDR controller were compared with those of an individual type-III PID controller. Both controllers were implemented successfully in the single-phase PFC. The total harmonic distortion of the proposed controller were much better than those of the individual type-III PID controller.

Key Words : Active PFC, PIDR controller, PFC

1. Introduction

In the grid-tie power converter system, in general, has low power factor and total harmonic distortion(THD) because of non-linear switching devices (i.e., IGBT, MOSFET, Diode …). Due to the requirements of power quality of the power system, all electric devices today have to comply with specific power factor and THD (e.g., IEC 61000-3-2, IEEE 519, IEC 1000-3-2) standards [1-3]. A common approach to satisfy power factor and THD standards is to incorporate an additional power factor correction (PFC) in the preceding stage of a switching converter [4].

The standard cascaded linear algorithm consisting of a slow outer voltage loop and a fast inner current loop using a proportional-integral-derivative (PID) controller or its modified versions based on two criterions, phase margin and bandwidth of the system, is unable to track a sinusoidal signal current, even for tracking the fundamental grid frequency in a single-phase grid-tie inverter [5-7]. To increase dynamic response of the

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outer voltage loop in use of PID controller, the notch-filter control strategy was proposed to extend the bandwidth of the outer voltage loop. The notch-filter control strategy has good performance in simulation, but in practical implementation, several problems emerged [8,9]. The adaptive non-linear control strategy using energy balance over one-half of the grid frequency to obtain the desired magnitude of grid current presented in [10] has good performance compared with the linear approach. A disadvantage of the nonlinear method is the dependency of the nonlinear carrier signal on the switching frequency [11]. Previous studies proposed a proportional-resonant (PR) controller to track a sinusoidal current of the single-phase grid-tie inverter [12,13]. In an ideal PR controller, the proportional gain equals zero, the magnitude of transfer function of the PR controller is infinite at resonant frequency and null at the other frequencies that any kind of PID controller does not have.

This paper proposed a hybrid proportional-integral-derivative-resonant (PIDR) controller to improve the drawbacks of the notch-filter and simple PID controller in the PFC reflecting the advantages of the PR controller. The PIDR controller combines a type-III PID controller with PR controllers for a single-phase PFC. Based on the reference signals of inductor current in frequency domain and small signal model of the PFC, the type-III PID controller was selected to obtain phase margin and bandwidth of the PFC system. The PR controllers were adopted to track the high frequency sinusoidal signals of inductor current reference. Then, the performances of the PIDR controller were confirmed through the simulation using PSCAD/EMTDC, and implemented on a 3 kW PFC prototype hardware. The effectiveness of the hybrid PIDR controller was demonstrated through the comparison between the individual type-III PID controller and the PIDR controller.

2. Power Factor Correction

2.1 PFC Model

Among several topologies of the PFC, the boost topology is most common [7-10]. Figure 1 shows a circuit diagram and control algorithm of a single-phase PFC using boost topology. It consists of a full-bridge diode rectifier and a conventional boost converter.

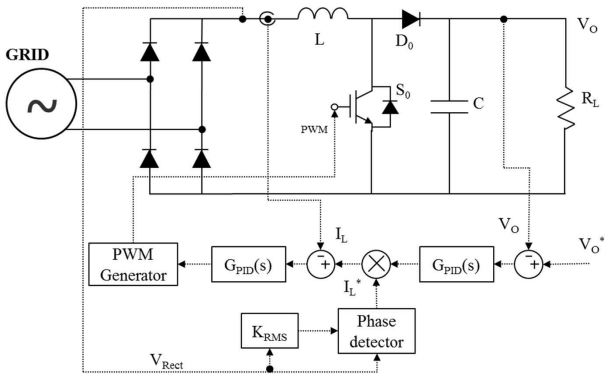


Fig. 1 Circuit diagram and control algorithm of a single-phase PFC

The control algorithm of the PFC consists of a voltage loop and a current loop. The dynamic response of the voltage loop in the PFC is much slower than that of the current loop, and it has a narrow bandwidth (normally 5 - 30 Hz) [5,8]. The controller of the current loop, which tracks high frequency reference signals, is the most important component of the PFC. This paper focuses mostly on the current controller.

Because the dynamic output of the PFC is much slower than its switching frequency, the small signal model of the PFC was presented

as:

$$G_{ui}(s)=\frac{\widetilde{v_O}}{\widetilde{i_L}}=\frac{(1-D)\cdot(R_L-Z_L)\cdot Z_{RC}}{R_L+Z_L} \quad (1)$$

$$G_{id}(s)=\frac{\widetilde{i_L}}{\widetilde{d}}=\frac{V_O}{R_L\cdot Z_{RC}}\cdot\frac{R_L\cdot Z_{RC}+1}{Z_L+(1-D)^2\cdot Z_{RC}} \quad (2)$$

where $G_{ui}(s)$ is the inductor current-to-output voltage transfer function, and $G_{id}(s)$ is the duty cycle-to-inductor current transfer function. I_L, D, and V_O are the average values of inductor current, duty cycle, and output voltage, respectively. Z_{RC} is the impedance of the resistor load (R_L) and the output capacitor (C) in parallel, and Z_L is the impedance of the inductor (L). $\hat{d}$, $\widehat{i_L}$, $\widehat{v_O}$, and $\widehat{v_{in}}$ are the amount of change in one switching cycle of the duty cycle, inductor current, output voltage, and input voltage, respectively. Detailed study of modeling of the PFC can be found in [1,4-6]. The parameters of the PFC prototype are 3 kW of power, a switching frequency of 20 kHz, 2.5 mH of inductor, 3,290 uF of boost capacitor, and a grid voltage of 220 V - 60 Hz.

2.2 An Individual Type-III PID Controller

Among many kind of PID controller, an type-III PID controller was selected because the type-III controller shows good performance in boosting phase margin, and extending bandwidth of the system. As the controllers were implemented on a digital signal processor (DSP), the computational delay and sampling effects of analog-digital-converter (ADC) were considered. The system has a sampling time of TS. Assuming that the average calculation time of the controller is T_S, the delay transfer function is e^{-sT_S}. Using Taylor expansion, the delay effect was represented in a first-order transfer function as follows:

$$e^{-sTs}=\frac{1}{1+s\cdot T_s} \quad (3)$$

and the sampling effect of the ADC is given by:

$$G_{ZOH}(s)=\frac{1}{1+s\cdot T_s/2} \quad (4)$$

Thus, the open loop transfer function of the current loop consisting of the model in (2), delay effect in (3), and zero-order hold effects in (4) are given by:

$$G_{plant}(s)=G_{id}(s)\cdot\frac{1}{1+s\cdot T_s}\cdot\frac{1}{1+s\cdot T_s/s} \quad (5)$$

The transfer function of the type-III PID controller has the following form:

$$G_{PID}(s)=k\frac{(s+\omega_{z1})(s+\omega_{z2})}{s\cdot(s+\omega_{p1})(s+\omega_{p2})} \quad (6)$$

The coefficients of the type-III PID controller for the current loop were calculated based on the duty cycle-to-inductor current transfer function of the PFC in (6) and

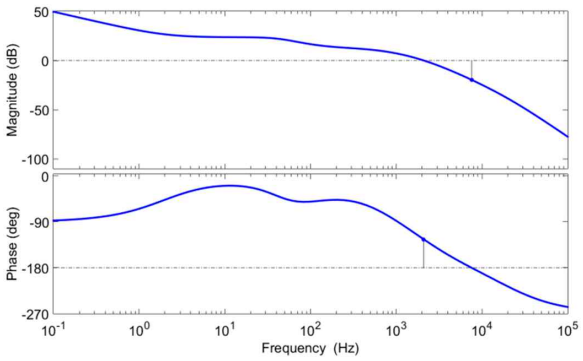


Fig. 2 Bode diagram of transfer function of the open loop including the type-III PID controller

considered two criteria (i.e., the phase margin and bandwidth). A bandwidth of 2 kHz (10% of switching frequency) and 60-degree phase margin were selected. Hence, k = 8,225.1, ω_{z1} = ω_{z2} = 426.1 rad/s, and ω_{p1} = ω_{p2} = 2.316e4 rad/s. The Bode diagram of the open loop including the current controller is depicted in Fig. 2.

3. Hybrid PIDR Controller

The hybrid PIDR controller is proposed to overcome the drawbacks of the individual type-III PID controller in current loop of the PFC by adding several PR controllers. The resonant frequencies of PR controllers are selected by the spectrum of inductor current of the PFC. The current of an inductor, (L), is represented as:

$$I_L = I_o|\sin(\omega t)| \qquad (7)$$

where I_0, ω are the maximum amplitude of inductor current and the grid angular frequency, respectively.

From (7), the inductor current is decomposed by Fourier expansion in frequency domain to several sinusoidal signals (i.e., 120 Hz, 240 Hz ...) and a DC signal presented in Fig. 3.

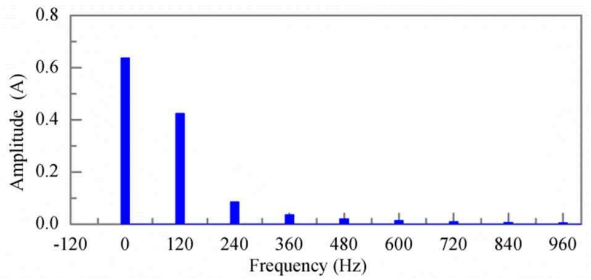


Fig. 3 Spectrum of $I_L = I_o|\sin(\omega t)|$

As shown in Fig. 3, the amplitude of the inductor current is composed by significant amplitude signals at 0 Hz (DC), 120 Hz, 240 Hz and 360 Hz and minor amplitude signals at 480 Hz, 600 Hz, and higher frequency. These signals are the current reference signals for the current controller. To track these signals, the transfer function of open current loop is required to have extreme high magnitude at these frequencies signals. Circuit diagram of the PFC using the hybrid PIDR controller is shown in Fig. 4.

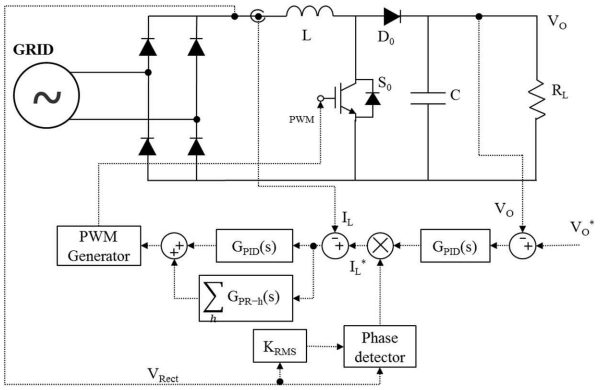


Fig. 4 Hybrid PIDR controller of the PFC

The PIDR controller includes a type-III PID controller in parallel with PR controllers. The type-III PID controller mainly controls DC (0 Hz) part of reference signal. The PR controllers only and mainly control reference signals which are coincident with its own resonant frequencies but no the others.

Because the PR controllers are adopted at frequencies 120 Hz, 240 Hz, 360 Hz, 480 Hz, the phase of open current loop including the type-III PID controller at resonant frequencies are required to be higher than -90-degree in range of 120 Hz - 480 Hz to maintain stability of the system. As presented in Fig. 2, the open current loop has 2 kHz of bandwidth, and has phase angle higher than -90-degree in range of 120 Hz - 480 Hz. Hence, the PID controller of the hybrid PIDR controller uses

the same parameters as mentioned in the last paragraph of subsection 2.2.

In practice, infinity magnitude of the transfer function of the PR controller can affect the stability of a system [7,13]. The transfer function of the PR controller is modified as follows:

$$G_{PR}(s) = k_p + k_r \frac{2\omega_c s}{s^2 + 2\omega_c s + \omega_o^2} \quad (8)$$

where ω_0 is the resonant frequency, and k_r is a constant that is selected to shift the magnitude of the transfer function of the PR controller vertically. To obtain null magnitude at the other frequencies, k_p equals 0.

The magnitude of the transfer function of the PR controller at resonant frequency described in (8) does not reach infinite, but it is still high enough to enforce a small steady-state error in high-frequency signals. The bandwidth of the PR controller can be widened by altering ω_c. The Bode diagram of the PR controller with k_p=1, k_r=100, ω_c = 0.01 rad/s, 120 Hz, 240 Hz, 360 Hz, and 480 Hz resonant frequencies is shown in Fig. 5.

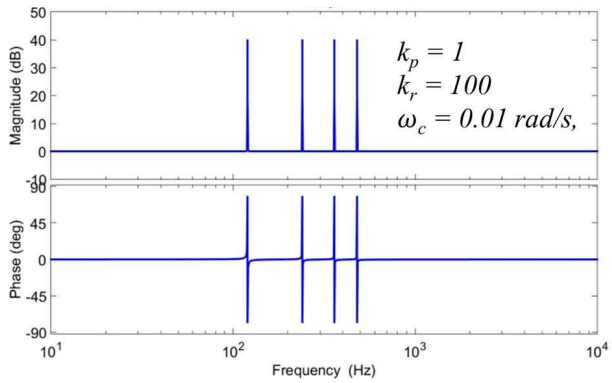


Fig. 5 Bode diagram of transfer function of the PR controller at 120 Hz, 240 Hz, 360 Hz, and 480 Hz

As in (8), the selected parameters of PR controller are zero of k_p to obtain null magnitude of the transfer function of the PR controller at non-resonant frequency, 100 of k_{r-h} to add 40 dB of magnitude of the transfer function of the PR controller at resonant frequencies (120 Hz, 240 Hz, 360 Hz, and 480 Hz), and 0.01 rad/s of ω_c of bandwidth. Bode diagram of open current loop including the PIDR controller was presented in Fig. 6.

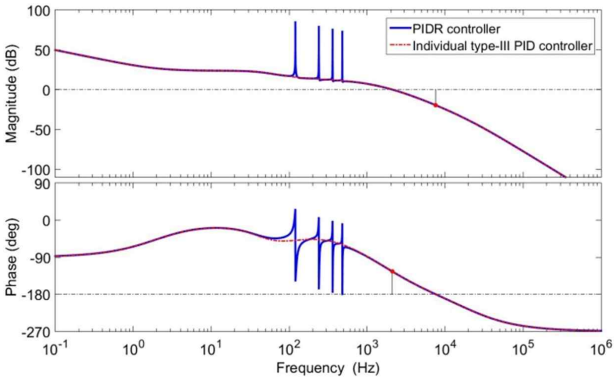


Fig. 6 Bode diagram of the open loop transfer function of the PFC using PIDR and type-III PID controller

Figure 6 clearly shows that the magnitudes of the transfer function of open current loop increased dramatically up 40 dB at 120 Hz, 240 Hz, 360 Hz, and 480 Hz, using the hybrid PIDR controller, as compared to the use of individual type-III PID controller. The bandwidth and phase margin of open current loop are also satisfied.

4. Simulation and Hardware Experiment

4.1 An Individual Type-III PID Controller

To verify the design of the type-III PID and PIDR controllers, the single-phase PFC is simulated with the both controllers in a continuous-time domain in PSCAD/EMTDC.

The time step in the simulation is 5 s. Circuit diagram of the simulation in PSCAD/EMTDC and the simulation results are shown in Fig. 7 and Fig. 8, respectively. The parameters of the PFC are presented in Table 1.

Table 1 Parameters of the PFC

Parameter	Value	Parameter	Value
Input voltage	220 V	Output voltage	380 V
AC line frequency	60 Hz	Output current	7.9 A
Switching frequency	20 kHz	Power	3 kW
Boost inductor	2.5 mH	Boost capacitor	3,290 F

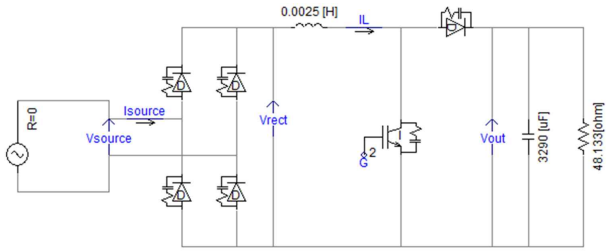
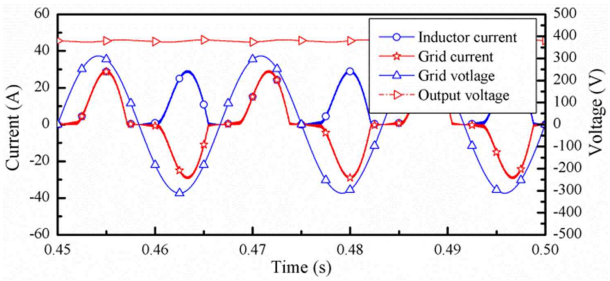


Fig. 7 Circuit diagram of the PFC in PSCAD/EMTDC

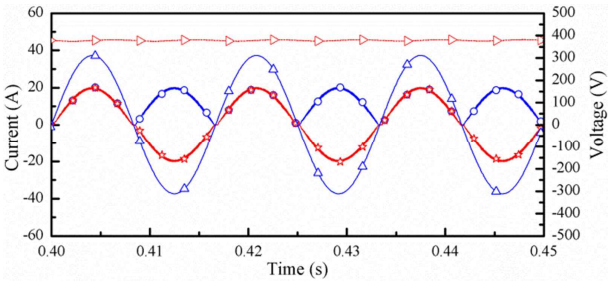
As depicted in Fig. 8, the grid current of the PFC using the individual type-III PID controller has high distortion in which the grid current waveform is poor. In contrast, the grid current of the PFC using PIDR controller has low distortion in grid current. The waveform of grid current is much better than that of the case using the type-III PIDR controller.

4.2 Experiment and the Results

The 3 kW single-phase PFC prototype hardware is used to experiment both the individual type-III PID and the hybrid PIDR controllers. The same parameters as in Table 1 are used. DSP TMS320F28335, a product of Texas Instruments, is used to implement the controllers and generate a PWM signal. The backward Euler method is used to discretize the transfer function of both controllers. The current and voltage are measured using hall sensors, HC-PDA and OPAM circuits, respectively. These signals are sampled by ADCs at a switching frequency of 20 kHz.



(a) Individual type-III PID controller



(b) Hybrid PIDR controller

Fig. 8 Simulation results of the PFC

Fig. 9 Hardware setup for experiment

The measurement signals are filtered by Butterworth filters to reduce noise, switching ripples, and sampling effects. The RMS and absolute instantaneous voltage value of the grid are used to calculate the grid phase angle. The grid voltage is supplied from a real grid in the laboratory. The hardware setup of the experiment is presented in Fig. 9.

To compare the performance of the controllers, the steady-state performances of nominal and light load are evaluated in terms of THD, and output voltage regulation.

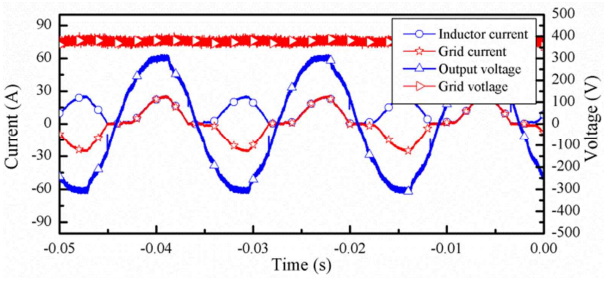
The summary of experiment results if the PFC with individual type-III PID and hybrid PIDR controllers are shown in Table 2.

Table 2 Experiment results of the PFC with individual type-III and hybrid PIDR controllers

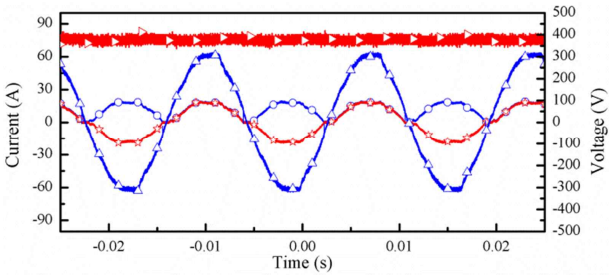
Parameter	Type-III	PIDR
Output voltage	377.6 V	378 V
Grid current (RMS)	13.96 A	12.98 A
THD	33.98%	9.78%
3nd harmonic current	6.5 A	1 A

Figure 10 (a) illustrates the steady-state input grid voltage, current, inductor current, and output voltage of the PFC using the individual type-III PID controller, and Fig. 10 (b) depicts those of the hybrid PIDR controller. Using the individual type-III PID controller, the harmonics of the grid current are high, even at full load. The shape of the grid current was poor in the PFC using the type-III PID controller.

As shown in Fig. 10 (b), the shape of the grid current using the hybrid PIDR controller is similar to that of the grid voltage. Using the hybrid PIDR controller, the PFC has lower inductor current of 13.08 A, and the input grid current of 12.98 A comparing to those of 14.04



(a) Individual type-III PID Controller



(b) PIDR controller

Fig. 10 Steady-state experiment of the PFC

A and 13.96 A of the individual type-III PID controller, respectively. The output voltage of the PFC using the PIDR and the individual type-III controller are 377.6 V and 378.0 V, respectively. The spectrum of the grid current using both the type-III PID and PIDR controller are presented in Fig. 11. The THD of the grid current using the PIDR controller (9.78%) is much lower than the THD of grid current using the individual type-III PID controller (33.98%).

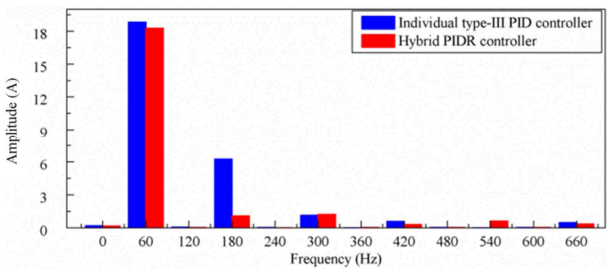
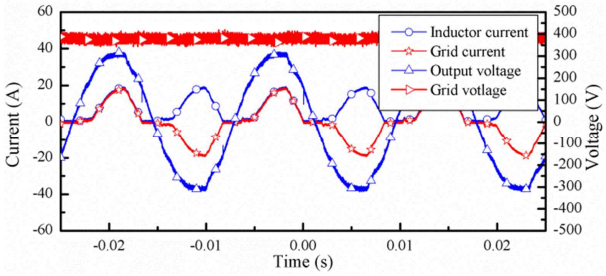
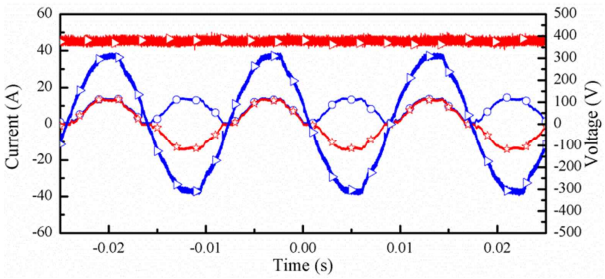


Fig. 11 Spectrum of the grid current in nominal load

Figure 12 shows the performance of the PFC in 71.5% of nominal load using the individual type-III PID controller in (a), and the hybrid PIDR controller in (b).



(a) Individual type-III PID controller



(b) PIDR controller

Fig. 12 Light load experiment of the PFC (71.5 %)

The output voltage of the PFC using both controllers reach the reference voltage (377.3 V of 380 V reference). The PFC using the hybrid PIDR controller also has performance of grid current (13.0% of THD) much better than those of using individual type-III PID controller (40.56 % of THD).

Comparing to [8,15,16], the THD of a single-phase PFC (100 kHz switching frequency) using notch filter or nonlinear controllers are around 4-7% (nominal load) and 6-19% (16% of nominal load) with a perfect sinusoidal voltage source condition. In this paper, the phase angle of grid voltage is directly calculated by the instantaneous value and RMS value of the real grid voltage in laboratory. As presented through the experiment results, the grid voltage contains harmonics. Therefore, the harmonics of the grid voltage affects the phase angle. The affection can be recognized easily by the waveform of current and voltage of grid in Fig. 13 (zoom in from Fig. 10 (b)). This is the main reason why the THD of grid current reaches approximately 9.78% (nominal load) and 13.0% (71.5% nominal load) by using the hybrid PIDR controller. The phase angle detection algorithm is going to be a up-coming research topic to improve the performance of the PFC in the real grid operation condition.

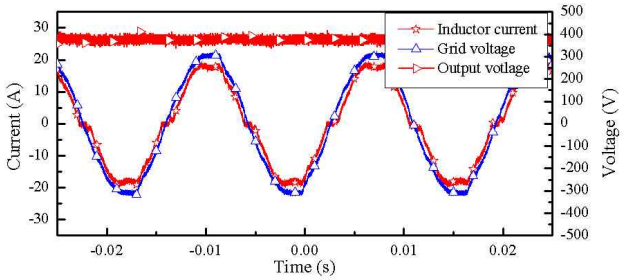


Fig. 13 Zoom in of experiment result under nominal load using the hybrid PIDR controller

5. Conclusion

This paper proposed a hybrid PIDR controller combining a type-III PID and PR controllers to improve the drawbacks of the individual type-III PID controller in the PFC. The type-III PID controller was selected to taking into account the bandwidth and phase margin of the PFC. The PR controller was adopted to enforce small steady-state error for controlling the high frequency current. The hybrid PIDR and an individual type-III PID controllers were simulated in PSCAD/EMTDC and implemented successfully in a single-phase

PFC hardware. The THD of the proposed controller (9.78%) are much better than the results of the individual type-III PID controller (33.78%). The hybrid PIDR controller has good performance under light load conditions. The distortion and THD in light load case of the hybrid PIDR controller increase slightly, but the individual type-III PID controller shows much higher. As a result, the hybrid PIDR controller is able to track and control high-frequency sinusoidal reference signals well, and thus demonstrated better performances.

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