

# Influence of Electron and Hole Distribution on 2T SONOS Embedded NVM

Woo Young Choi<sup>1,\*</sup>, Da Som Kim<sup>1</sup>, Tae Ho Lee<sup>2</sup>, Young Jun Kwon<sup>2</sup>,  
Sung-Kun Park<sup>2</sup>, and Gyuhan Yoon<sup>1</sup>

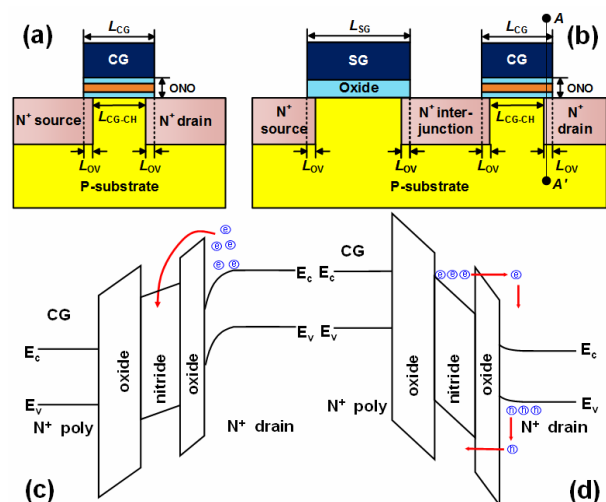
**Abstract**—The influence of electron and hole (EH) distribution on two-transistor (2T) silicon-oxide-nitride-oxide-silicon (SONOS) embedded nonvolatile memory (eNVM) is investigated in terms of reliability. As PE (program/erase) cycles are repeated, it is observed that the electron distribution in the nitride layer becomes wider. It leads to the EH distribution mismatch, which degrades the reliability of 2T SONOS eNVM.

**Index Terms**—2T SONOS, eNVM, mismatch, reliability

## I. INTRODUCTION

A two-transistor (2T) silicon-oxide-nitride-oxide-silicon (SONOS) memory cell has been considered as an attractive option to embedded nonvolatile memory (eNVM) due to its over-erase immunity and CMOS process compatibility [1]. Unlike a standalone SONOS NAND flash memory cell which uses Fowler-Nordheim tunneling for both program/erase (PE) operations, a 2T SONOS eNVM cell uses different PE mechanisms: channel hot electron injection (CHEI) for program operation and band-to-band-tunneling-induced hot-hole injection (BTBT-HHI) for erase operation. It is because low-voltage and high-speed operation are required for eNVM. However, because a 2T SONOS eNVM cell uses

different PE mechanisms and charge trapping storage region, the mismatch between trapped electron and hole (EH) distribution can cause reliability issues. In the case of one-transistor (1T) SONOS eNVM cells shown in Fig. 1(a), the EH distribution mismatch has already been discussed elsewhere [2-4]. On the other hand, to the best of our knowledge, no EH distribution mismatch has been discussed so far in the case of 2T SONOS eNVM cells as shown in Fig. 1(b). This manuscript contributes to the reliability degradation of 2T SONOS eNVM cells induced by the EH distribution mismatch. Fig. 1(c) and (d) show their PE mechanisms by using vertical energy band diagrams. CHEI program is used to accelerate the electron trapping because interjunction between select gate (SG) and control gate (CG) potential decrease as voltage drop at the pinch-off region increases due to the



**Fig. 1.** Schematics of (a) 1T, (b) 2T SONOS eNVM cell. Vertical energy band diagram extracted from the  $A-A'$  line during, (c) program, (d) erase operation.

Manuscript received Jan. 24, 2016; accepted Apr. 10, 2016

<sup>1</sup> Department of Electronic Engineering, Sogang University, 35 Baekbeom-ro, Mapo-gu, Seoul, Korea

<sup>2</sup> System IC Division, SK Hynix, Inc, Cheongju, Chungcheongbuk-do, Korea

E-mail : wchoi@sogang.ac.kr

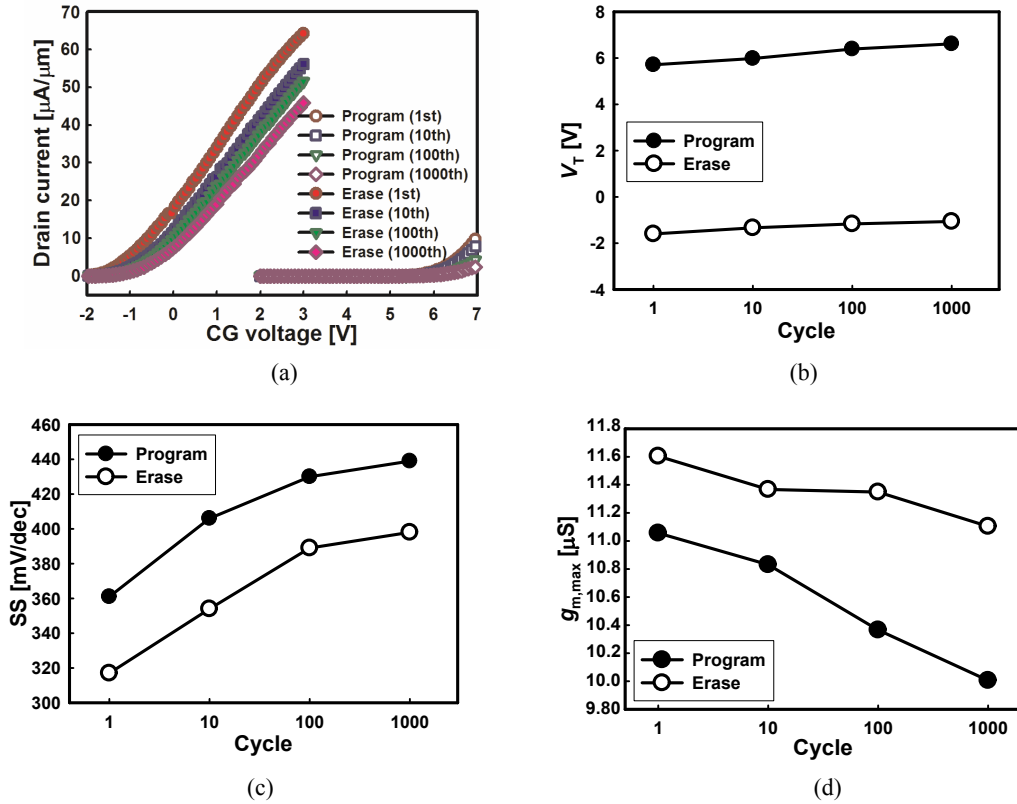


Fig. 2 (a) Measured  $I_{DS}$ - $V_{GS}$ , (b)  $V_T$ , (c) SS, (d)  $g_{m,max}$ .

trapped electrons. However, CHEI program induces electron trapping widening, which leads to EH distribution mismatch. Thus, EH distribution mismatch on 2T cells is more severe than 1T cells. It is problematic that EH distribution mismatch is aggravated as PE cycles are repeated.

## II. RESULTS AND DISCUSSION

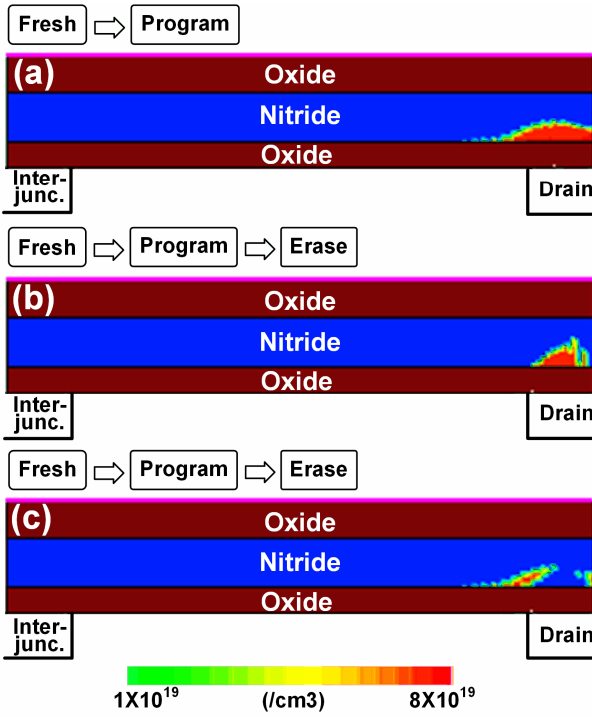
Fig. 2 shows the measurement results of 100-nm 2T SONOS eNVM cell. Its PE conditions are summarized in Table 1. In the case of program operation, gate voltage is higher than drain voltage due to a thick ONO stack. It has been observed that the pile-up of electrons during each PE cycle results in threshold voltage ( $V_T$ ) shift, subthreshold slope (SS) and maximum transconductance ( $g_{m,max}$ ) degradation. In order to observe the mismatch between trapped EH distribution at each PE state, two-dimensional device simulation has been performed by using Synopsys Sentaurus [5]. Fig. 1(b) shows the simulated 2T SONOS cell structure. The select gate length ( $L_{SG}$ ) is 200 nm. Control gate length ( $L_{CG}$ ) is 100

Table 1. Program/erase conditions

Operation	$V_{SG}$	$V_{CG}$	$V_D$	$V_S$	Time
Program	5.0 V	7.0 V	4.5 V	0 V	20 $\mu\text{s}$
Erase	5.0 V	0 V	4.5 V	Float	100 ms

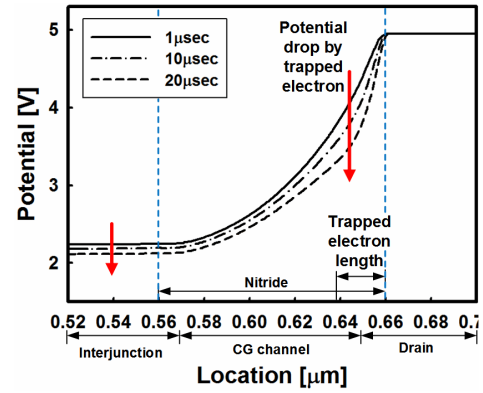
nm. Gate overlap length ( $L_{OV}$ ) is 10 nm. ONO stack thickness is 6/8/4.5 nm respectively. Graded source/drain junction doping gradient from gate edge is 5 nm/dec. CHEI and BTBT-HHI have been used for program and erase operation, respectively as shown in Table 1. Read operation has been performed by exchanging source and drain regions with  $V_D$  fixed at 1 V. It should be noted that model parameters such as effective tunneling mass are adjusted to make one PE cycle in device simulation correspond to 200 PE cycles in measurement for short simulation time and higher convergence.

Fig. 3 and show the simulated profiles of trapped electrons and holes during the first PE cycle. Narrow electron distribution is related to maximum lateral electric field position of CG during program. Because interjunction has floating potential, decreased voltage drop at the pinch-off region by trapped electron makes interjunction potential decrease as shown in Fig. 4(a).

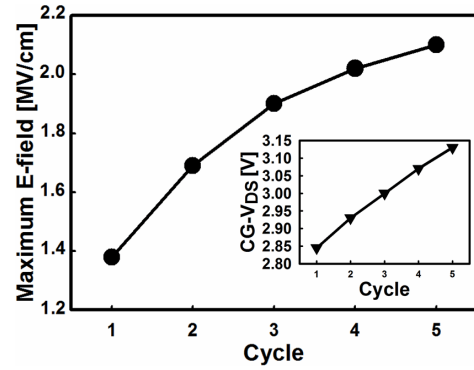


**Fig. 3.** (a) Simulated trapped electron distribution in CG after the first program operation, (b) Simulated trapped hole distribution in CG after the first erase operation, (c) Simulated trapped electron distribution in CG after the first erase operation.

Thus, the electron trapping is accelerated by increased maximum lateral electric field during program operation. After the first PE cycle, some trapped electrons still remain as shown in Fig. 3(c). This mismatch causes the voltage applied to the CG ( $CG-V_{DS}$ ) and maximum lateral electric field increase as PE cycles are repeated. The inset of Fig. 4(b) shows the  $CG-V_{DS}$  versus the PE cycle number. The maximum lateral electric field increases as PE cycles are repeated as shown in Fig. 4(b). Program acceleration becomes more severe as the PE cycle repeated. Thus, EH distribution mismatch of 2T cells is more severe than that of 1T cells as PE cycles are repeated as shown in Fig. 5. Fig. 6 shows that the  $V_T$  shift, SS and  $g_{m,max}$  of 2T cells are degraded as the local pile up of electrons increases. First,  $V_T$  degradation is explained by the increase of source-to-channel potential barrier height due to the EH mismatch. When the electrons are trapped in the nitride layer over the channel, the channel energy band under the trapped electrons tends to shift upward [7]. Second, SS degradation is related to the channel surface which is controlled by the gate voltage [8-10]. In the subthreshold region, the surface channel

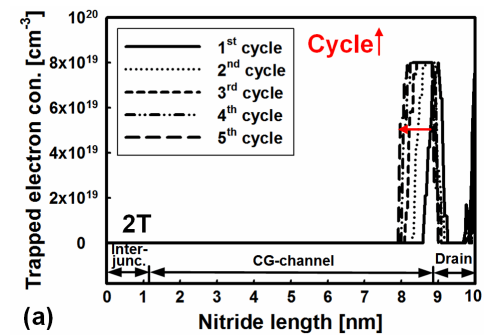


(a)

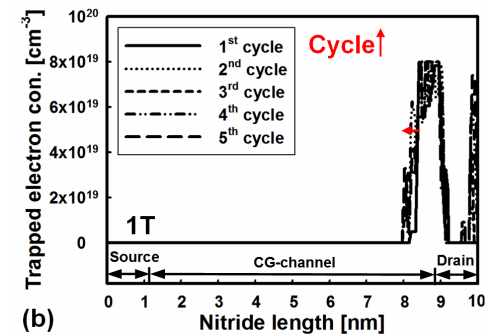


(b)

**Fig. 4.** (a) Simulated potential during the first program, (b) Simulated maximum lateral electric field during five PE cycles. The inset shows that  $V_{DS}$  of CG increases during five PE cycles.



(a)



(b)

**Fig. 5.** Simulated electron distribution in the erased state as PE cycles are repeated for (a) a 2T, (b) 1T cell.

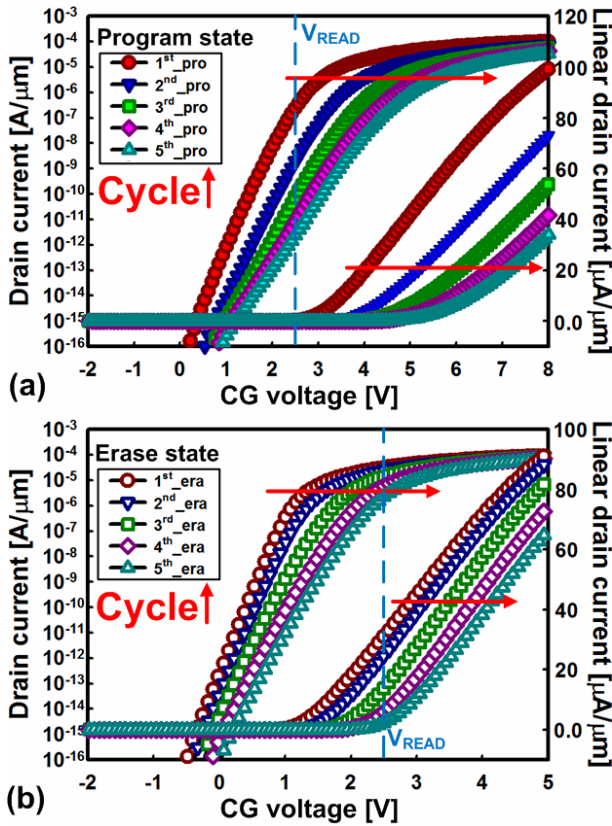


Fig. 6. Simulated  $I_{DS}-V_{GS}$  during five PE cycles (a) when programmed, (b) when erased.

under the trapped electrons is depleted and the rest of the surface channel is inverted, which means poor coupling between the gate and surface channel. Finally,  $g_{m,avr}$  degradation is related to parasitic source resistance. When electrons are trapped over the graded junction, the electron concentration of graded junction decreases.

### III. CONCLUSIONS

The influence of EH mismatch on 2T SONOS eNVM has been discussed for the first time. During the program operation of 2T cells, electron distribution is wider than hole distribution due to the accelerated electron trapping. Thus, EH distribution becomes worse as PE cycles are repeated. It is also observed that the 2T SONOS eNVM cells are more vulnerable to the EH distribution mismatch than 1T ones.

### ACKNOWLEDGMENTS

This work was supported in part by the NRF of Korea

funded by the MSIP under Grant NRF-2015003565 (Mid-Career Researcher Program), in part by the KEIT funded by the MOTIE under Grant 10041855 (IT R&D Program) and in part by the MOTIE/KSRC under Grant 10044842 (Future Semiconductor Device Technology Development Program).

### REFERENCES

- [1] Y. Kwon, T. Lee, J. Kim, S. Park, I. Cho and K. Yoo, "Characterization of 64kB Test Chip for Touch Application on 90nm SONOS Technology," *Proc. IEEE 6<sup>th</sup> International Memory Workshp*, pp. 1-4, May. 2014.
- [2] A. Furnemont, M. Rosmeulen, J. Van Houdt, H. Maes, and K. De Meyer, "Cycling behavior of nitride charge profile in NROM-type memory cells," in *Proc. 21st Non-Volatile Semicond. Memory Workshp*, pp. 66-67, Feb. 2006.
- [3] A. Padovani, L. Larcher, and P. Pavan, "Hole distributions in erased NROM devices: profiling method and effects on reliability," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 343-349, Jan. 2008.
- [4] N. K. Zous, M. T. Lee, W. J. Tsai, A. Kuo, L. T. Huang, T. C. Lu, C. J. Liu, T. Wang, W. P. Lu, W. Ting, J. Ku, and C.-Y. Lu, "Lateral migration of trapped holes in a nitride storage flash memory cell and its qualification methodology," *IEEE Electron Devices Lett.*, vol. 25, no. 9, pp. 649-651, Sep. 2004.
- [5] Sentaurus Device User Guide Version: H-2013.03, Synopsys, 2013.
- [6] A. Shappir, D. Levy, Y. Shacham-Diamand, E. Lusky, I. Bloom, and B. Eitan, "Spatial characterization of localized charge trapping and charge redistribution in the NROM device," *Solid-State Electron.*, vol. 48, no. 9, pp. 1489-1495, Sep. 2004.
- [7] E. Lusky, Y. Shacham-Diamand, G. Mitnberg, A. Shappir, I. Bloom, and B. Eitan, "Investigation of channel hot electron injection by localized charge-trapping nonvolatile memory devices," *IEEE Trans. Electron Devices*, vol. 51, no. 3, pp. 444-451, Mar. 2004.
- [8] E. Lusky, Y. Shacham-Diamand, B. Eitan, and I. Bloom, "Characterization of channel hot electron

injection by the subthreshold slope of NROM device,” *IEEE Electron Device Lett.*, vol. 22, no. 11, pp. 556-558, Nov. 2001.

- [9] L. Larcher, G. Verzellesi, P. Pavan, E. Lusk, I. Bloomm, and B. Eitan, “Impact of programming charge distribution on threshold voltage and subthreshold slope of NROM memory cells,” *IEEE Trans. Electron Devices*, vol. 49, pp. 1939-1946, Nov. 2002.
- [10] A. Shappir, Y. Shacham-Diamand, E. Lusk, I. Bloom, B. Eitan, “Subthreshold slope degradation model for localized-charge-trapping based non-volatile memory devices,” *Solid-State Electron.*, vol. 47, no. 5, pp. 937-941, May. 2003.



**Woo Young Choi** received the B.S., M.S. and Ph. D. degrees in the School of Electrical Engineering from Seoul National University, Seoul, Korea in 2000, 2002 and 2006, respectively. From 2006 to 2008, he was with the Department of

Electrical Engineering and Computer Sciences, University of California, Berkeley, USA as a post-doctor. Since 2008, he has been a member of the faculty of Sogang University (Seoul, Korea), where he is currently an Associate Professor with the Department of Electronic Engineering. He has authored or coauthored over 120 papers in international journals and conference proceedings and holds 25 Korean patents. His current research interests include fabrication, modeling, characterization and measurement of CMOS/CMOS-compatible semiconductor devices and nanoelectromechanical (NEM) relays/memory cells.



**Da Som Kim** received the B.S. degree in 2013 from Sejong University, Seoul, Korea. She is currently working toward the M.S. degree in the Department of Electronic Engineering, Sogang University, Seoul, Korea. Her current research interests

include embedded nonvolatile memory (eNVM) and nanoscale novel devices.



**Tae Ho Lee** received the B.S. degrees in the Department of Electronic Engineering from Ulsan University, Ulsan, Korea in 2008. In 2007, he joined the CIS development group, SK hynix, where he worked on tech development for CIS logic. From

2009 to 2012, he worked the DDI development group, where he worked on tech development and product engineering for DDI. He is currently working toward the technology development group, where he was responsible for embedded Flash and logic development.



**Young Jun Kwon** received the B.S., and M.S. degrees in the Department of Semiconductor Engineering from Chungbuk National University, Cheongju, Korea in 2004 and 2006, respectively. From 2006 to 2011, he worked the product development

group, Magnachip and Donbuhitek Semiconductor, where he worked on product engineering for EEPROM, embedded Flash. He is currently working toward the technology development group, SK Hynix Semiconductor, where he was responsible for BCDMOS and embedded Flash and CIS development.



**Sung-Kun Park** was born in Korea, in 1969. He received his B.S. degree in 1992 from Ulsan University, Ulsan, Korea, M.S. degree in 1996 from Pusan National University, Pusan, Korea, and his Ph.D. degree in electronic engineering from Kyungpook

National University, Daegu, Korea, in 2000. Since 2000, he has been working as a semiconductor device and process integration engineer in SK hynix and Dongbu electronics. He is currently with SK hynix Semiconductor Inc., Cheongju, Korea. His research interest includes bipolar-CMOS-DMOS (BCDMOS) for smart power IC, pixel for CMOS image sensor (CIS), and nonvolatile memory (NVM). Especially, embedded nonvolatile memories including single poly NVM without additional processes and SONOS are major research interests.



**Gyuhan Yoon** received the B.S., and M.S. degrees in the Department of Electronic Engineering from Sogang University, Seoul, Korea in 1981 and 1984, respectively. In 1984, He joined the memory development group, LG Semiconductor, where he

worked on product engineering for EPROM, SRAM and DRAM, From 2000 to 2009, he was an executive manager of R&D division, Hynix Semiconductor, where he was responsible for DRAM and CIS development. He is currently a director of semiconductor group, Sogang Institute of advanced technology, Sogang University. He has authored or coauthored over 10 papers. He is the holder of 20 Korean patents and 4 international patents. His current research interests include the reliability of semiconductor memory.