JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, VOL.16, NO.5, OCTOBER, 2016
http://dx.doi.org/10.5573/JSTS.2016.16.5.687
ISSN(Print) 1598-1657
ISSN(Online) 2233-4866

A Transformer-Matched Millimeter-Wave CMOS Power Amplifier

Seungwon Park and Sanggeun Jeon

Abstract—**A differential power amplifier operating at millimeter-wave frequencies is demonstrated using a 65-nm CMOS technology. All of the input, output, and inter-stage network are implemented by transformers only, enabling impedance matching with low loss and a wide bandwidth. The millimeter-wave power amplifier exhibits measured small-signal gain exceeding 12.6 dB over a 3-dB bandwidth from 45 to 56 GHz. The output power and PAE are 13 dBm and 11.7%, respectively at 50 GHz.**

Index Terms—**CMOS, millimeter-wave, power amplifier, transformer**

I. INTRODUCTION

The CMOS single-chip transceivers have been widely implemented at RF and microwave frequencies for low cost and high reliability [1, 2]. As the gate width scales down deeply, the single-chip solution becomes feasible even at millimeter-wave (mm-wave) frequencies [3, 4]. Nonetheless, a CMOS power amplifier (PA) is still one of the most challenging blocks to integrate on the single-chip transceivers because of low breakdown voltage and high passive-component loss. This challenge becomes exacerbated as the frequency increases to mm-wave band.

Several mm-wave CMOS PAs have been reported for space satellite applications at Q band and for gigabit short-range communications such as WPAN or wireless HD at V band [5-11]. In the PAs, transmission lines, stubs, baluns, or transformers were used for impedance matching and power combining. Especially, an on-chip transformer is a very promising component for mm-wave PAs. As the frequency increases, the inductance value required for impedance matching is lowered and thus making the transformer smaller and less lossy. This allows for PA design with a compact size and high gain. Therefore, a transformer has been widely employed not only for low-frequency PAs [12-14], but also for several mm-wave PAs. However, some mm-wave PAs based on transformers still suffer from a narrow bandwidth [6, 7] or low output power [5].

In this paper, we demonstrate an mm-wave wideband PA implemented in a 65-nm CMOS technology. To achieve low-loss and wideband operation, transformers are employed and optimized for the input, inter-stage, and output matching network. In Section II, the PA design details are described. The measurement results are given in Section III, followed by conclusions in Section IV.

II. MM-WAVE PA DESIGN

A schematic of the proposed mm-wave PA is shown in Fig. 1. The PA employs a 3-stage differential common-source topology. The total gate width of the first two stages is 160 μm and the last stage has a total gate width of 240 μm to achieve high output power. The impedance matching and power combining is fulfilled by four transformers (X_1–X_4).

1. Transistor Cell Layout

In the proposed PA, each transistor cell (M_1–M_6) is

Manuscript received Mar. 29, 2016; accepted Jul. 19, 2016
School of Electrical Engineering, Korea University, Seoul 136-713, Korea
E-mail : sgjeon@korea.ac.kr

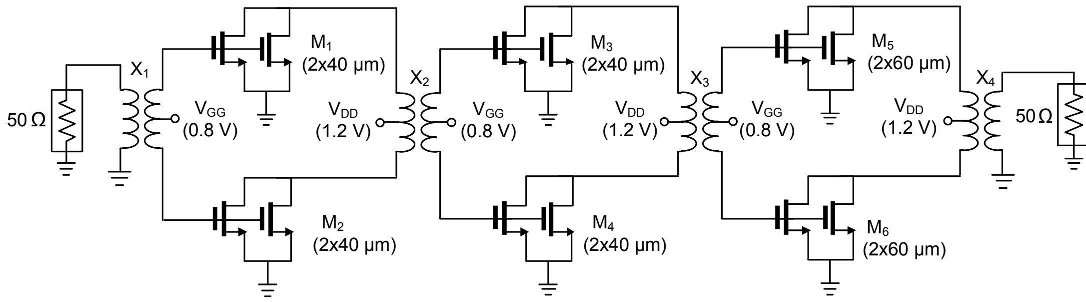

Fig. 1. Schematic of the transformer-matched mm-wave PA.

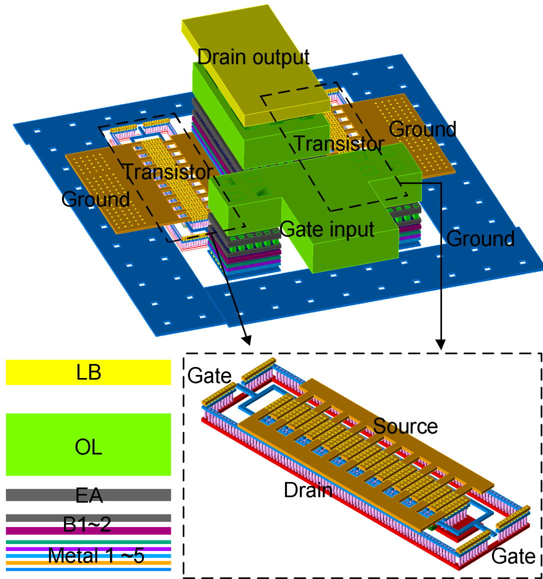

Fig. 2. Layout of the combined transistor cell (M_1–M_4) with a total gate width of 2 x 2 μm x 20 fingers.

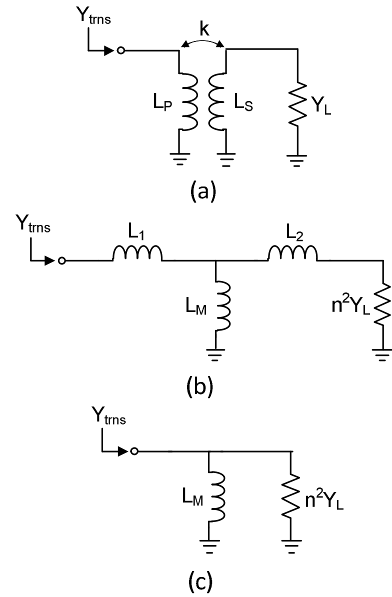

Fig. 3. Transformer loaded by Y_L at the secondary winding (a), its T-equivalent circuit (b), simplified equivalent circuit when *k* is high at mm-wave frequencies (c).

composed of two unit transistors that are combined for high operation frequency and high output power. Fig. 2 shows the layout of the transistor cell used for the first and second stages (M_1–M_4). The metal layer profile is also shown. Two unit transistors, each having twenty gate fingers of 2-μm width, are placed with drain and source flipped over to each other.

There are two gate feeds located at the opposite sides of a unit transistor. However, only one side of the gate feed is used for interconnection to simplify the layout and avoid excessive parasitic capacitance. The gate feeds from two unit transistors are combined using M1 layer and go up to the second top layer (OL) for low-loss interconnection to the transformer. The drains are combined in the middle of two transistors with M2 layer and go up to the top layer (LB) for interconnection. The sources are grounded with a sufficient number of vias from M2 to M1. This dual combined transistor cell reduces gate parasitic resistance significantly and improves power gain compared to a single transistor cell with the same gate width.

2. Transformer Design

A transformer loaded by an admittance Y_L at the secondary winding is shown in Fig. 3(a). L_P and L_S are the inductances of the primary and secondary windings respectively, and *k* is a coupling coefficient. Then, the admittance seen looking into the primary winding Y_{trns}, can be readily calculated from a T-equivalent circuit of the transformer, as shown in Fig. 3(b). For simplicity of analysis, parasitic capacitances and resistances are neglected. The turn ratio (*n*), the mutual inductance (L_M)

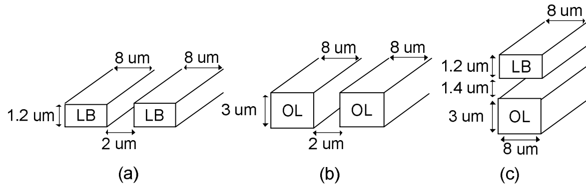

Fig. 4. Three coupled-line structures: Edge-coupled line using LB (a), edge-coupled line using OL (b), broadside-coupled line using LB and OL (c).

and the leakage inductances of the primary (L_1) and secondary (L_2) windings are determined by [15] :

$$n = \sqrt{\frac{L_S}{L_P}}\ , \tag{1}$$

$$L_M = k\sqrt{L_P L_S}\ , \tag{2}$$

$$L_1 = L_P - L_M\ , \tag{3}$$

$$L_2 = \frac{L_S - L_M}{n^2}\ . \tag{4}$$

According to Eqs. (2-4), L_1 and L_2 are significantly smaller than L_M when k is high enough. Furthermore, as the frequency increases to mm-wave band, the inductance required for impedance matching becomes smaller, thus reducing the physical size of the transformer. Then, the shunt-connected L_M becomes more dominant than the series-connected L_1 and L_2. Under these conditions, the equivalent circuit simply reduces to a shunt combination of L_M and Y_L, as shown in Fig. 3(c).

In order to obtain a high k, three coupled-line structures are considered and compared in simulation. Fig. 4(a) and (b) show two edge-coupled structures using top two thick metal layers (LB and OL layers respectively) with the minimum spacing of 2 μm. In addition, Fig. 4(c) shows a broadside-coupled structure between LB and OL. The line width of the structures is 8 μm. The simulated coupling coefficients for the three structures are 0.64, 0.74, and 0.86, respectively, at 50 GHz. Hence, we chose the broadside-coupled structure for the transformer design.

Fig. 5 shows a structure of the transformer used for the mm-wave PA in this work. The transformer employs a single turn to maximize the self-resonant frequency and Q-factor at the expense of slight increase of chip area at mm-wave frequencies. Two center taps are located at both primary and secondary windings for DC biasing in

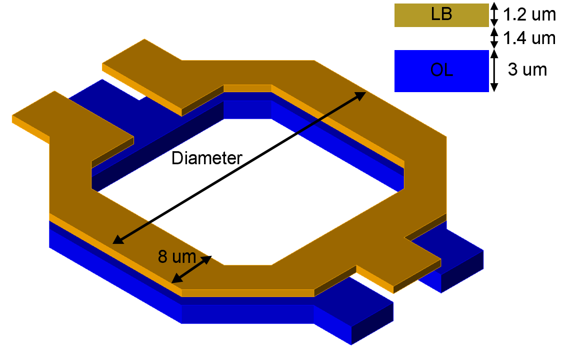

Fig. 5. A transformer structure including two center taps used for the mm-wave PA.

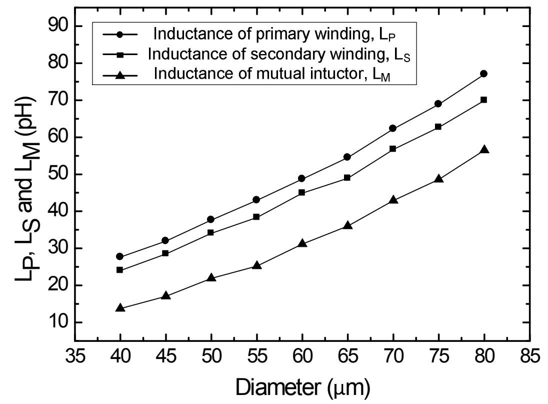

Fig. 6. Primary, secondary and mutual inductances versus the diameter of the transformer.

the inter-stage transformers (X_2 and X_3 in Fig. 1). Instead, the input and output transformers (X_1 and X_4) have a single center tap at one of the windings using the LB layer.

The diameter of the transformer is utilized as a design parameter to achieve individual impedance matching at each stage of the PA. In Fig. 6, the simulated L_P and L_S (half inductance values of the primary and secondary windings) are shown as a function of the diameter. The mutual inductance L_M is also calculated from Eq. (2). As shown in Fig. 3(c), when k of the transformer is high and the dimension is small, the load admittance Y_L is transformed to Y_{trns} dominantly by L_M. Therefore, the impedance matching can be performed by choosing a proper diameter that determines L_M, which is described in the following sections.

3. Design of Output Matching Network

A half equivalent circuit of the output matching

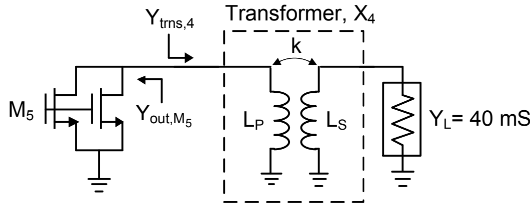

Fig. 7. Output matching network of the mm-wave PA.

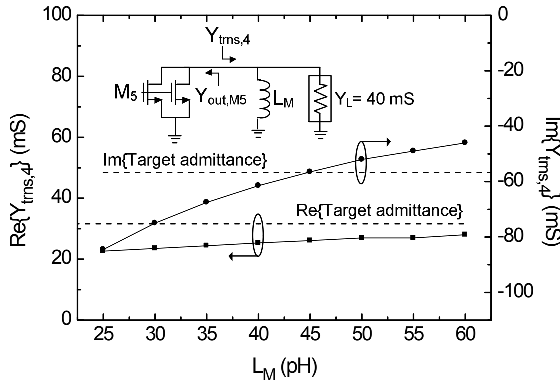

Fig. 8. Simulated $Y_{trns,4}$ at 50 GHz as a function of L_M. The target admittance of $Y_{trns,4}$ for the optimum matching is superimposed.

network of the PA is shown in Fig. 7. The primary and secondary windings of the transformer (X_4) are connected to M_5 and Y_L, respectively. For simplicity, the load impedance is approximated to be half of 50 Ω, thus resulting in Y_L = 40 mS. The output admittance of M_5 ($Y_{out,M5}$) is simulated as 7 + *j* 46 mS at 50 GHz, while the load-pull admittance for the maximum output power ($Y_{load\text{-}pull}$) is 59 – *j* 30 mS at 50 GHz. In order to achieve both high output power and high gain, the admittance seen looking into the transformer, $Y_{trns,4}$ should be compromised between $Y^*_{out,M5}$ and $Y_{load\text{-}pull}$. Therefore, we chose the target admittance of $Y_{trns,4}$ to be 32 - *j* 56 mS after several performance simulations.

In Fig. 8, $Y_{trns,4}$ is calculated as a function of shunt inductance that is placed between M_5 and Y_L. It is found that $Y_{trns,4}$ can be closely matched to the target admittance by using a single shunt inductor of 45 pH. This shunt inductor can be implemented by a mutual inductance L_M of the transformer (X_4), as shown in Fig. 3. According to Fig. 6, a diameter of around 70 μm will result in L_M of 45 pH. It should be noted that there are series leakage inductances of L_1 and L_2 which may also affect $Y_{trns,4}$. However, L_1 and L_2 are calculated from Eqs. (3, 4) to be 19 and 14 pH, respectively. These series

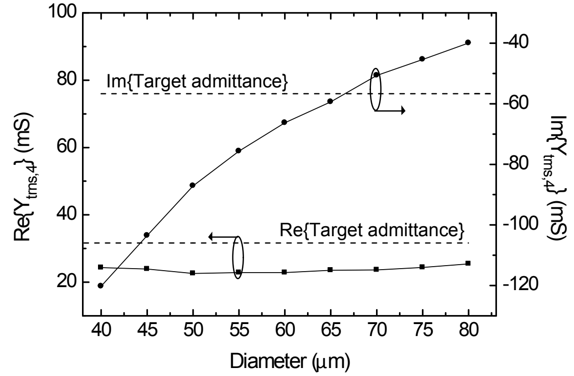

Fig. 9. Simulated $Y_{trns,4}$ at 50 GHz as a function of diameter of the transformer. The target admittance of $Y_{trns,4}$ for the optimum matching is superimposed.

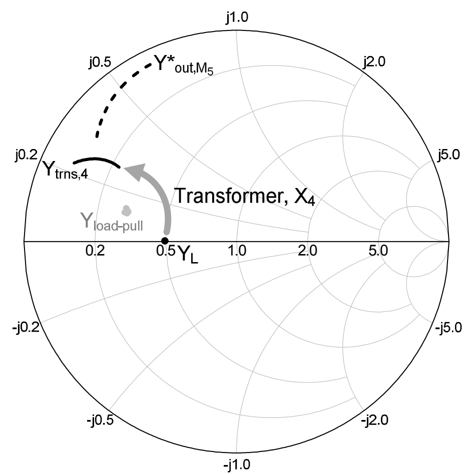

Fig. 10. Output matching process simulated from 40 to 60 GHz.

inductances correspond to reactance as small as 6 Ω and 4.4 Ω at 50 GHz, and thus they can be neglected in the first order. On the other hand, the susceptance of the shunt L_M of 45 pH is 70 mS at 50 GHz, which becomes a dominant component in the transformer. This reduces the transformer equivalent circuit to Fig. 3(c) and allows for the output impedance matching fulfilled simply by a single transformer.

To find the optimum diameter of the transformer, a full-wave EM simulation was performed and $Y_{trns,4}$ of the transformer is calculated versus the diameter, shown in Fig. 9. It is found that a diameter of 65 μm results in the real and imaginary values of $Y_{trns,4}$ which fulfill compromised matching to the target admittance. Fig. 10 shows the result of the output admittance transformation that is simulated from 40 to 60 GHz. As expected, the output load Y_L is transformed to $Y_{trns,4}$ by X_4, which is

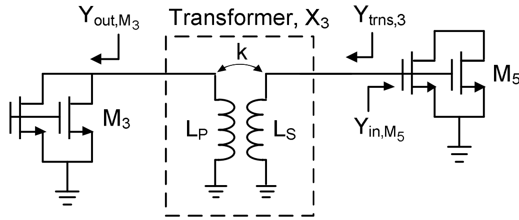

Fig. 11. Inter-stage matching network of the mm-wave PA.

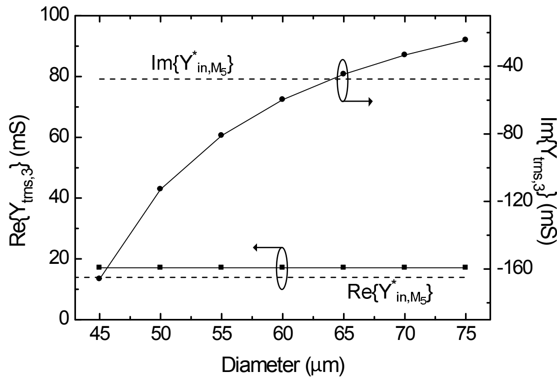

Fig. 12. Simulated $Y_{trns,3}$ at 50 GHz as a function of diameter of the transformer. The target admittance of $Y_{trns,3}$, which is $Y^*_{in,M5}$, is superimposed.

located between $Y^*_{out,M5}$ and $Y_{load\text{-}pull}$ to achieve both high gain and high output power.

4. Design of Inter-stage Matching Network

Fig. 11 shows a half equivalent circuit of the inter-stage matching network between M_3 and M_5. For high gain of the PA, $Y_{out,M3}$ is transformed by a transformer X_3 into $Y_{trns,3}$ that should be the complex conjugate of $Y_{in,M5}$. Since $Y_{out,M3} = 7 + j\ 36$ mS and $Y^*_{in,M5} = 14 - j\ 47$ mS at 50 GHz, the impedance transformation could be primarily fulfilled by a shunt inductor that is provided by the mutual inductance of X_3. To verify the feasibility, $Y_{trns,3}$ is simulated as a function of the diameter of X_3 and compared to $Y^*_{in,M5}$ in Fig. 12. It can be seen that a diameter of 65 µm achieves the optimum conjugate matching between M_3 and M_5. Fig. 13 shows the admittance transformation result of the inter-stage matching simulated from 40 to 60 GHz. The transformed admittance $Y_{trns,3}$ lies close to $Y^*_{in,M5}$ as expected. The matching performance is a little degraded at the high-frequency end due to the effect of parasitic components of the transformer other than L_M.

The inter-stage matching network between M_1 and M_3

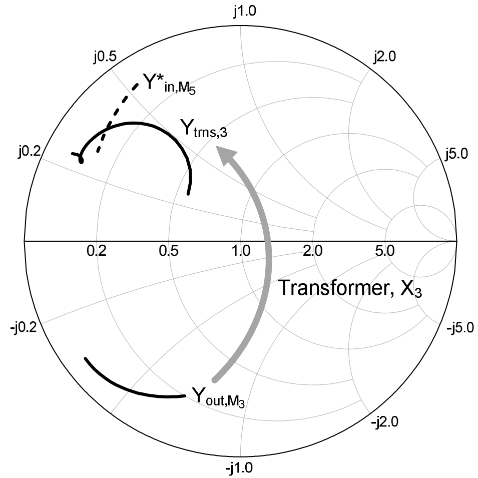

Fig. 13. Inter-stage matching process simulated from 40 to 60 GHz.

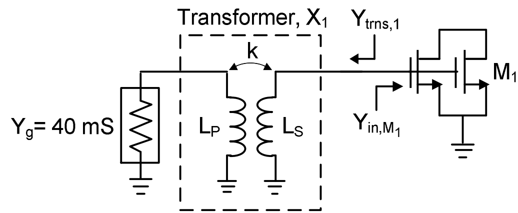

Fig. 14. Input matching network of the mm-wave PA.

is also designed with a transformer X_2 in a similar way. The mutual inductance of X_2 is utilized for conjugate matching and its diameter is determined to be 50 µm.

5. Design of Input Matching Network

Fig. 14 shows a half equivalent circuit of the input matching network. For conjugate matching, $Y_{trns,1}$ should be equal to $Y^*_{in,M1}$ which is simulated to be $3 - j\ 55$ mS at 50 GHz. However, as shown in Fig. 15, the real-part condition cannot be satisfied with a single transformer, and instead requires an additional series inductance of 9 pH. This small inductor is implemented using a short interconnection line of 70 µm between X_1 and M_1. Finally, the diameter of X_1 is determined to be 45 µm. The process of the admittance transformation from Y_g to $Y_{trns,1}$ is shown in Fig. 16.

III. MEASUREMENT

The PA is implemented in a 65-nm 1P10M low-power CMOS technology. The f_t and f_{max} of this technology are

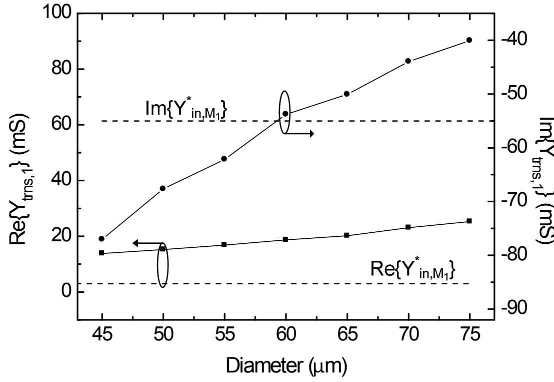

Fig. 15. Simulated $Y_{trns,1}$ at 50 GHz as a function of diameter of the transformer. The target admittance of $Y_{trns,3}$, which is $Y^*_{in,M1}$, is superimposed.

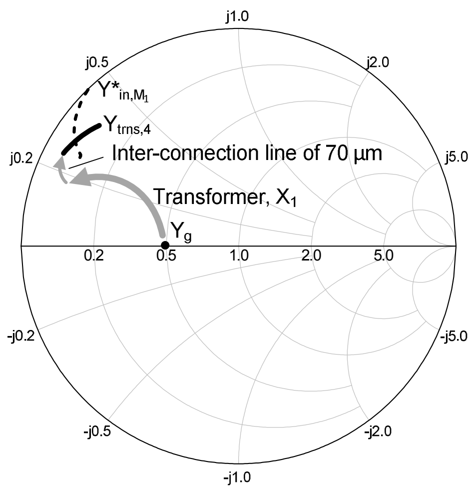

Fig. 16. Input matching process simulated from 40 to 60 GHz.

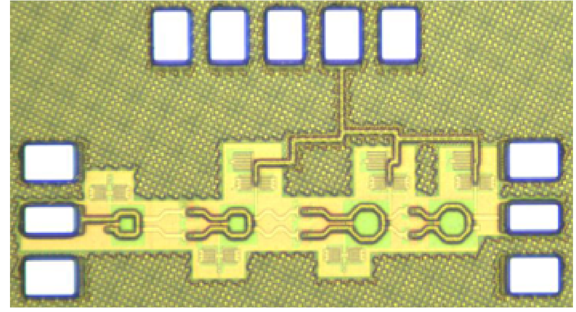

Fig. 17. Photograph of the mm-wave PA.

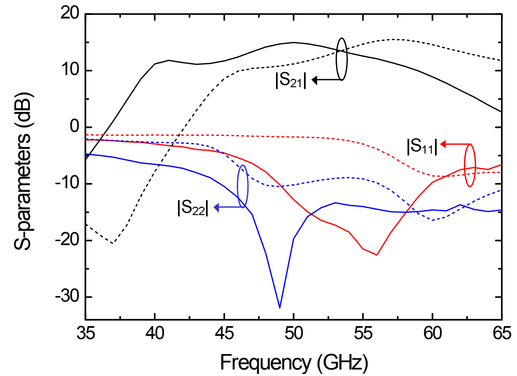

Fig. 18. Measured (solid line) and simulated (dashed line) S-parameters.

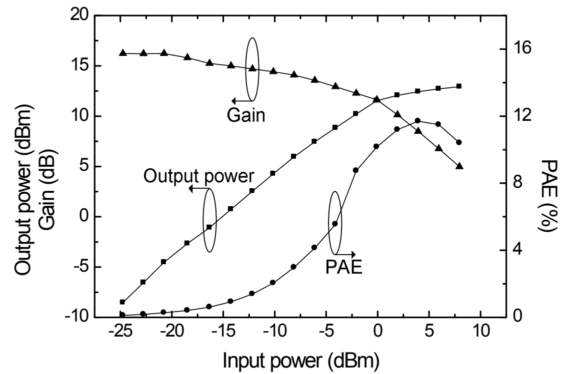

Fig. 19. Measured output power, gain and PAE versus the input power at 50 GHz.

180 and 200 GHz, respectively. The chip photograph of the PA is shown in Fig. 17. The chip size is 0.98 × 0.55 mm^2 including the probing pads. Fig. 18 shows the measured S-parameters of the PA. The peak small-signal gain is 15.6 dB at 50 GHz and the 3-dB bandwidth is 11 GHz from 45 to 56 GHz. Compared to the simulation, the measured gain is shifted by 5 GHz in frequency. The discrepancy presumably comes from inaccurate transistor model at mm-wave frequency band.

The measured output power, gain, and PAE versus the input power at 50 GHz are shown in Fig. 19. The maximum output power of 13 dBm is achieved with PAE of 11.7%.

Table 1 compares the performance of the proposed PA with that of other mm-wave CMOS PAs at the similar frequency band. The PA in this work exhibits relatively wideband operation and competitive output power and PAE due to the transformer-based matching network.

IV. CONCLUSIONS

An mm-wave PA is fabricated in a 65-nm CMOS technology. To achieve low-loss and wideband matching, all matching networks are implemented using transformers. The PA exhibits a peak gain of 15.6 dB and a 3-dB bandwidth ranging from 45 to 56 GHz. The peak

Table 1. Performance summary and comparison to other published CMOS PAs at similar frequency band

Ref.	Frequency (GHz)	P_{sat} (dBm)	Gain	peak PAE (%)	V_{DD} (V)	Technology
[5]	46	8.3 (@ 46 GHz)	8.5	17.8 (@ 46 GHz)	1.1	45-nm CMOS
[6]	50 – 59	11.4 (@ 58 GHz)	> 37.8	16.4 (@ 58 GHz)	1.2	65-nm CMOS
[7]	52.5 – 54.5	9.6 (@ 53.5 GHz)	> 26	17.3 (@ 53.5 GHz)	1.2	65-nm CMOS
[8]	52	10.6 (@ 56 GHz)	5.8	6.5 (@ 56 GHz)	1.1	45-nm CMOS
[9]	44 – 60	11 (@ 52 GHz)	> 5.3	7.1 (@ 52 GHz)	1.2	65-nm CMOS
This work	45 – 56	13 (@ 50 GHz)	> 12.6	11.7 (@ 50 GHz)	1.2	65-nm CMOS

output power and PAE are measured to be 13 dBm and 11.7%, respectively.

ACKNOWLEDGMENTS

This work was supported by BK21 plus through the National Research Foundation of Korea (NRF) funded by the Ministry of Science, ICT and Future Planning and by Defensive Specialized Laboratory for Terahertz Electronic Devices through Korean Agency for Defense Development (UD150043RD). The authors would like to thank IDEC for MPW and CAD tool support.

REFERENCES

[1] H. Darabi, S. Khorram, H.-M. Chien, M.-A. Pan, S. Wu, S. Moloudi, J. C. Leete, J. J. Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran and A. Rofougaran, "A 2.4-GHz CMOS transceiver for bluetooth," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 2016 – 2024, Dec. 2001.

[2] M. Zargari, D. K. Su, C. P. Yue, S. Rabii, D. Weber, B. J. Kaczynski, S. S. Mehta, K. Singh, S. Mendis and B. A. Wooley, "A 5-GHz CMOS transceiver for IEEE 802.11a wireless LAN system," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1688 – 1694, Dec. 2002.

[3] C. Marcu, D. Chowdhury, C. Thakkar, J.-D. Park, L.-K. Kong, M. Tabesh, Y. Wang, B. Afshar, A. Gupta, A. Arbabian, S. Gambini, R. Zamani, E. Alon and A. M. Niknejad, "A 90 nm CMOS low-power 60 GHz transceiver with integrated baseband circuitry," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3434 – 3447, Dec. 2009.

[4] J. Lee, Y.-A. Li, M.-H. Hung and S.-J. Huang, "A fully-integrated 77-GHz FMCW radar transceiver in 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2746 – 2756, Dec. 2010.

[5] M. Motoyoshi and M. Fujishima, "46 GHz differential power amplifier with 11 GHz bandwidth using on-chip transformer," *in Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol*., Aug. 2014, pp. 1 – 3.

[6] J. Lin, C. C. Boon, X. Yi and G. Feng, "A 50-59 GHz CMOS injection locking power amplifier," *IEEE Microw. Wireless Comp. Lett.,* vol. 25, no. 1, pp. 52 – 54, Jan. 2015.

[7] J. Lin, C. C. Boon, X. Yi and W. M. Lim, "A compact single stage V-band CMOS injection-locked power amplifier with 17.3% efficiency," *IEEE Microw. Wireless Comp. Lett.,* vol. 24, no. 3, pp. 182 – 184, Mar. 2014.

[8] K. Raczkowski, S. Thijs, W. D. Raedt, B. Nauwelaers and P. Wambacq, "50-to-67 GHz ESD-protected power amplifers in digital 45 nm LP CMOS," *in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2009, pp. 382 – 383.

[9] W. Fei, H. Yu, Y. Shang and K. S. Yeo, "A 2-D distributed power combining by metamaterial-based zero phase shifter for 60-GHz power amplifier in 65-nm CMOS," *IEEE Trans. Microw. Theory Tech*., vol. 61, no. 1 pp. 505 – 516, Jan. 2013.

[10] P. Chiang, W. Lin, T. Huang and H. Wang, "A 53 to 84 GHz CMOS power amplifier with 10.8-dBm output power and 31 GHz 3-dB bandwidth," *in IMS, 2014 IEEE MTT-S.*

[11] Y. Yoshihara, R. Fujimoto, N. One, T. Mitomo, H. Hoshino and M. Hamada, "A 60-GHz CMOS power amplifier with marchand balun-based parallel power combiner," in *IEEE A-SSCC Dig. Tech. papers, Nov. 2008,* pp.121-124.

[12] J. Jand, C. Park, H. Kim and S. Hong, "A CMOS RF power amplifier using an off-chip transmision line transformer with 62% PAE," *IEEE Microw.*

Wireless Comp. Lett., vol. 17, no. 5, pp. 385 – 387, May. 2007.
[13] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu and A. M.M Niknejad, "A 5.8 GHz 1 V linear power amplifier using a novel on-chip transformer power combiner in standard 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1054 – 1063, May. 2008.
[14] J. Jang,G. Liu, P. Haldi, T. J. K. Liu and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600 – 609, Mar. 2008.
[15] W. L. Lam and C. H. Chan, "Power amplifier with high transformation ratio power combiner in GaAs technology," *Proceedings of 2014 IEEE Int. Workshop on Electromagnetics,* pp. 199 – 200, May. 2014, Sapporo, Japan.

Seungwon Park received the B.S. and M.S. degrees in the electrical engineering from Korea University, Seoul, Korea, in 2013 and 2015, respectively, and is currently working toward the Ph.D. degree in electrical engineering from the same university. His research interest includes microwave and millimeter-wave power amplifier circuit.

Sanggeun Jeon received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2004 and 2006, respectively. From 1999 to 2002, he was a full-time Instructor in electronics engineering at the Korea Air Force Academy. From 2006 to 2008, he was a Research Engineer in the Caltech High-Speed Integrated Circuits Group, where he was involved with CMOS phased-array receiver design. Since 2008, he has been with the School of Electrical Engineering at Korea University, Seoul, Korea, where he is currently an Associate Professor. His research interests include integrated circuits and systems at microwave, mm-wave, and terahertz bands for high-speed wireless communication and high-resolution imaging applications.