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# Efficient Signature-Driven Self-Test for Differential Mixed-Signal Circuits

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*Abstract*—**Predicting precise specifications of *differential* mixed-signal circuits is a difficult problem, because analytically derived correlation between process variations and conventional specifications exhibits the limited prediction accuracy due to the phase unbalance, for most self-tests. This paper proposes an efficient prediction technique to provide accurate specifications of differential mixed-signal circuits in a system-on-chip (SoC) based on a nonlinear statistical nonlinear regression technique. A spectrally pure sinusoidal signal is applied to a differential DUT, and its output is fed into another differential DUT through a weighting circuitry in the loopback configuration. The weighting circuitry, which is employed from the previous work [3], efficiently produces different weights on the harmonics of the loopback responses, i.e., the signatures. The correlation models, which map the signatures to the conventional specifications, are built based on the statistical nonlinear regression technique, in order to predict accurate nonlinearities of individual DUTs. In production testing, once the efficient signatures are measured, and plugged into the obtained correlation models, the harmonic coefficients of DUTs are readily identified. This work provides a practical test solution to overcome the serious test issue of differential mixed-signal circuits; the low accuracy of analytically derived model is much lower by the errors from the unbalance. Hardware measurement results showed less than 1.0 dB of the prediction error, validating that this approach can be used as production test.**

*Index Terms*—**ADC, analog-to-digital converter, DAC, digital-to-analog converter, mixed-signal testing**

## I. INTRODUCTION

Cost in production test for a SoC can account for as much as nearly a half of the total manufacturing cost [1]. As a promising low-cost test solution, a self-test platform for SoCs has been attractive, which eliminates the need for a costly automated-test-equipment (ATE).

Overall performance of a SoC relies on that of the analog and mixed-signal intellectual-property (IP). A number of high-speed mixed-signal circuits for SoCs are designed by employing differential signaling for their inputs/outputs (I/O), due to higher immunity to environmental noise, and more. Self-test approach has been, however, hardly ever attempted for differential mixed-signal circuitry, because of the unbalance which is introduced by adding circuit components to differential I/O of a device-under-test (DUT) for test-purpose. The unbalance significantly degrades the performance of a DUT. Furthermore, the analytically derived correlations used for most self-tests has a limited test accuracy, and this issue becomes more serious due to the unbalance. This is why self-test methods have rarely been attempted for differential mixed-signal circuits. The aim of this work is to accomplish a self-test technique to produce high test-accuracy for the nonlinearity of differential mixed-signal circuits in a SoC, using a regression technique.

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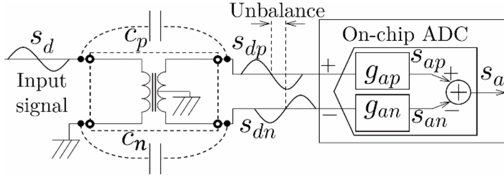


**Fig. 1.** ADC's performance degraded by unbalance.

## II. LIMITED ACCURACY ON DIFFERENTIAL CIRCUIT TESTING

It is necessary to discuss the unbalance effects on differential mixed-signal circuit, because the signature used for this work is generated by the unbalance for test purpose. This motivation has been discussed in the previous work [3] as well. Because instruments of an ATE, which support differential analog I/O interfaces, are exorbitant in general, low-cost test approaches need to use network devices (e.g., transformer, differential amplifier, and more) to facilitate conversion between a differential pair and a single-ended signal. As shown in Fig. 1, a single-ended input signal, $s_d(t) = 2cos(\omega_0 t)$ is applied to a differential ADC (i.e., one of mixed-signal DUT examples), in order to test its nonlinearity. To convert the single-ended input terminal to a differential pair of an ADC input, a radio-frequency (RF) transformer with a one-to-one winding ratio is commonly used as a network device. However, most of actual network devices have a variation from an ideal phase difference (i.e., $180^\circ$) between $s_{dp}$ and $s_{dn}$, which is called *unbalance*. This is because each of parasitic capacitances $c_p$ and $c_n$ exhibits a different time constant in general (i.e., $c_p \neq c_n$), and this difference causes the time delay between $s_{dp}(t)$ and $s_{dn}(t)$, resulting in the unbalance, $\vartheta$. Thus, $s_{dp}(t) = cos(\omega_0 t)$, and $s_{dn}(t) = -cos(\omega_0 t + \vartheta)$. A magnitude gain from a transformer is assumed as a unity, and the harmonic distortion of a DUT is considered up to the third order, for simplicity. Then, $s_{dp}(t)$ and $s_{dn}(t)$ are fed to the positive and negative transfer functions, $g_{ap}(t)$ and $g_{an}(t)$ modeled with a Taylor expansion [5], respectively. Their outputs are

$$\begin{cases} s_{ap}(t) = \varsigma_1 s_{dp}(t) + \varsigma_2 s_{dp}^2(t) + \varsigma_3 s_{dp}^3(t) \\ s_{an}(t) = \varsigma_1 s_{dn}(t) + \varsigma_2 s_{dn}^2(t) + \varsigma_3 s_{dn}^3(t) \end{cases} \tag{1}$$

where $\varsigma_i$ is the i-th harmonic coefficient of an ADC. An ADC output $s_a(t)$ ($= s_{ap}(t) - s_{an}(t)$) is then obtained as

$$s_a(t) = \bar{\varsigma}_1 l_1 / 4cos(\omega_0 t) + \bar{\varsigma}_2 l_2 / 2sin(2\omega_0 t) + \bar{\varsigma}_3 l_3 / 4cos(3\omega_0 t) \tag{2}$$

where $\bar{\varsigma}_1 = 4\sqrt{2}\varsigma_1 + 3\sqrt{2}\varsigma_3$, $\bar{\varsigma}_2 = \sqrt{2}\varsigma_2$, $\bar{\varsigma}_3 = \sqrt{2}\varsigma_3$, $l_1 = \sqrt{1 + cos(\vartheta)}$, $l_2 = \sqrt{1 - cos(2\vartheta)}$, and $l_3 = \sqrt{1 + cos(3\vartheta)}$. The nonlinearity can be evaluated with the total-harmonic-distortion (THD) or $\xi$ from (2) as

$$\xi = \left(4\bar{\varsigma}_2^2 l_2^2 + \bar{\varsigma}_3^2 l_3^2\right) / \left(\bar{\varsigma}_1^2 l_1^2\right). \tag{3}$$

Thus, the harmonic performance is degraded by the unbalance [4].

## III. PROPOSED SELF-TEST TECHNIQUE

Test accuracy of low-cost testing for differential mixed-signal circuits is affected by two major causes: the unbalance (discussed previously) and the prediction model with low accuracy (discussed as follows). Fig. 2(a) illustrates the two ways to predict the specification of DUTs: one with $f_{pc}$ and the other with $f_{ps}$ and $f_{sc}$. $f_{pc}$ represents the conventional prediction model which is *analytically* derived from *process variation* to *specification*, as in most self-test approaches [6, 7]. However, this model has a limited accuracy, because the precise and detailed behaviors of the nonlinearity cannot be described by analytically deriving in low-order equations, along with assumptions and approximations. This low accuracy issue by *analytically derived model* should be made more severe by the errors from the unbalance which is discussed previously.

The proposed self-test approach overcomes those two causes by precisely predicting the specifications of differential mixed-signal circuits employed in a SoC

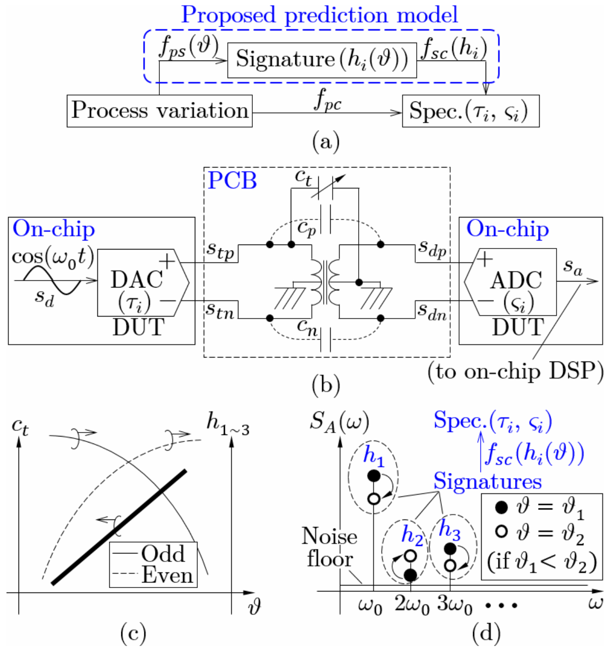


**Fig. 2.** (a) Proposed prediction model, (b) Test configuration of the previous work [3], (c) Correlation between $c_t$, $\vartheta$, and $h_{1\text{-}3}$, (d) Relation $f_{sc}$ between efficient signatures and specifications.

using an accurate prediction model for high-order nonlinearities of DUTs. The model is built based on the efficient signatures from the unbalance. This work is an extended work of the previous work [3] to employ the loopback test configuration where an input of a DUT (e.g., DAC) is connected to an output of another DUT (e.g., ADC) as shown in Fig. 2(b). This brings some benefits, e.g., no need for additional equipment to source/capture signals, cost-effective test, and more. A spectrally pure sinusoidal signal $s_d(t)$ is applied to a DAC, and its outputs $s_{tp/tn}(t)$ are unbalanced by parasitic capacitances $c_{p/n}$ of an RF transformer with center taps, as in Fig. 1. The capacitance $c_t$ set on a variable capacitor intensifies the capacitive difference between $c_p$ and $c_n$, resulting higher unbalance $\vartheta$, as shown in a thick line [4] of Fig. 2(c). The pairs of $c_t$ and $\vartheta$ are measured once with network analyzer, before production testing. In addition, as discussed in (2), higher $\vartheta$ decreases the odd-order (e.g., $h_{1,3}$) and it increases the even-order (e.g., $h_2$) harmonic coefficients of $S_A(\omega)$, thereby $h_i$ as a function of $\vartheta$, i.e., $h_i(\vartheta)$, where $S_A(\omega)$ represents the spectral expression of $s_a(t)$. Fig. 2(c) summarizes the relation among $c_t$, $\vartheta$, and $h_i$. As a result, $c_t$ directly introduces the change in $h_i$. Thus, an RF transformer with a variable capacitor will be called *weighting circuitry* in this paper. Then, as shown in Fig. 2(b), the unbalanced $s_{dp/dn}(t)$ are applied to an ADC to produce the loopback response, $s_a(t)$. Using this configuration, the proposed prediction model (i.e., $f_{ps}$ and $f_{sc}$ of Fig. 2(a)) is built based on the efficient signatures $h_i$. This model can be accurately and easily derived, compared to $f_{pc}$, because accurate signatures $h_i$ can be simply obtained from the loopback measurements, instead of analytically deriving $f_{ps}$, and also they are highly correlated with process variation of DUTs. Then, once only $f_{sc}$ is derived, the $i$-th harmonic coefficients of individual DAC and ADC (i.e., $\tau_i$ and $\varsigma_i$, respectively) can be readily identified, using the obtained $h_i$. $f_{sc}$ with high-order nonlinear expansions can be precisely derived with the statistical nonlinear regression modeling [2]. To obtain $f_{sc}$ from the regression process, the training process is first performed using two different sets of $h_i$ ($i = 1,2,...,n$) (i.e., $2n$ input data) and two sets of the corresponding specifications $\tau_i$ and $\varsigma_i$ ($i = 1,2,...,n$) (i.e., $2n$ output data). Because $n$ data (i.e., one set of $h_i$) are obtained from one loopback response measurement, two sets of the loopback measurements are performed, by sequentially setting two different values on $c_t$, in order to measure two different sets of $h_i$. Thus, the loopback responses are measured twice for the training process. The coherent sampling is needed for this work. In addition, those specifications for the training process are separately identified using an external test instrument, prior to the training process. In production testing or validation process, two sets of $h_i$ are simply captured and plugged into the obtained $f_{sc}$ to readily predict $\hat{\tau}_i$ and $\hat{\varsigma}_i$.

The following simplified quantitative derivation explains how the signature $h_i$ is strongly correlated

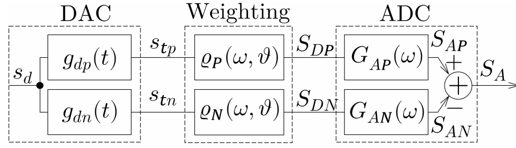


**Fig. 3.** Quantitative model of configuration shown in Fig. 2(b).

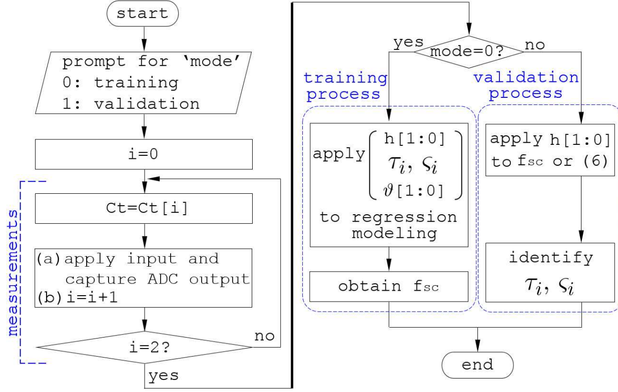


**Fig. 4.** Test procedure for the proposed method.

with the process variation, and $\tau_i$ and $\varsigma_i$. Fig. 3 represents the quantitative model of the test configuration shown in Fig. 2(b). $s_d(t)=cos(\omega_0 t)$ is applied to a DAC, and its differential outputs $s_{tp/tn}(t)$ are fed into an ADC input through the weighting circuitry.

$$\begin{cases} s_{tp}(t)=g_{dp}(s_d(t))=\overline{\tau}_1\cos(\omega_0 t)+\overline{\tau}_2\cos^2(\omega_0 t) \\ S_{TP}(\omega)=\pi(\tau_1\delta(\omega-\omega_0)+\tau_2\delta(\omega-2\omega_0)+\tau_3\delta(\omega-3\omega_0)) \end{cases} \tag{4}$$

where $s_{tp}(t)$ and $S_{TP}(\omega)$ are the DAC outputs in time/spectral-domains, respectively, and $s_{tn}(t)=-s_{tp}(t)$ and $S_{TN}(\omega)=S_{TP}(\omega)$. In addition, $\tau_1=\overline{\tau}_1+3\overline{\tau}_3/4$, $\tau_2=\overline{\tau}_2/2$, and $\tau_3=\overline{\tau}_3/4$. Then, the spectral input and output signals of an ADC, $S_{DP/DN}(\omega)$ and $S_{AP/AN}(\omega)$, respectively, are as

$$\begin{cases} S_{DP}(\omega)=\sum_{i=1}^{3}\pi\varrho_P(\omega_0,\vartheta)\tau_i\delta(\omega-i\omega_0) \\ S_{DN}(\omega)=\sum_{i=1}^{3}\pi\varrho_N(\omega_0,\vartheta)\tau_i\delta(\omega-i\omega_0) \end{cases}$$
$$\begin{cases} S_{AP}(\omega)=\sum_{i=1}^{3}(2\pi)^{1-i}\varsigma_i(S_{DP}(\omega))^{*(i-1)} \\ S_{AN}(\omega)=\sum_{i=1}^{3}(2\pi)^{1-i}\varsigma_i(S_{DN}(\omega))^{*(i-1)} \end{cases} \tag{5}$$

where $\varrho_{P/N}$ indicate the spectral transfer functions of the positive/negative channels for the weighting circuits. In addition, $*i$ indicates the $i$-fold iteration of the convolution with itself. The harmonic components of $S_A(\omega)$ $(=S_{AP}(\omega)+S_{AN}(\omega))$ can be obtained as

$$\begin{cases} S_A(\omega_0)=\sum_{i=1}^{3}\rho(i)(S_{DP}(\omega_0)^{*(i-1)}+S_{DN}(\omega_0)^{*(i-1)}) \\ S_A(2\omega_0)=\sum_{i=1}^{3}\rho(i)(S_{DP}(2\omega_0)^{*(i-1)}+S_{DN}(2\omega_0)^{*(i-1)}) \\ S_A(3\omega_0)=\sum_{i=1}^{3}\rho(i)(S_{DP}(3\omega_0)^{*(i-1)}+S_{DN}(3\omega_0)^{*(i-1)}) \end{cases} \tag{6}$$

where $\rho(i)=(2\pi)^{1-i}\varsigma_i$. Eq. (6) shows the strong correlation among the efficient signatures, the process variation, and $\tau_i$ and $\varsigma_i$, as depicted in Fig. 2(a).

Fig. 4 shows the proposed test procedure in more detail for better understanding. Two sequential processes are conducted in on-chip digital core: the training process first and the validation processes later. $f_{sc}$ is derived in the training process, and production testing is conducted using the obtained $f_{sc}$ in the validation process. The training process mode starts by setting `mode=0`. For each process up-front, the two measurements indicated in a dotted line are performed as discussed earlier. The first measurements (i.e., `i=0`) are conducted by applying a sinusoidal input to a training set of DACs, by setting $c_t$ on a predefined capacitance of `Ct[0]` (or its corresponding $\vartheta$ `[0]`), and then a set of harmonics `h[0]` are measured from a training set of ADCs. For the second measurements (`i=1`), the same measurements are then iterated to obtain a different harmonic set (`h[1]`) introduced by setting $c_t$ on a different capacitance `Ct[1]` (or $\vartheta$ `[1]`), where a training set represents a set of DUTs, which is only used to build $f_{sc}$, and also $\tau_i$ and $\varsigma_i$ of each training set are measured using an external test instrument for the training process, as discussed earlier; this process is omitted in Fig. 4 for simplicity. After the two measurements, the obtained `h[1:0]`, $\tau_i$ and $\varsigma_i$, and the used $\vartheta$ `[1:0]` are applied to the regression process, as depicted in `training process` of Fig. 4. Then $f_{sc}$ for $\tau_i$ and $\varsigma_i$ is generated as shown in (7).

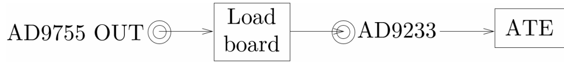


**Fig. 5.** Hardware measurement setup.

$$\begin{cases}\hat{\tau}_1 = f_{sc,\tau_1}(\vartheta[1:0], h[1:0]) \\ \hat{\tau}_2 = f_{sc,\tau_2}(\vartheta[1:0], h[1:0]) \\ \hat{\tau}_3 = f_{sc,\tau_3}(\vartheta[1:0], h[1:0]) \\ \cdots \end{cases} \begin{cases}\hat{\varsigma}_1 = f_{sc,\varsigma_1}(\vartheta[1:0], h[1:0]) \\ \hat{\varsigma}_2 = f_{sc,\varsigma_2}(\vartheta[1:0], h[1:0]) \\ \hat{\varsigma}_3 = f_{sc,\varsigma_3}(\vartheta[1:0], h[1:0]) \\ \cdots \end{cases} \quad (7)$$

where $f_{sc,\tau_i}$ and $f_{sc,\varsigma_i}$ indicate the obtained correlation model $f_{sc}$ to calculate $\hat{\tau}_i$ and $\hat{\varsigma}_i$, respectively. This training process is performed only once, prior to the production test (i.e., validation process). Similarly, the validation process mode starts by separately starting the flow chart with `mode=1`, and the same measurement procedure is performed as in the training process, but with a validation set of DACs and ADCs. A validation set represents a number of DAC/ADC units to be actually tested. Then, the obtained `h[1:0]` are applied for (7) to readily identify $\tau_i$ and $\varsigma_i$ of the validation sets, as shown in `validation process` of Fig. 4. Finally, the total-harmonic-distortions (THD) of individual DACs and ADCs are calculated with the obtained $\hat{\tau}_i$ and $\hat{\varsigma}_i$.

## IV. Hardware Experiment Results

To validate the performance of the proposed method, the hardware measurements have been conducted with commercial DACs (AD9755) and ADCs (AD9233) from Analog Devices, as shown in Fig. 5. The training process was first conducted. A 100 MHz clock signal is fed to the DAC and ADC clock inputs by HP 8644B. A 20.734 MHz sinusoidal signal was applied to the DAC input in the coherent sampling. The DAC outputs were then applied to the load board employing the weighting circuitry ($c_t$ measured including $c_{p/n}$). The unbalanced signals from the weighting circuitry were then sent to the buffers of an ATE, through the ADC. The DAC and ADC were synchronized with the ATE for the accurate measurements. The measurements were performed twice by sequentially setting unbalances (i.e., $\vartheta = 0^\circ$, $18^\circ$) on the variable capacitor. Finally, the postprocessing produced $f_{sc}$. Then, the validation process was performed by conducting the same measurements with the validation set. The proposed postprocessing discussed earlier was performed in the workstation of the ATE to predict the harmonic coefficients of the DACs and the ADCs. Total 50 units of ADCs were used for the hardware measurements: 20 units for training set, and the rest, 30 units for validation set. The reference results of the identical DUTs were obtained using differential instruments of an ATE. Fig. 6 compares the THD results of the proposed method with the obtained reference results. In addition, Table 1 summarizes the results of Fig. 6, comparing with those of the previous self-test methods [6, 7]. The means and the standard deviations of the prediction errors were less than 1.0 dB, which represents higher test accuracy than those of the previous methods.

**Table 1.** Prediction errors of THD in dB

| Proposed method | | | | [6] | | [7] | |
|---|---|---|---|---|---|---|---|
| DAC | | ADC | | DAC | | ADC | |
| mean | std. | mean | std. | mean | std. | mean | std. |
| 0.53 | 0.35 | 0.27 | 0.23 | 1.10 | n/a | 0.4 | n/a |

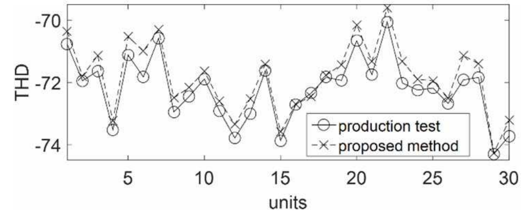


**Fig. 6.** THD results (dB) of ADCs by the proposed method.

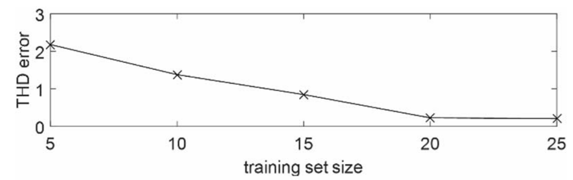


**Fig. 7.** THD prediction error (dB) depending on training set size.

### 1. Dependency of Training Set Size

It has been evaluated how much the training set size impacts on the prediction accuracy of the proposed method. In the training process, several sets of the correlation functions were individually generated, by using different size of the training set. In the validation process, each obtained set of functions has been sequentially used to predict the THD of the identical validation set. The THD prediction accuracy raised, as

the training set size was increased, as shown in Fig. 7, because the more training set size, the higher correlation between harmonics in the training/validation sets. In addition, the THD error was saturated from the size of 20, due to the limitations on the correlation enhancement.

## V. CONCLUSIONS AND FUTURE WORK

In this paper, we proposed an efficient test method to accurately predict the specifications of differential mixed-signal circuits in a SoC, based on the regression scheme. The hardware measurement results showed low prediction error rate of THD as less than 1.0 dB for this work, which represents higher test accuracy compared to previous works. Thus, this work has overcome the serious test issue of differential mixed-signal circuits, that the low accuracy of analytically derived model is much lower by the errors from the unbalance. The proposed method was therefore validated to be a cost-effective test methodology which can be readily used for practical production testing. Our future efforts will be made to expand this test scheme to support the multitone and noise testing.

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