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Analysis of Stability and Dynamic Behaviour of Ultra Lift Luo Converter

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Abstract – Ultra Lift Luo Converter (ULC) gained considerable research interest in recent years. The stability analysis of voltage mode and peak current mode controlled ULC in continuous conduction mode is analyzed in this paper. The Eigen value theory is used for the stability analysis of voltage mode controlled ULC. Then to characterize the dynamics of inner current loop, the expressions of closed loop transfer function and loop gain are determined. An algorithm has been developed to analyze the stability of the peak current mode controlled ULC. The theoretical results are correlated with the simulation results obtained using PSIM 9.1(SMARTCTRL 1.0) software. Finally it is proposed to fabricate a prototype and validate the performance by suitable experimental setup.

Keywords: Luo converter, Voltage mode, Peak current mode, Inner current loop control, On-slope inductor current, Critical compensation slope, Small signal averaged model

1. Introduction

Voltage Lift (VL) technique is used in Luo converters for producing an output voltage increasing either in arithmetic or geometric progression at each stage. VL technique is usually adopted in periodical switching circuit and delivers high output voltage with enhanced circuit characteristics. In Luo converters, a capacitor is charged and positioned on top to yield a high output voltage. The self- lift, re-lift, triple-lift and quadruple-lift converters can be developed from elementary topology. The Ultra lift Luo Converter provides higher output voltage gain than all other Luo converters is used in this work [1, 2]. The literature survey signifies that the study of the stability analysis for Ultra Lift Luo converter has not been revealed so far. This paper brings out a study on the stability analysis and dynamic performance of ULC. This analysis has been carried out separately for the voltage mode and peak current mode controller using different methods. The stability of the linear dynamic system is usually evaluated using the Eigen value theory [3-5]. Peak current mode control with better line regulation, good transient response, over current protection is employed for converter regulation [6, 7]. For the relative stability analysis of peak current mode control, perturbation theory, sample and hold theory and modified pade approximation method are used and the expressions for closed loop transfer function and loop gain are derived. The analysis of stability explains the system behaviour, when it is subjected to perturbation. The sample and hold modelling is used for modeling the inner current loop of the controller by considering the inner current loop dynamics and discrete nature of the loop. The convergence value of the closed loop transfer function is acquired using modified pade approximation method [8-10].

The boundary region for the stable operation of the system is obtained by deriving the expressions for on-slope inductor current, critical compensation slope operating at maximum duty cycle and the limiting value of duty cycle of the converter. The expressions for control current for the inner loop of the controller with and without slope compensation are derived for the design of the outer voltage loop [9-11]. For the appropriate analysis of the power stage of the system, small signal averaged model is applied and various power stage transfer functions are derived [12-16].

This paper deals with the stability analysis for the voltage mode controlled ULC using the Eigen value theory. Then the study of the stability analysis and dynamic behaviour of peak current mode controlled ULC is carried out using the perturbation theory and the controller is designed using PSIM 9.1 SMARTCTRL 1.0 software. The stability of the system is analysed from the solution map obtained in SMARTCTRL 1.0. As this is the multi loop controller, each loop must be stable for proper operation of the controller and it is verified using bode plots.

2. Ultra Lift Luo Converter

The circuit diagram of Ultra Lift Luo Converter is shown in Fig. 1. It consists of a power switch 'S', three freewheeling diodes D_1, D_2, D_3, two inductors L_1 and L_2, two capacitors C_1 and C_2 and the load resistor R. In the description of converter operation, it is assumed that, ULC operates in CCM and the circuit is divided into two states

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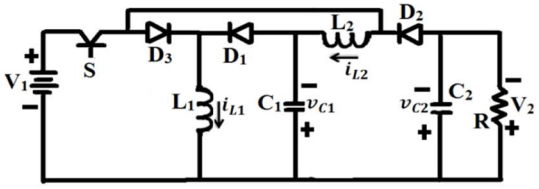

Fig. 1. Ultra Lift Luo Converter [2]

namely, Switch-ON and Switch-OFF. During switch ON, D_3 is forward biased, so that the inductor (L_1) current, I_{L1}, starts increasing with slope V_1/L_1 and I_{L2} starts increasing with slope $(V_1\text{-}V_3)/L_2$.

In this interval, capacitor C_1 is charged to $\left[\left(\frac{k}{1-k}\right)V_1\right]$ voltage level to lift the output voltage higher. Now when the switch is turned OFF, D_3 becomes reversed biased. D_1 and D_2 become forward biased and I_{L1} starts decreasing and C_1 discharges. I_{L1} decreases with slope - V_3/L_1 and I_{L2} decreases with slope $-(V_2\text{-}V_3)/L_2$. The gain of the converter is given as,

$$\frac{V_2}{V_1} = \frac{K(2-K)}{(1-K)^2} \tag{1}$$

where,

V_1 - Input voltage (V)
V_2 - Output voltage (V)
V_3 - Nodal voltage (V)
K - Duty cycle of the converter

3. Stability Analysis of Voltage Mode Controlled ULC by Eigen Value Theory

Fig. 2 shows the basic voltage mode controller used in the Ultra lift Luo converter. The controller has an alterable clock to set the frequency, a voltage error amplifier, a ramp signal generator and a comparator to compare the output error signal with the ramp signal. The signal from the comparator output is used for driving the power switch. The on-time duration is calculated using the difference between the reset time of the ramp signal generator and the time at which the error voltage intersects with the positive –going ramp signal. The dynamics of the feedback controller is determined through use of the error amplifier components such as R_{fe} and C_{fe}.

It is considered that the state variables are inductor (L_1) current i_{L1}, inductor (L_2) current i_{L2}, capacitor (C_1) voltage v_{C1}, output voltage v_0 and the control voltage in the control block V_{ctrl}. The averaged state equations are given in Eqn. (2), Eqn. (3), Eqn. (4), Eqn. (5) and Eqn. (6).

$$\frac{di_{L1}}{dt} = \frac{(1-K)}{L_1}v_{C1} + \frac{K}{L_1}v_1 \tag{2}$$

$$\frac{di_{L2}}{dt} = \frac{(2K-1)}{L_2}v_{C1} + \frac{1-K}{L_2}v_2 + \frac{K}{L_2}v_1 \tag{3}$$

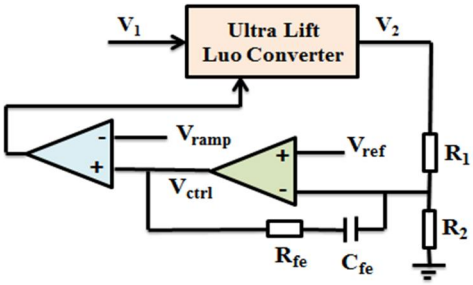

Fig. 2. Voltage mode controlled ULC

$$\frac{dv_{C1}}{dt} = \frac{(2K-1)}{C_1}i_{L1} + \frac{1-K}{C_1}i_{L2} + \frac{K}{R_iC_1}v_1 \tag{4}$$

$$\frac{dv_2}{dt} = \frac{(K-1)}{C_2}i_{L2} - \frac{1}{R_0C_2}v_2 \tag{5}$$

$$\frac{dv_{ctrl}}{dt} = -v_2\left(\frac{B}{R_{fe}C_{fe}} + \frac{1}{R_0C_2}\right) + v_{ref}\left(\frac{B}{R_{fe}C_{fe}}\left(1+\frac{R_1}{R_2}\right)\right) - \frac{i_{L2}}{C_2}(K-1)(B) \tag{6}$$

In this system, the proportional coefficient, $B = \frac{R_{fe}}{R_1}$ affects the stability of the circuit. The stability of the linear dynamic system is evaluated using the Eigen value theory. The Jacobian matrix is substantial for the stability analysis of the dynamic systems which is described by the state equations. The system behaviour near the equilibrium point is related to Eigen values of the Jacobian matrix. In order to obtain the equilibrium point of the Jacobian matrix, the derivative of the state variables must be zero at steady state condition. Eqn. (7) gives the value of the equilibrium point (N_o) which is determined in the steady state by making the derivative of the state variables to be zero.

$$N_o = \begin{bmatrix} I_{L1} \\ I_{L2} \\ V_{C1} \\ V_{C2} \\ V_{Ctrl} \end{bmatrix} = \begin{bmatrix} \frac{V_1}{1-2K}\left[\frac{K}{R_i} - \frac{(3K-2)}{R_0(K-1)^2}\right] \\ V_1\left[\frac{K(3K-2)}{(K-1)^3R_0}\right] \\ V_1\left[\frac{K}{K-1}\right] \\ V_1\left[\frac{K(3K-2)}{(K-1)^2}\right] \\ V_{Li} + K(V_{Hi} - V_{Li}) \end{bmatrix} \tag{7}$$

Using Eqn. (7), the Jacobian matrix at the equilibrium point ($J(N_o)$) is derived in Eqn. (8) and it is used for stability analysis of the system.

$$(N_o) = \begin{bmatrix} 0 & 0 & \frac{(1-K)}{L_1} & 0 & \frac{v_1}{L_1(V_{Hi}-V_{Li})} \\ 0 & 0 & \frac{(2K-1)}{L_2} & \frac{1-K}{L_2} & \frac{v_1}{L_2(V_{Hi}-V_{Li})} \\ \frac{(2K-1)}{C_1} & \frac{1-K}{C_1} & 0 & 0 & \frac{-v_1}{R_iC_1(V_{Hi}-V_{Li})} \\ 0 & \frac{(K-1)}{C_2} & 0 & \frac{-1}{R_0C_2} & 0 \\ 0 & \frac{(1-K)B}{C_2} & 0 & \frac{-B}{R_{fe}C_{fe}} - \frac{1}{R_0C_2} & 0 \end{bmatrix} \tag{8}$$

Table 1. Eigen values of Jacobian matrix for various 'B' values

B	Eigenvalues for different 'B' values	Stability
0.02	1.0e+04 * (-1.4261 ± 2.5240i, -2.5211 + 0.0000i, -0.3317 + 0.0000i,-0.0004 + 0.0000i)	Stable (all negative real parts)
0.025	1.0e+04 * (-1.5450 ± 2.7024i,-2.7411 + 0.0000i, -0.3495 + 0.0000i, -0.0004 + 0.0000i)	Stable (all negative real parts)
0.03	1.0e+04 * (- 1.6472 ± 2.8592i, -2.9338 +0.0000i, -0.3613 + 0.0000i, -0.0004 + 0.0000i)	Stable (all negative real parts)
0.035	1.0e+04 * (-1.7376 ± 2.9998i, -3.1063 + 0.0000i, -0.3695 + 0.0000i, -0.0004 + 0.0000i)	Stable (all negative real parts)
0.04	1.0e+04 * (-1.8190 ±3.1280i, -3.2629 + 0.0000i, -0.3757 + 0.0000i,-0.0004 + 0.0000i)	Stable (all negative real parts)
0.047	1.0e+04 * (-1.9076±3.2687i,3.4345 + 0.0000i, -0.3813 + 0.0000i, -0.0004 + 0.0000i)	Unstable (one positive real parts)

In the above equation, V_{Hi} and V_{Li} are high and low boundary value of ramp signal. Table 1 shows the Eigen values of the Jacobian matrix $J(N_o)$ for various values of 'B'. The system is stable when all the Eigen values have negative real parts and is unstable when any one Eigen value has a positive real part. From Table 1 it is inferred that, real parts of the Eigen values increase with increase in 'B' values and when B reaches to 0.047, the system loses its stability property.

4. Stability analysis of Peak current mode controlled ULC

The peak current mode controller with inner current loop and outer voltage loop is shown in Fig. 3.

In this part of the paper, the study of stability analysis is focussed on the input inductor current that is controlled by the inner current loop of the controller. An algorithm is developed for PCM controlled ULC and the corresponding flowchart is shown in Fig. 4. The analysis comprises four aspects, namely,

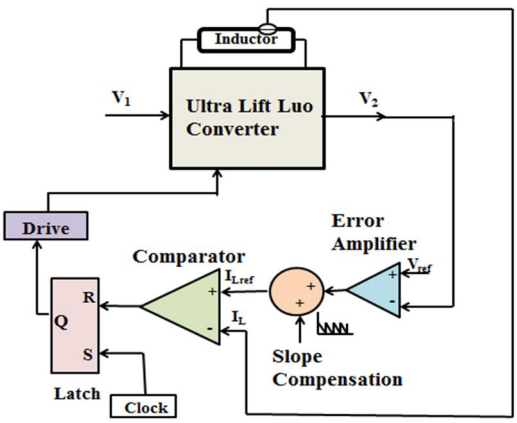

Fig. 3. Peak current mode controlled ULC

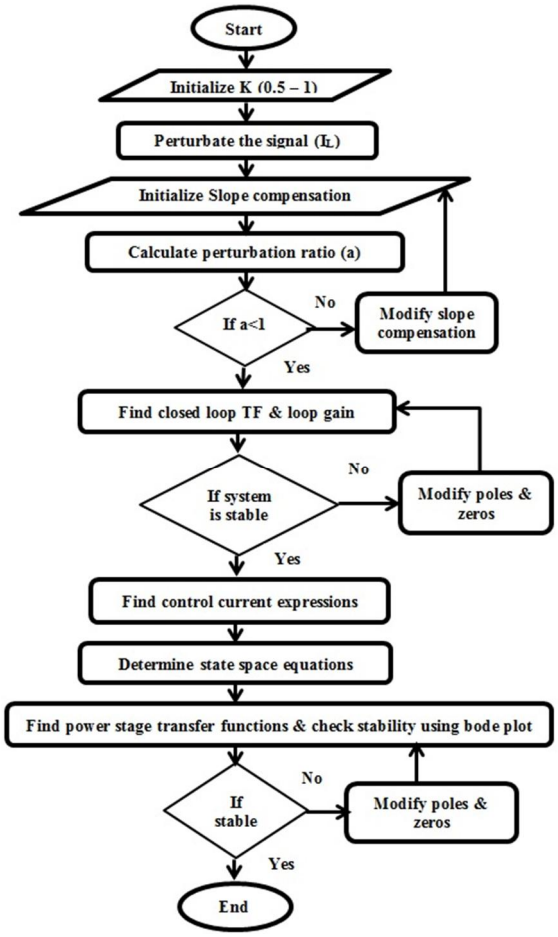

Fig. 4. Flowchart for the stability analysis of peak current mode controlled converter

1. Dynamics of the inner current loop of the controller
2. Margin of stability
3. Expressions of the control current
4. Dynamic behaviour of the controller

4.1 Dynamics of the inner current loop of the controller

In a peak current mode controller, there exists the instability problem due to sub harmonic oscillations when the duty cycle exceeds 0.5. These oscillations are avoided by slope compensation. In this part of the analysis, the perturbation theory is used for the stability analysis of the inner current loop from which perturbation ratio (a) is obtained as a function of slope compensation (M_3) and duty cycle as given in Eqn. (9).

$$a = \frac{\frac{K}{1-K} - \frac{M_3}{M_1}}{1+\frac{M_3}{M_1}} \tag{9}$$

where, M_1 is On slope input inductor current. In order to study the dynamics of the inner loop, the control current is sampled. The sampled control current is transformed to small signal inductor current. By using Sample and Hold

theory, inductor current is held for a switching period till the next sampling instant and finally it is modelled in the Z-domain.

The discrete closed loop control voltage to inductor voltage transfer function is given in Eqn. (10).

$$H_{icl}(z) = \frac{i_l(z)}{v_C(z)} = \frac{(1+a)}{R_s}\left(\frac{z}{z+a}\right) \quad (10)$$

The transfer function of the inner current loop of the controller using modified pade approximation is given in Eqn. (11).

$$H_{icl}(s) = \frac{1}{R_s}\left(\frac{{\omega_h}^2}{s^2+2s\varepsilon_h\omega_h+{\omega_h}^2}\right) \quad (11)$$

Where, ω_h is angular frequency and given as $\omega_h = \pi f_s$ and ε_h is damping coefficient and given as

$$\varepsilon_h = \frac{\pi}{4}\left(\frac{1-a}{1+a}\right) \quad (12)$$

The inner current loop gain is essential for the relative stability analysis. The loop gain of the inner current loop of the converter is given in Eqn. (13) which is a function of perturbation ratio and switching frequency.

$$T_i(s) = \frac{{\omega_h}^2}{s(s+\omega_{sh})} = \frac{\pi^2 {f_s}^2}{s\left(s+\frac{\pi^2}{2}\left(\frac{1-a}{1+a}\right)f_s\right)} \quad (13)$$

Relative stability is measured in terms of the phase margin and the relation between phase margin and perturbation ratio is given in Eqn. (14). Usually the value of perturbation ratio must be small for achieving a feasible margin of stability in terms of phase margin.

$$a = \frac{\sqrt[4]{1+tan^2PM}-\frac{2}{\pi}tanPM}{\sqrt[4]{1+tan^2PM}+\frac{2}{\pi}tanPM} \quad (14)$$

4.2 Margin of stability

To decide the boundary regions for the stable operation of the converter, on slope inductor current (M_{1min}), critical value of compensation slope (M_{3cr}), minimum compensation slope (M_{3min}) with respect to maximum duty cycle must be computed. The expressions for (M_{1min}), (M_{3cr}), (M_{3min}) are determined in Eqn. (15), Eqn. (16) and Eqn. (17) respectively.

$$M_{1min} = \frac{(1-K_{max})}{K_{max}(2-K_{max})} \times \frac{V_2}{L_1} \quad (15)$$

$$M_{3cr} = \frac{V_2}{L_1}\frac{(K_{max}-0.5)}{K_{max}(2-K_{max})} \quad (16)$$

$$M_{3min} = \frac{V_2}{L_1}\frac{(K_{max}-0.5)}{K_{max}(2-K_{max})} + \frac{V_2}{\pi L_1}\left(\frac{tanPM}{K_{max}(2-K_{max})\sqrt[4]{1+tan^2PM}}\right) \quad (17)$$

Table 2. PM verses M_{3min}

PM(deg)	M_{3min} (A/ms)
30	17.81
45	22.66
60	27.42

When the input voltage is varied from 5V to 20V, the duty cycle varies between 0.693 and 0.464. M_{3min} is the function of maximum duty cycle and phase margin (PM) and also M_{3min} is greater than M_{3cr}. By rearranging Eqn. (16), the expression for critical duty cycle for the given normalized compensation can be obtained and it is given in Eqn.(27). The value of the critical duty cycle is found to be 0.73. Table 2 shows the values of M_{3min} for various PM.

At the point of maximum duty cycle, minimum compensation slope of ULC increases with the increase in phase margin as shown in Table 2.

4.3 Control current expressions

Calculation of the control current values should be done for the design of the outer voltage loop. The expressions for the control current of peak current mode controlled Ultra Lift Luo converter with slope compensation(I_{CS}) and without slope compensation(I_{CN}) are given in Eqn. (18) and Eqn. (19) respectively.

$$I_{CS} = \frac{I_2}{(1-K)^2} + \frac{V_2 K}{L_1 f_s}\left(\frac{(1-K_{max})K_{max}}{(2-K_{max})} + \frac{(K_{max}-0.5)}{K_{max}(2-K_{max})} + \left(\frac{1}{\pi}\right)\left(\frac{tanPM}{K_{max}(2-K_{max})\sqrt[4]{1+tan^2PM}}\right)\right) \quad (18)$$

$$I_{CN} = \frac{I_2}{(1-K)^2} + \frac{V_2}{2L_1 f_s}\left(\frac{1-K}{2-K}\right) \quad (19)$$

Fig. 5 shows the values of control current without slope compensation for various PM. Fig. 5 shows that control current without slope compensation is inversely proportional to the phase margin. Table 3 exhibits the variations in the control current values of slope compensation for different duty cycles and input voltages when PM=30°, PM=45°, PM=60°.

The control current values given in Table 3 are essential for the outer voltage loop design of the controller. The control current with slope compensation increases with

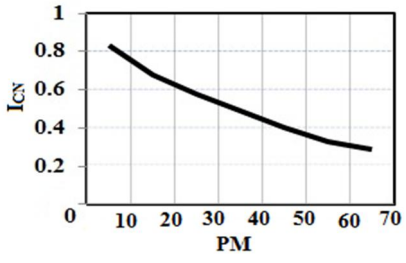

Fig. 5. I_{CN} verses PM

Table 3. Control current with slope compensation for various PM

Duty cycle	Input Voltage (V)	Control current (A) for various PM		
		30°	45°	60°
0.5	16	1.23	1.35	1.50
0.525	14	1.35	1.47	1.64
0.55	12	1.48	1.62	1.79
0.585	10	1.71	1.85	2.03
0.602	9	1.84	1.99	2.17
0.624	8	2.03	2.19	2.38
0.643	7	2.23	2.39	2.59
0.668	6	2.54	2.70	2.91
0.693	5	2.92	3.09	3.30

increase in phase margin for various duty cycles.

4.4 Dynamic behavior of the controller

This part carries an analysis of the dynamic behavior of the converter operating in continuous conduction mode in response to perturbations in the duty cycle. The small signal averaged model is used for deriving the power stage transfer functions of the peak current mode controlled Ultra Lift Luo converter. The state variables for this converter are inductor (L_1) current-x_1, inductor (L_2) current-x_2, capacitor(C_1) voltage-x_3, capacitor(C_2) voltage-x_4. The source variables are input voltage- $u_1$and duty cycle- k. The state space equations in matrix form for Ultra Lift Luo converter is given in Eqn. (20). By introducing small perturbations such as $x_1 = x_{10} + \widehat{x_1}$; $x_2 = x_{20} + \widehat{x_2}$; $x_3 = x_{30} + \widehat{x_3}$; $x_4 = x_{40} + \widehat{x_4}$; $u_1 = u_{10} + \widehat{u_1}$; $k = K + \hat{k}$, in Eqn. (20), the state space equations are rewritten and given in Eqn. (21).

For the design of the outer voltage loop of the controller, it is essential to determine the plant transfer function (TF) for the outer loop. The modulator transfer function $T_{ms}(s)$, inductor current to duty ratio transfer function $T_{pi}(s)$, control voltage to duty ratio transfer function $T_{icl}(s)$, control to output transfer function $T_{co}(s)$, output voltage to duty ratio transfer function $T_p(s)$ are given in Eqn. (22), Eqn. (23), Eqn. (24), Eqn. (25). Eqn. (26) respectively.

5. Efficiency Analysis

In ULC, output of the converter is increased in geometric progression with the reduction in losses in parasitic components and increased efficiency. By considering the equivalent series resistance across each parasitic component, the efficiency (η) of the converter is calculated from total power loss (P_{Loss}) and output power (P_o) using the relation given in Eqn. (28).

$$\eta = \frac{P_o}{P_o + P_{Loss}} \tag{28}$$

The output power is calculated from Eqn. (29)

$$P_o = \frac{{V_2}^2}{R} \tag{29}$$

The total power loss is calculated as the sum of loss across $L_1(P_{loss\_L_1})$, $L_2(P_{loss\_L_2})$, $C_1(P_{loss\_C_1})$, $C_2(P_{loss\_C_2})$ and switching loss with the assumption of negligible diode loss from the following Eqn. (30).

$$P_{loss} = P_{loss\_L_1} + P_{loss\_L_2} + P_{loss\_C_1} + P_{loss\_C_2} + P_{switch} \tag{30}$$

$$P_{loss} = {I_{L_1}}^2 R_{L_1} + {I_{L_2}}^2 R_{L_2} + {I_{C_1}}^2 R_{C_1} + {I_{C_2}}^2 R_{C_2} + [V_{DS} * I_D * f_{sw} * \left(\frac{Q_{GS}+Q_{GD}}{I_G}\right)] \tag{31}$$

In the above equations, I_{L_1}, I_{L_2}, I_{C_1}, I_{C_2} are the rms values of current through L_1, L_2, C_1, C_2 respectively. The losses are calculated by measuring the rms values of the currents for the parasitic elements. $R_{L_1}, R_{L_2}, R_{C_1}, R_{C_2}$ are the equivalent series resistance of L_1, L_2, C_1, C_2 respectively. V_{DS}, I_D, I_G are the drain source voltage, drain current, gate current of the MOSFET respectively. Q_{GS} and Q_{GD} are gate to source charge and gate to drain charge in MOSFET respectively. By substituting Eqn. (29) and Eqn. (31) in Eqn.(28), the efficiency of the converter is found to be 94%.

6. Results

The design parameters of the Ultra Lift Luo converter are given in Table 4. Using the specifications given in Table 4, the circuit is simulated in PSIM 9.1 (SMARTCTRL 1.0) software.

Fig. 6 shows the simulated results of gate pulse and inductor current waveforms of ULC for V_1=12V and K=0.55.

Table 4. Converter specifications

Input Voltage	5V to 20V
Output Voltage	-48V
L_1=L_2	1mH
C_1 = C_2	1µF
R	100Ω
Switching frequency (f_s)	100 kHz
Duty cycle (K)	0.55

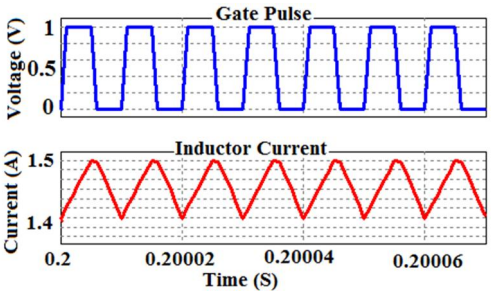

Fig. 6. Gate pulse and Inductor current waveforms of Ultra lift Luo converter

Table 5. Comparison of control current values of simulation and theoretical results

PM (deg)	Control current(A) (Simulation result)	Control current (A) (Theoretical result)
30	1.42	1.48
45	1.59	1.62
60	1.74	1.78

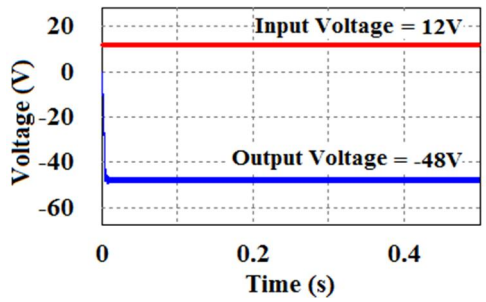

Fig. 7. Voltage waveforms of Ultra lift Luo converter

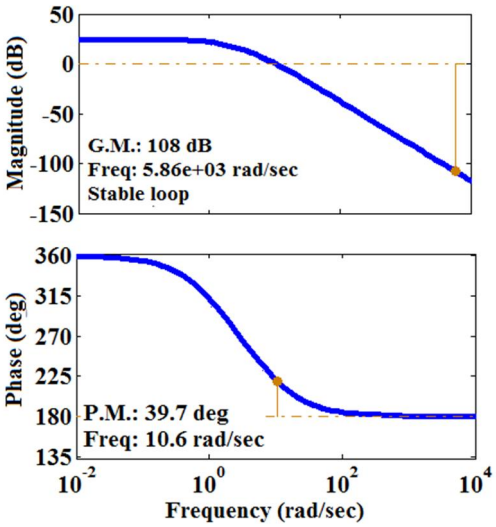

Fig. 8. Bode plot for inductor current to duty ratio transfer function

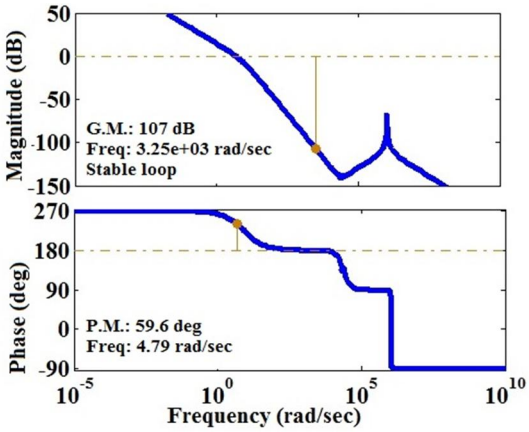

Fig. 9. Bode plot for output voltage to duty ratio transfer function

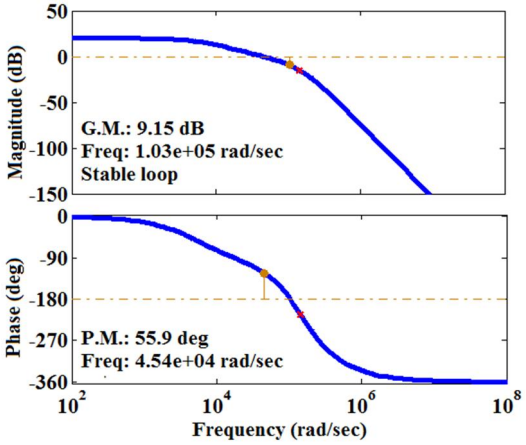

Fig. 10. Bode plot for closed loop control to inductor current transfer function

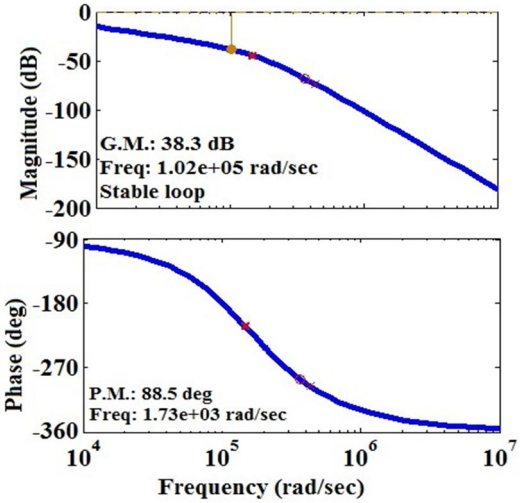

Fig. 11. Bode plot for loop gain of inner current loop transfer function

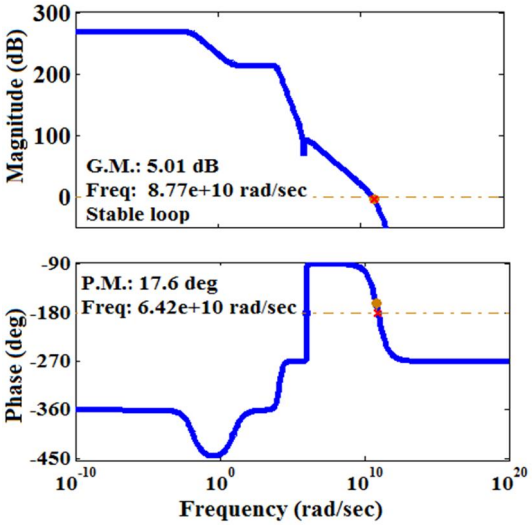

Fig. 12. Bode plot for modulator transfer function

The input and output voltage waveform of the converter is shown in Fig. 7.

Table 5 shows a comparison of the theoretical and simulation results of control current values of the controller for three phase margins.

The inference from Table 5 is that control current ranges from 1.48A to 1.78A for the specified margin of stability. The solution map of SMARTCTRL for different phase margins is shown in Fig. 18. The solution map shows bode plot and the values of the controller parameters required for the design of inner current loop and outer voltage loop. The stable operation of each loop is validated through bode plots shown in Fig. 8 to Fig. 14.

Bode plots illustrates the transfer function of each loop for input voltage = 12V and duty cycle = 0.55. Each bode plot shows that each loop is stable with both positive gain margin and phase margin. The experimental setup of ULC is shown in Fig. 15. The main elements used in the laboratory prototype are given in Table 6.

The Spartan-6 FPGA(Field Programmable Gate Array) controller is used to generate the PWM pulses for driving the MOSFET switch. Using ADC, output voltage is converted into digital signal. PWM signal is generated by comparing the square signal generated by N bit counter and the square signal that contains the duty cycle information.

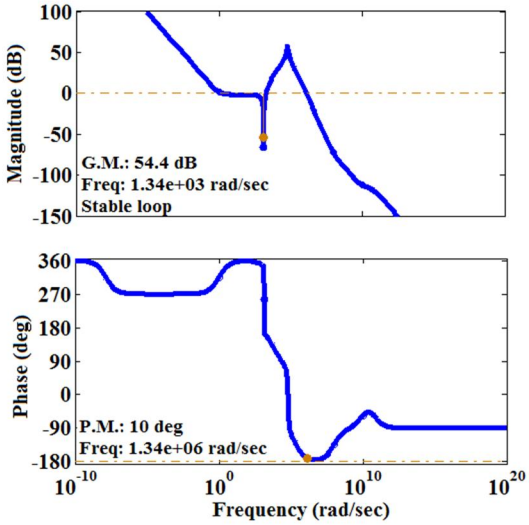

Fig. 13. Bode plot for control voltage to duty ratio transfer function

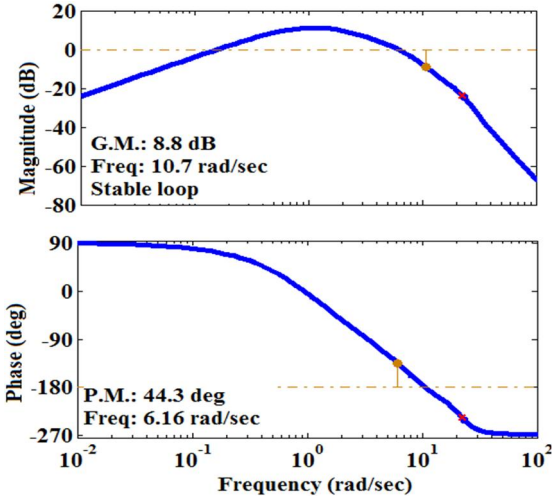

Fig. 14. Bode plot for control to output voltage transfer function

Table 6. Elements in the Prototype

Switch	MOSFET- IRF250
Diode	MUR3060
Inductor	1mH
Capacitor	1μF

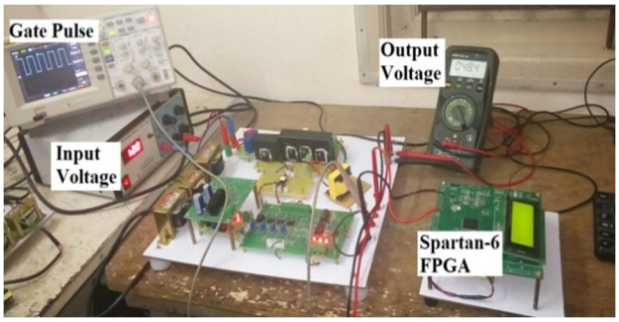

Fig. 15. Experimental set up

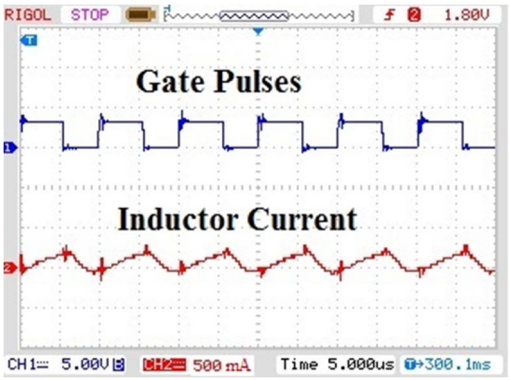

Fig. 16. Gate pulse and input inductor current waveform

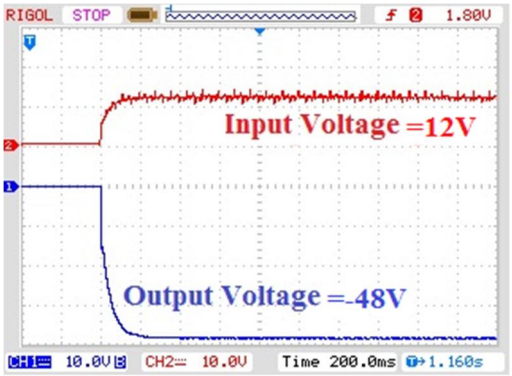

Fig. 17. Input voltage and output voltage waveform

When both the values are equal, the comparator output is set to '1' and it is used to set RS latch. The overflow signal from the counter resets RS latch. The Latch output represents the PWM signal.

The gate pulse and the inductor current waveforms for V_1 = 12V and K = 0.55 are given in Fig. 16. Fig. 16 is similar to the simulation result shown in Fig. 6.

The input and output voltage waveforms of the experimental results are given in Fig. 17 which is similar to the waveforms shown in Fig. 7.

7. Conclusion

The operating principle of ULC is explained in this work. The stability analysis of voltage mode and peak current mode PWM controlled ULC are explored. In the voltage mode control, the Eigen values of the Jacobian matrix increase linearly with increase in the proportional coefficient. It is observed that, when B reaches 0.047, the system loses its stability, as the Eigen value has a positive real part. The use of compensator components to ensure the B value does not exceed 0.046 is, therefore suggested.

In the peak current mode control, at the point of maximum duty cycle, minimum compensation slope of the converter increases as the phase margin increases and the critical value of compensation slope is less when compared to minimum compensation slope. The slope compensation control current also increases as the phase margin increases with the increase in duty cycle. The value of critical duty cycle is found to be 0.73. It is also concluded that each loop is stable with a positive phase margin and gain margin. The solution map obtained using SMARTCTRL 1.0 shows stable operation of the peak current mode controlled converter. Finally a feasible prototype is developed and the performance is validated by a suitable experimental setup. The efficiency of the converter is found to be 94%. Using the methods used in this paper, it is possible to analyse the stability of any Luo converter and to find the specific margin of stability of the system.

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APPENDIX 1

$$\begin{bmatrix}\dot{x_1}\\ \dot{x_2}\\ \dot{x_3}\\ \dot{x_4}\end{bmatrix}=\begin{bmatrix}0 & 0 & \frac{(1-k)}{L_1} & 0\\ 0 & 0 & \frac{(2k-1)}{L_2} & \frac{(1-k)}{L_2}\\ \frac{(2k-1)}{C_1} & \frac{(1-k)}{C_1} & 0 & 0\\ 0 & \frac{(k-1)}{C_2} & 0 & \frac{(-1)}{R_0C_2}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\end{bmatrix}+\begin{bmatrix}k/L_1\\ k/L_2\\ -k/R_iC_1\\ 0\end{bmatrix}[u_1] \tag{20}$$

$$\begin{bmatrix}\dot{x_1}\\ \dot{x_2}\\ \dot{x_3}\\ \dot{x_4}\end{bmatrix}=\begin{bmatrix}0 & 0 & \frac{(1-K)}{L_1} & 0\\ 0 & 0 & \frac{(2K-1)}{L_2} & \frac{(1-K)}{L_2}\\ \frac{(2K-1)}{C_1} & \frac{(1-K)}{C_1} & 0 & 0\\ 0 & \frac{(K-1)}{C_2} & 0 & \frac{(-1)}{R_0C_2}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\\ x_4\end{bmatrix}+\begin{bmatrix}K/L_1\\ K/L_2\\ -K/R_iC_1\\ 0\end{bmatrix}[u_1]+\begin{bmatrix}\frac{(u_{10}-x_{30})}{L_1}\\ \frac{(2x_{30}-x_{40}-u_{10})}{L_2}\\ \frac{(2x_{10}-x_{20}-u_{10})}{C_1}\\ \frac{x_{20}}{C_2}\end{bmatrix}[\hat{k}] \tag{21}$$

$$T_{ms}(s)=\frac{T_i(s)}{R_sT_{pi}(s)} \tag{22}$$

$$T_{pi}(s)=\frac{\begin{array}{c}\{(u_{10}-x_{30})[s^3(L_2R_0C_1C_2)+s^2(L_2C_1)+s[(R_0C_1(1-K)^2)+(R_0C_2(1-3K+2K^2))\\ +(2K^2-3K)]]\}+\{(x_{40}+u_{10}-2x_{30})[(1-K)^2)(1+sR_0C_2)]\}+\{(K\\ -1)(x_{20}+u_{10}-2x_{10})(s^2L_2R_0C_2+sL_2+R_0(1-K)^2)\}\\ -\{[R_0x_{20}(K^3-3K^2+3K-1)]\}\end{array}}{\begin{array}{c}s^4(L_1L_2R_0C_1C_2)+s^3(L_1L_2C_1)+s^2[(L_1R_0C_1(1-D)^2)+(R_0C_2(L_1+L_2)(1-3K+2K^2))]\\ +s[(L_1+L_2)(1-3K+2K^2)]+R_0(2K^4-7K^3+9K^2-5K+1)\end{array}} \tag{23}$$

$$T_{icl}(s)=\frac{T_{ms}(s)}{1+T_i(s)} \tag{24}$$

$$T_{co}(s)=T_{icl}(s)*T_p(s) \tag{25}$$

$$T_p(s)=\frac{\begin{array}{c}\{(x_{40}+u_{10}-2x_{30})[s^2(L_1R_0C_1)(1-K)+R_0(1-4K+5K^2-2K^3)]\}\\ +\{(R_0x_{20})[s(L_1+L_2)(1-3K+2K^2)+s^3(L_1L_2C_1)]\}\\ +\{R_0(2K-1)(K-1)[(2K-1)(u_{10}-x_{30})-(sL_1)(x_{20}+u_{10}-2x_{10})]\}\end{array}}{\begin{array}{c}s^4(L_1L_2R_0C_1C_2)+s^3(L_1L_2C_1)+s^2[(L_1R_0C_1(1-K)^2)+(R_0C_2(L_1+L_2)(1-3K+2K^2))]\\ +s[(L_1+L_2)(1-3K+2K^2)]+R_0(2K^4-7K^3+9K^2-5K+1)\end{array}} \tag{26}$$

$$K_{crit}=1-\frac{0.5V_2}{M_3L_1}+0.5\sqrt{\left(\frac{V_2}{M_3L_1}\right)^2+4} \tag{27}$$

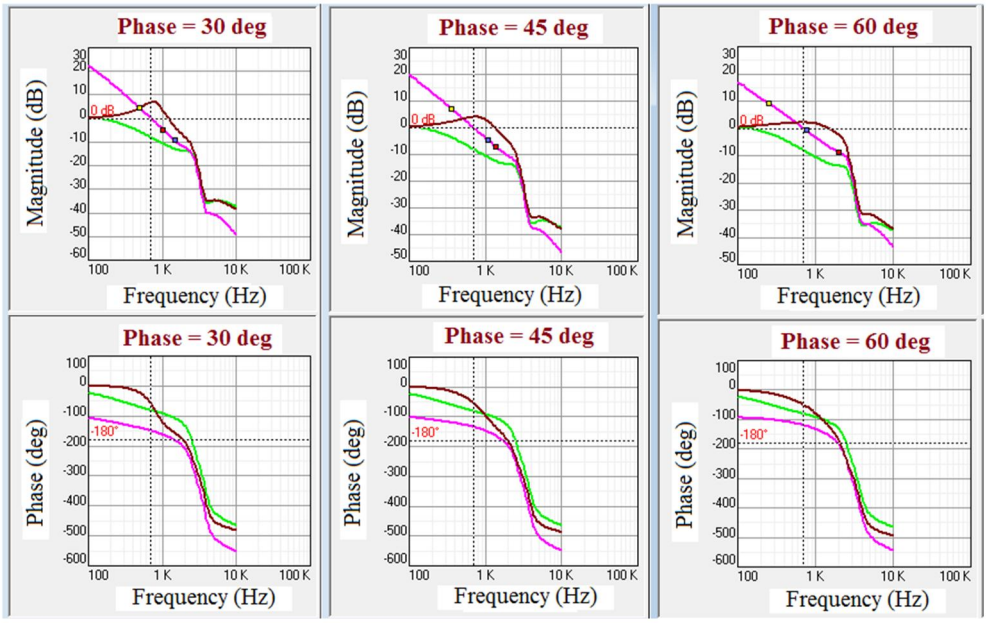

Fig. 18. Solution map waveforms for various phase margin