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넓은 출력 전압제어범위를 갖는 3레벨 단상 단일전력단 AC/DC 컨버터

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Three Level Single-Phase Single Stage AC/DC Resonant Converter With A Wide Output Operating Voltage Range

Takongmo Marius[1], Min-Ji Kim[1], Jae-Sung Oh[1], Gang-Woo Lee[1], Eun-Soo Kim†, and In-Gab Hwang[1]

Abstract

This study presents a single-phase single-stage three-level AC/DC converter with a wide controllable output voltage. The proposed AC/DC converter is designed to extend the application of e-mobility, such as electric vehicles. The single-stage converter integrates a PFC converter and a three-level DC/DC converter, operates at a fixed frequency, and provides a wide controllable output voltage (approximately 200 - 430Vdc) with high efficiencies over a wide load range. In addition, the input boost inductors operate in a discontinuous mode to improve the input power factor. The switching devices operate with ZVS, and the converter's THD is small, especially at full load. The feasibility of the proposed converter is verified by the experimental results of a 1.5 kW prototype.

Key words: Hybrid three-level DC/DC converter, LLC resonant converter, Single stage AC/DC converter, EV Charger

1. Introduction

AC/DC converters are essential converters to energize DC loads to an AC source. For high power and high voltage DC applications, single-phase AC/DC converters operating with ZVS and ZCS are required to limit switching loses. Previous designs of electric vehicle (EV) charging systems comprise of a front-end AC/DC topology such as single phase interleaved PFC converter, bridgeless PFC converter to improve the input power factor, followed by an isolated high frequency DC/DC three level resonant converter to regulate the output voltage.[1],[2] However, such systems are two separate switch mode converters and thus the overall cost and size of the AC-DC converter are increased because of additional switching devices and gate drives. In addition, a sophisticated control mechanism that includes the sensing of certain key parameters such as input currents and voltages are required. The single stage AC/DC converter was proposed to mitigate the drawbacks of the two stage topology. However, previously published single-phase, three level phase shift (TL-PS) single stage AC-DC converters face problems of hard switching especially at low loads resulting in poor efficiencies. Also, auxiliary windings were used to widen the output voltage range but it was difficult to have a controllable output voltage greater than twice the normal output voltage ($2V_o$). Moreover, the presence of the auxiliary windings increased the voltage stress on the switching devices.[3]-[7]

In this paper, a single-phase three level single stage converter that mitigates the aforementioned drawbacks of previously published single stage converters is presented. It is designed to extend the

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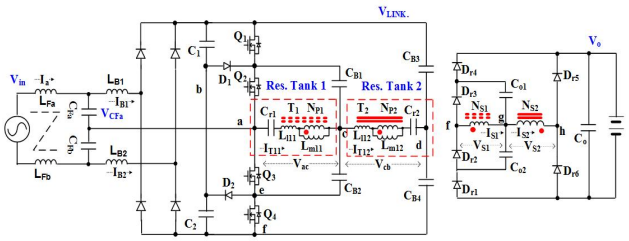
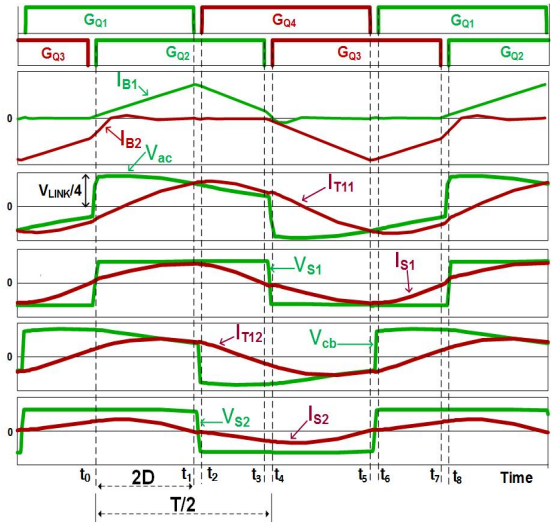


(a) The proposed single-phase 3-level AC/DC converter



(b) Operating waveforms of the proposed 3-level AC/DC converter

Fig. 1. The proposed single-phase single-stage 3-level AC/DC converter and its operating waveforms.

application of electric vehicles to areas where the three phase supply is not accessible and to improves the power density and efficiency of EV charging systems that operate within a wide controllable output voltage range ($200V_{dc}$-$430V_{dc}$).

2. The Proposed Single-Phase Single-Stage Three-Level AC-DC Converter

Fig. 1(a) shows the circuit diagram of the proposed single-phase single stage three level AC/DC LLC resonant converter. It is powered by a single-phase AC source ($220V_{rms}$) and comprises of input filters (L_{Fa}/L_{Fb}, C_{Fa}/C_{Fb}), boost inductors (L_{B1}/L_{B2}), input rectifiers and a three level LLC resonant converter for output voltage regulation. The filter capacitors (C_{Fa}, C_{Fb}) and filter inductors (L_{Fa}, L_{Fb}) are connected to the single-phase input source to filter the input currents. The neutral point of the filter capacitors (C_{Fa}, C_{Fb}) is connected between the source of switch Q_2 and the drain of switch Q_3. The boost inductors (L_{B1}, L_{B2}) are connected to the input rectifiers and each pair of the switching devices (Q_1 & Q_4) and (Q_2 & Q_3) in the primary side is alternately switched on and off with a fixed duty ratio of 50%. During the interval t_0~t_1 Q_1 & Q_2 are switched on likewise during the time interval t_4~t_5 Q_3 & Q_4 are switched on; the boost inductors (L_{B1}, L_{B2}) are energized according to the phase shift modulation of the three level converter. When the switching device Q_1 (or Q_4) is switched off during the interval t_2~t_3 (or t_6~t_7), the boost inductors (L_{B1}, L_{B2}) transfers the previously stored energy to the link capacitors C_1 and C_2 and their currents begin to reduce. The proposed single stage converter has two transformers (T_1, T_2) whose primary windings are connected in parallel and the secondary windings are connected in series to ensure proper load sharing within the two transformers. The resonant circuits (Res. Tank 1, Res. Tank 2) operates with a constant switching frequency of Q_1 and Q_4 (Q_2 and Q_3), that alternately operate with a 50% duty. Output voltage regulation is done via phase modulation of the primary switching devices. 1/4 of the link voltage (V_{LINK}) is applied across the primary sides of each resonant circuits (Res. Tank 1, Res. Tank 2) and a voltage according to the gain characteristic of the converter and the phase shift (D) is reflected to the secondary windings connected in series across the output diodes (D_{r1}~D_{r6}). In addition, since the proposed single-phase single stage three-level AC/DC converters operate with a fixed frequency, the magnetic inductances of the transformers (L_m) are designed to be considerably bigger than those in conventional LLC resonant converters operating with variable frequency control and as a result, limits conduction losses.

3. The Operating Modes Of The Proposed Converter

Mode 1 (t_0~t_1): In mode 1, the switching devices Q_1 and Q_2 are turned on. The filter capacitor voltage (V_{CFa}) is applied across the input boost inductor (L_{B1}) and current flows from C_{Fa} through L_{B1}, the input rectifier diodes, Q_1 & Q_2 and returns to C_{Fa}. The boost inductor (L_{B1}) is energized while the boost inductor L_{B2} resets to zero. 1/4 of the link voltage (V_{LINK}) is applied across the primary terminals of the resonant circuits (Res. Tank 1, Res. Tank 2) and power is transferred to the secondary terminals.

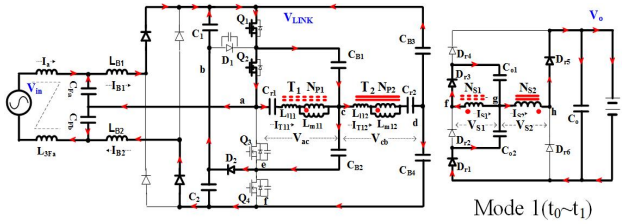


Fig. 2. Current flow in mode 1 (t_0~t_1).

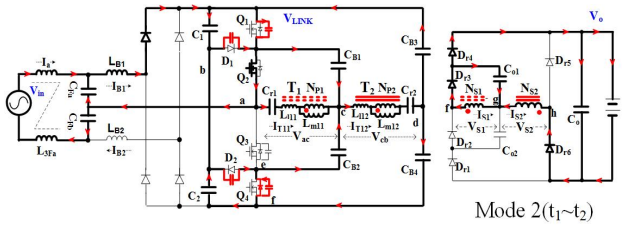


Fig. 3. Current flow in mode 2 (t_1~t_2).

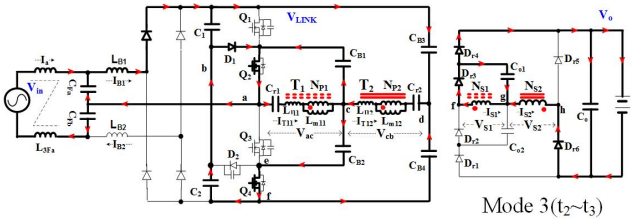


Fig. 4. Current flow in mode 3 (t_2~t_3).

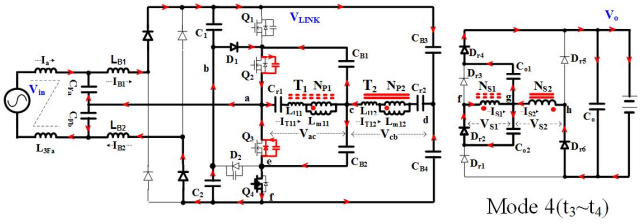


Fig. 5. Current flow in mode 4 (t_3~t_4).

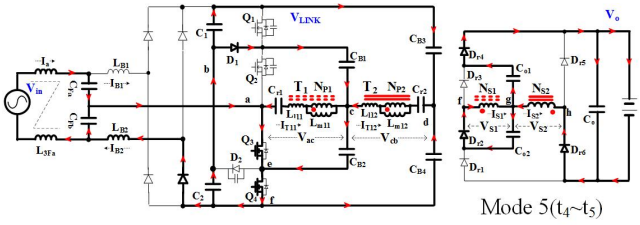


Fig. 6. Current flow in mode 5 (t_4~t_5).

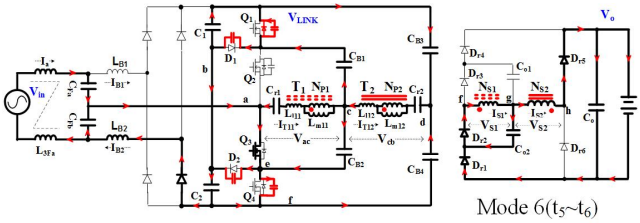


Fig. 7. Current flow in mode 6 (t_5~t_6).

Mode 2 (t_1~t_2): At t_1, Q_1 is switched off and its parasitic capacitor is charged while that of Q_4 is discharged. This mode ends when the voltage across the parasitic capacitor of Q_1 is clamped to half ($\frac{1}{2}V_{LINK}$) of the link voltage and when the voltage across the parasitic capacitor of Q_4 decreases to zero.

Mode 3 (t_2~t_3): This is a freewheeling stage; the switching device Q_1 is switched off and Q_4 is switched on with ZVS. Q_2 remains on and the energy previously stored in the boost inductor LB2 is transferred to the link capacitors. Also, resonant current in Res. Tank 1 flows through Q_2, C_{r1}, T_1, C_{B1} and back to Q_2. Simultaneously, resonant current in Res. Tank1 flows through C_2, clamping diode D_1, Q_2, C_{r1}, T_1, the blocking capacitors C_{B2} and Q_4 while the resonant current in Res. Tank 2 flows through the link capacitor(C_1) C_{B3}, C_{r2}, T_2, C_{B2}, Q_4 and the link capacitor(C_2)

Mode 4 (t_3~t_4): In this mode, Q_2 is switched off and its parasitic capacitor begins to charge while that of Q_3 is discharged. This mode ends when the voltage across the parasitic capacitor of Q_2 is clamped to half ($\frac{1}{2}V_{LINK}$) of the link voltage and when the voltage across the parasitic capacitor of Q_3 decreases to zero. Q_3 is switched on with ZVS.

Mode 5 (t_4~t_5): In this mode, the switching devices Q_3 and Q_4 are switched on, the boost inductor L_{B1} completely reset to zero while the boost inductor L_{B2} is energized as current flows from C_{Fb} through Q_3 & Q_4, the input rectifier diode and L_{B2}. In addition, $\frac{1}{4}$ of the link voltage ($1/4V_{LINK}$) is applied across the primary terminals of the resonant circuits (Res. Tank 1, Res. Tank 2) and power is transferred to the secondary terminals

Mode 6 (t_5~t_6): At t_5, Q_4 is switched off and its parasitic capacitor (C_{oss4}) is charged to the voltage across C_2. Simultaneously, the capacitor (C_{oss1}) across Q_1 is discharged to zero. In addition, the junction capacitance (C_{JD1}) of clamping Diode1 (D_1) is charged while the junction capacitance (C_{JD2}) of clamping diode 2 is discharged. This mode ends when the voltage across the parasitic capacitor of Q_4 is clamped to half ($\frac{1}{2}V_{LINK}$) of the link voltage and when the voltage across the parasitic capacitor of Q_1 decreases to zero.

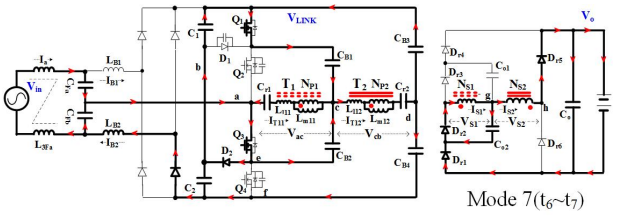


Fig. 8. Current flow in mode 7 (t_6~t_7).

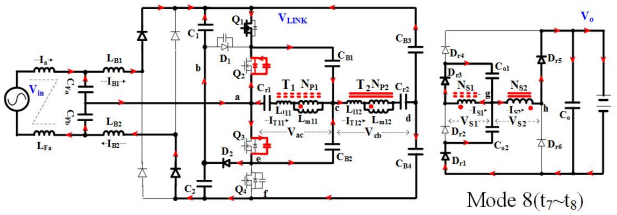


Fig. 9. Current flow in mode 8 (t_7~t_8).

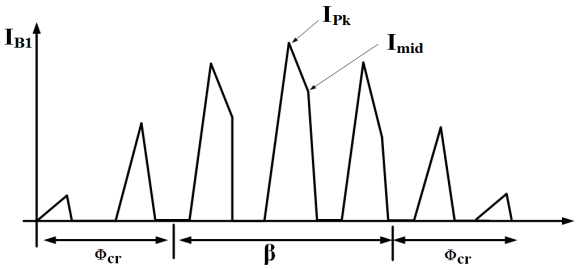


Fig. 10. Boost inductor's current waveform.

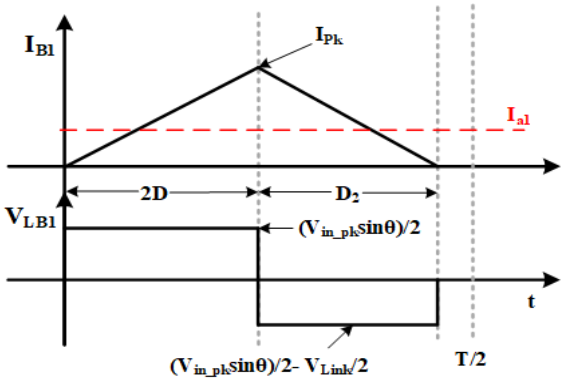


Fig. 11. Boost inductor's waveforms in the interval 0≤Θ≤∅cr.

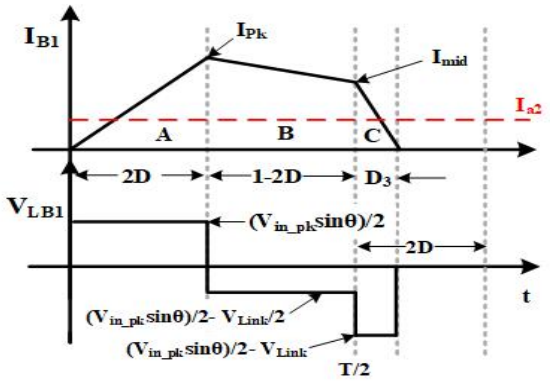


Fig. 12. Boost inductor's waveforms in the interval ∅cr≤Θ≤(π-∅cr).

Mode 7 (t_6~t_7): This is a freewheeling stage; the switching device Q_4 is switched off and Q_1 is switched on with ZVS. In addition, Q_3 remains on and the energy previously stored in the boost inductor (L_{B2}) is transferred to the link capacitors as current flows from C_{Fb} through Q_3, blocking diode D_2, input capacitor C_2, the input rectifier diodes, L_{B2}, and back to C_{Fb}. During this period, the inductor current of L_{B2} begins to reset.

Mode 8 (t_7~t_8): In this mode, Q_3 is switched off and its parasitic capacitor begins to charge while that of Q_2 is discharged. This mode ends when the voltage across the parasitic capacitor of Q_3 is clamped to half ($\frac{1}{2}V_{LINK}$) of the link voltage and when the voltage across the parasitic capacitor of Q_2 decreases to zero. Q_2 is switched on with ZVS and the switching cycle restarts.

4. Analysis Of The Single Stage AC/DC Converter

4.1 Steady state analysis to accurately design the boost inductance

For high power application and input power factor correction, the boost inductors of single-phase single-stage AC/DC converter are designed to operate in discontinuous mode (DCM). This is to ensure that the boost inductors (L_{B1}, L_{B2}) completely rest before the next switching cycle. The power transferred to the output of the single stage converter is a function of the link voltage (V_{LINK}) which is a function of the boost inductance (L_{B1}, L_{B2}), switching frequency (f_s), peak input voltage (V_{in_pk}) and the phase shift (D). The inductance of the boost inductor significantly affects the performance of the three level single stage converter. The link voltage (V_{LINK}) decreases with an increase in boost inductance when all the other parameters are kept constant. Fig. 10 shows the waveform of the boost inductor's current operating in the discontinuous mode over half the period.

The boost inductor's current waveform is divided into two intervals. Within the interval $0 \le \Theta \le \varnothing_{cr}$ and $(\varnothing_{cr} + \beta) \le \Theta \le \pi$, the boost inductor currents completely reset to zero after the switch Q_1 is switched off. However, in the interval $\varnothing_{cr} \le \Theta \le (\pi - \varnothing_{cr})$, the boost inductor currents slowly decrease after Q_1 is switched off, and rapidly reset to zero after Q_2 is switched off.

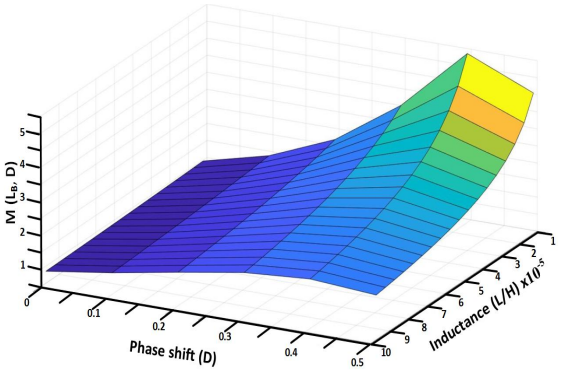


Fig. 13. Voltage gain characteristics [M(L_B, D)] as a function of the boost inductance (L_B) and phase-shift(D) of a single-phase single stage AC/DC converter.

In the following analysis, we assume Va is taken as reference voltage.

From the voltage-second analysis of the boost inductor operating in the interval $0 \le \Theta \le \varnothing_{cr}$, the critical angle $\varnothing_{cr}$ is expressed by

$$\phi_{cr} = \sin^{-1}\left(\frac{V_{LINK}}{V_{in\_pk}}(1-2D)\right) \quad (1)$$

the average input current in the interval $0 \le \Theta \le \varnothing_{cr}$ is determined by

$$I_{a1}(\theta) = \frac{D^2 V_{LINK}\sin(\theta)}{4L_B f_s\left(\frac{V_{LINK}}{V_{in\_pk}} - \sin(\theta)\right)} \quad (2)$$

Also, the average input current in the interval $\varnothing_{cr} \le \Theta \le (\pi - \varnothing_{cr})$ is determined by

$$I_{a2}(\theta) = \frac{V_{LINK}V_{in\_pk}\sin(\theta)(4D^2+1) - V_{LINK}(1-D)^2}{16L_B f_s\left(V_{LINK} - V_{in\_pk}\sin(\theta)\right)} \quad (3)$$

However, the converter's input power is expressed by

$$P_{IN} = \frac{4}{\pi}\left(\int_0^{\phi_{cr}} V_{in} n . I_{a1}(\theta)d\theta + \int_{\phi_{cr}}^{\frac{\pi}{2}} V_{in} . I_{a2}(\theta)d\theta\right) \quad (4)$$

substituting $I_{a1}(\theta)$ and $I_{a2}(\theta)$ into Eqn.4

$$P_{IN} = \frac{4}{\pi}\left(\int_0^{\phi_{cr}} V_{in} . \frac{D^2 V_{LINK}\sin(\theta)}{4L_B f_s\left(\frac{V_{LINK}}{V_{in\_pk}} - \sin(\theta)\right)}d\theta + \int_{\phi_{cr}}^{\frac{\pi}{2}} V_{in} . \frac{V_{LINK}V_{in\_pk}\sin(\theta).(4D^2+1) - V_{LINK}(1-D)^2}{16L_B f_s(V_{LINK} - V_{in\_pk}\sin(\theta))}d\theta\right) \quad (5)$$

Hence, the boost inductance is calculate with Eqn. 6.

$$L_B = \frac{4}{\pi}\left(\int_0^{\phi_{cr}} V_{in} . \frac{D^2 V_{LINK}\sin(\theta)}{4P_{IN} f_s\left(\frac{V_{LINK}}{V_{in\_pk}} - \sin(\theta)\right)}d\theta + \int_{\phi_{cr}}^{\frac{\pi}{2}} V_{in} . \frac{V_{LINK}V_{in\_pk}\sin(\theta).(4D^2+1) - V_{LINK}(1-D)^2}{16P_{IN} f_s(V_{LINK} - V_{in\_pk}\sin(\theta))}d\theta\right) \quad (6)$$

where V_{LINK} is the Link voltage,
L_B is the Boost inductance (L_B=L_{B1}=L_{B2})
V_{in_pk} is the peak input voltage
$\varnothing_{cr}$ is the critical angle,
f_s is the switching frequency and
D is the phase shift between the switches.

At steady state, we assume that the boost inductor's reset current equals the load current. The voltage gain $\left[M(L_B, D) = \frac{V_{LINK}}{V_{in\_pk}}\right]$ of the converter's PFC circuit is expressed by

$$M(L_B, D) = \frac{\left[4K - (4D^2-1) \pm \sqrt{(4K-(4D^2-1))^2 + 4(8K+(2D-1)^2)4D^2}\right]}{2(8K+(2D-1)^2)} \quad (7)$$

where $K = \frac{2L_B}{RT}$; R= the Load and T= the Period.

Fig. 13 shows a three-dimensional plot of the PFC circuit's voltage gain [M(L_B, D)] with respect to the phase shift and boost inductance. The simulation result of the PFC circuit's voltage gain [M(L_B, D)] shows that the magnitude of the voltage gain is inversely proportional to the boost inductance (L_B) and proportional to the phase shift (D).

4.2 The voltage gain analysis of converter's resonance circuit

The single-phase single-stage AC/DC converter operates with a constant frequency and it's output voltage (V_o) is directly proportional to the transformers turn ratio. The link voltage (V_{LINK}) decreases with a decrease in turn ratio when all the other parameters are kept constant. The primary terminals of the resonant circuits (Res. Tank 1, Res. Tank 2) are connected in parallel while the secondary terminals are connected in series. The converter's output voltage of is the sum of the voltages across the secondary windings. The transformers are esigned considering the conditions in which maximum current

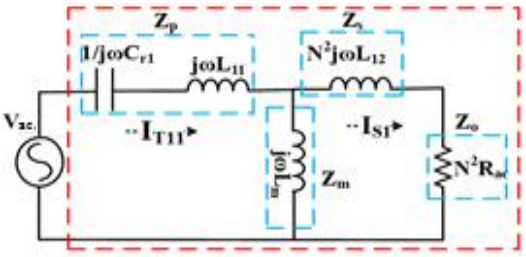


Fig. 14. Equivalent circuit of the resonant tank.

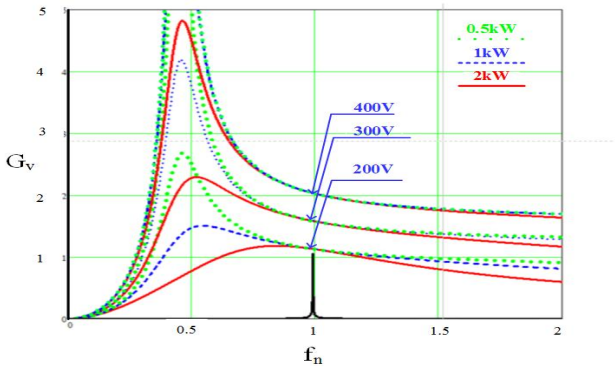


Fig. 15. Voltage gain of the resonant tank.

flows in the converter (V_{LINK}=400V and V_o=200V at full load). The equivalent circuit (Res. Tank 1) of one of the converter's resonant tanks is shown in Fig. 14. Where L_{l1}, L_{l2} and L_m are respectively the primary leakage inductance, the secondary leakage inductance and the magnetizing inductance of transformer 1. Z_o is the output load while Z_p, Z_m and Z_s are respectively the primary, magnetizing and the secondary impedance of the resonant circuit. C_{r1} is the resonant capacitor, N is the turn ratio of transformers and Z_{in} is the total impedance of one of the resonant circuits. we assume that the parameters of the two transformers are identical, that is

$$L_{l1} = L_{l11} = L_{l12},\quad L_m = L_{m11} = L_{m12}$$
$$L_{l2} = L_{l21} = L_{l22},\quad L_{eq} = L_{eq1} = L_{eq2}$$

The normalized voltage gain equation of the proposed converter is expressed by

$$G_V = \frac{1}{N}\left|\frac{1}{1+A-\left(\frac{1}{f_n}\right)^2\left(A+\frac{B}{B+1}\right)+jQ(1+B)\left(f_n-\frac{1}{f_n}\right)}\right| \tag{8}$$

where $A=\frac{L_{l1}}{L_m}$, $B=\frac{N^2L_{l2}}{L_m}$, $f_n=\frac{f_s}{f_r}$,

$Q=\frac{2\pi f_r L_{eq}}{N^2R_{ac}}$ and $R_{ac}=\frac{8N^2}{\pi^2}R_L$

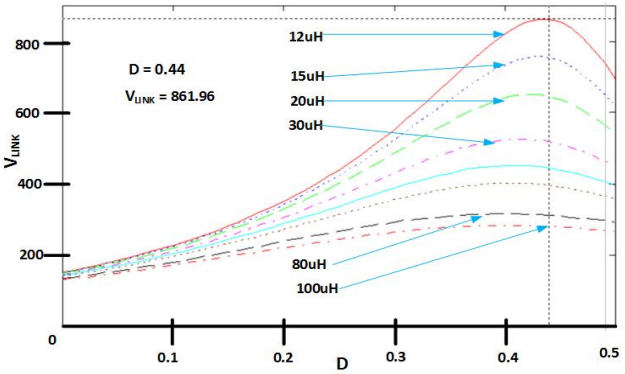


Fig. 16. V_{LINK} voltage simulation.

The voltage gain of the resonant tank for different operating output voltage and load is presented in Fig. 15.

5. Design Consideration

In this section, the design procedure is explored based on the analysis in the previous section. The design specifications are illustrated below.

Input voltage: V_{in} = 220V_{rms} ±15%
Output voltage: V_o = 200~430V_{dc}
Maximum Link voltage: V_{LINK} = 860V_{dc}
Switching frequency: f_s= 112.8kHz
Power output: P_o =2kW
Required Efficiency: η = 90%
Turn ratio $N=N_1/N_2$ = 1

5.1 Boost inductance design

Experiments has proven that the link voltage (V_{LINK}) increases with a decrease in boost inductance when all the other parameters are kept constant. In addition, The link voltage (V_{LINK}) increases with a increase in transformer's turn ratio. However, the power delivered to the output is a function of the switching frequency (f_s), the input voltage (V_{in}), the boost inductance (L_B), the phase shift (D) and the link voltage (V_{LINK}).

$$P_o = f(f_s, V_{in}, L_B, D, V_{LINK}) \tag{9}$$

The proposed single stage, single-phase converter is designed to operate over a wide output range of 200V_{dc}~ 430V_{dc} and a unity turn ratio was selected to limit the maximum link voltage range to 860V_{dc}. The boost inductance that will effectively boost the input voltage to the expected maximum link voltage is obtained by substituting the designed parameters into

TABLE I
MAIN RATINGS AND TRANSFORMER PARAMETERS

Input ratings	Input Voltage(V_{in})	$220V_{AC}$	
	Output voltage (V_o)/ output Diode(I_{omax})	$200V_{dc}$/10A, $430V_{dc}$/4.65A (2kW)	
	Switching frequency(f_s)/ resonant frequency(f_r)	112.8kHz/109.8kHz	
Used Devices	Switching Devices(Q_1~Q_4)	SCT3030AL (650V/70A/30mΩ)	
	Input Diodes	GP2D050A120B [1200V/50A/1.6V/SIC]	
	Clamping Diodes(D_1~D_2)	GP2D050A060B [600V/50A/1.45V/SIC]	
	Output Diodes	GP2D050A060B [600V/50A/1.45V/SIC]	
Para meters	L_{Fa}~L_{Fb}/C_{Fa}~C_{Fb}/L_{B1}~L_{B2}	4m0.94mH/3.3uF/11.5uH	
	C_{r1}~C_{r2}/C_B/C_{o1},C_{o2}	220nF/4.4uF/4.4uF	
Trans former (T)	Core material	Ferrite Core (PL-7, 6062))	
	Primary/ Secondary Inductance	L_p/L_s	83.13uH/84uH
	Magnetizing/Leakage Inductance	L_m/L_{eq}	78.19uH/10.34uH
	Turn Ratio	N(N_1/N_2)	1(8T/8T)

equation (6). A boost inductance of 11.7 uH was calculated.

A boost inductance (L_B= 12μH) plotted on Fig. 16 shows that the PFC circuit will effectively boost the input voltage to a maximum link voltage (V_{LINK}) of $861.96V_{dc}$ for proper output voltage regulation at full load, without exceeding the breakdown voltage of the switching devices.

5.2 Maximum magnetizing inductance calculation

In a three level topology, the inner most switching devices (Q_2 & Q_3) are easily switched on with ZVS compared to the outer most switching devices (Q_1 & Q_4). This is because during the dead time (t_1~t_2 and t_7~t_8) a huge amount of energy is required to charge and discharge the capacitors of these switching devices (Q_1 & Q_4) and the clamping diodes (D_1 & D_2). However, during the dead time (t_3~t_4 and t_5~t_6) the capacitances of the clamping diodes are unchanged and as a result, the switching devices (Q_2 & Q_3) are easily switched on with ZVS. The maximum magnetizing inductance is calculated considering the converter's worst-case operating condition; (operating with the minimum output voltage of $200V_{dc}$ at rated load). This is because, at this operating condition, the reflected voltage to the primary during the dead time is minimum. The maximum magnetizing inductance is determined by

$$L_m = \frac{(NV_o)t_{dead}}{8f_s(2.C_{oss}+2.C_{JD}).\frac{V_{LINK}}{2}} \quad (10)$$

In this paper, two transistors were connected in parallel to withstand the circulating current. In addition, from the topology of the proposed converter, the voltage across the secondary terminals of each transformer is given by $NV_o=V_{LINK}/4$. Hence, the maximum magnetizing inductance is expressed by

$$L_m < \frac{t_{dead}}{16f_s(4.C_{oss}+2.C_{JD})} \quad (11)$$

from the MOSFET and diode datasheet,

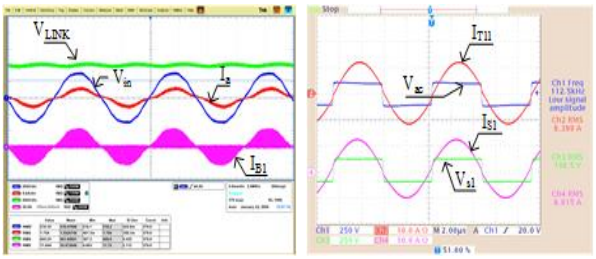
$$C_{oss} = 300pF \text{ and } C_{JD} = 490pF$$

$$L_m < \frac{418ns}{16(112.5khz)(4.300pF+2.490pF)} = 106uH$$

A magnetic inductance (L_{m11}) of 78uH was used to realize the proposed single-phase three level AC/DC LLC converter.

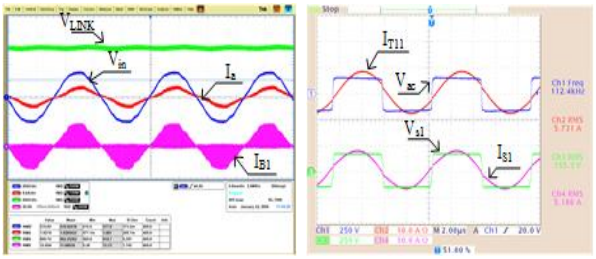
6. Experimental Results

A 2kW single-phase single stage three level AC/DC converter with a wide output voltage range characteristic was designed and implemented to verify the operation of the proposed converter. The proposed converter is controlled with a program loaded in a 16-bit dsPIC33FJ16GS502 micro-controller that constantly senses the output voltage and current and operates the switching devices with a fixed frequency. The converter's operating output voltage (V_o) is controlled through phase shift (D). Table 1 shows the circuit's device ratings and transformers parameters. Fig. 17, Fig. 18 and Fig. 19 show the inductor currents (I_{B1}), input voltages (V_{in}), phase currents (I_a), link voltages (V_{LINK}) and primary voltages/currents of the LLC resonant circuit (Res. Tank 1). Fig. 20 shows the measured linked voltages and Fig. 21 shows the efficiency characteristics and total harmonic distortion (THD) curves of the proposed converter for different loads of each output voltage. Experimental results show that all the switching devices are switched on



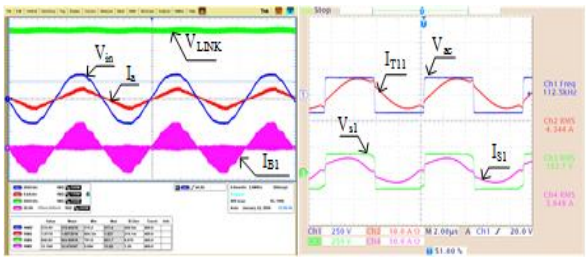
(a) Ch1:200V/div, Ch2:5A/div Ch3:200V/div, Ch4:30A/div, 4ms/div (b) Ch1:250V/div, Ch2:10A/div, Ch3:250V/div, Ch4:10A/div, 1.6us/div.

Fig. 17. Experimental wave-forms. (a) the PFC Circuit, (b) the current/ voltage across the transformer's primary and secondary [200V/1.5kW].



(a) Ch1:200V/div, Ch2:5A/div, Ch3:200V/div, Ch4:30A/div, 4ms/div (b) Ch1:250V/div, Ch2:10A/div, Ch3:250V/div, Ch4:10A/div, 1.6us/div.

Fig. 18. Experimental wave-forms. (a) the PFC Circuit, (b) the current/ voltage across the transformer's primary and secondary [300V/1.5kW].



(a) Ch1:200V/div, Ch2:5A/div, Ch3:200V/div,Ch4:30A/div, 4ms/div (b) Ch1:250V/div, Ch2:10A/div, Ch3:250V/div,Ch4:10A/div, 1.6us/div.

Fig. 19. Experimental wave-forms. (a) the PFC Circuit, (b) the current/ voltage across the transformer's primary and secondary [430V/1.5kW].

with ZVS especially at low loads and, the input currents have limited distortion. Moreover, the maximum measured link voltage is less than the breakdown voltage of the switching devices. The highest efficiencies are obtained with the $200V_{dc}$ output experiments. However, the converter's efficiencies decrease as the operating output voltage (V_o) increases due to the increase in input boost inductor currents that increase conduction losses. A maximum

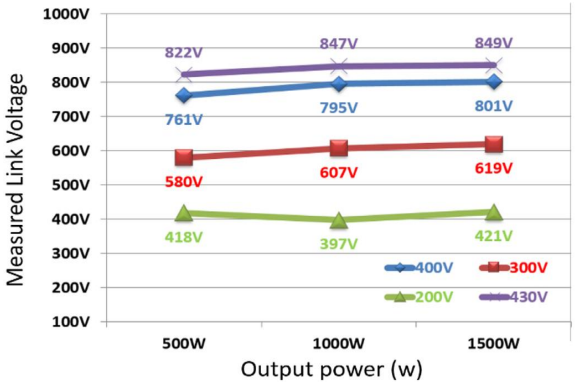


Fig. 20. Measured link voltage (V_{LINK}) of the designed prototype.

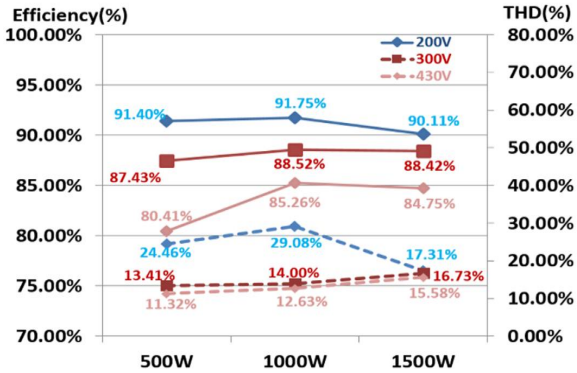


Fig. 21. Efficiency and THD of the proposed single-phase single stage AC/DC converter.

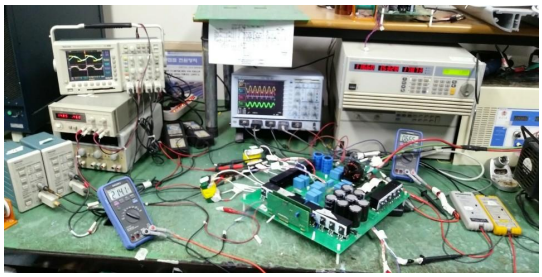


Fig. 22. Setup of the laboratory prototype.

efficiency of 91.75% was recorded with a $1kW/200V_{dc}$ experiment while a minimum efficiency of 80.41% was registered with a $500W/430V_{dc}$ experiment.

Fig. 22 shows the setup of the laboratory prototype with the proposed single-phase three level single stage converter.

7. Conclusion

A single-phase single stage three level AC/DC converter with a wide controllable output voltage was presented. The proposed converter integrates a PFC circuit and a three level DC/DC LLC circuit into one. Moreover, it operates at a fixed frequency and provides a wide controllable output voltage (200Vdc-

30Vdc) with a high efficiency over a wide load range. In addition, all the switches are switched on with ZVS and the overall THD of the designed converter is smaller than that of previous single phase single stage AC/DC converters.

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