A New Overlap Current Restraining Method for Current-source Rectifier

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Abstract

To ensure a DC current path and avoid large voltage overshoot of the DC-link inductor, alternating PWM pulses in the current-source rectifier should be supplemented by overlap time, which generates an overlap current and causes input current distortion. In this study, the influence of overlap time is illustrated by comparing the AC-side current before and after overlap time is added. The overlap current distribution caused by overlap time is discussed under different modulation carriers, including triangle carrier, positive-going carrier, and negative-going carrier. The quantitative relationship between the extra harmonics of the AC-side current and overlap time is based on the Fourier analysis. Based on the commutation analysis, a new carrier modulation scheme that can restrain overlap current is proposed. A 3 kW prototype is established to verify the effectiveness of the influence of overlap time and the proposed restraining modulation scheme.

Key words: Current-source rectifier, Grid current, Overlap current harmonics, Overlap time, Restraining method

I. INTRODUCTION

Power grid harmonics is one of the most pressing issues of the modern power system. The PWM rectifier is an effective solution to reduce harmonics and achieve high power factor. On the basis of the characteristics of the DC-link power supply, the PWM rectifier can be divided into voltage-source rectifier (VSR) and current-source rectifier (CSR) [1]-[4]. Although VSR is widely applied in industry, CSR has its advantages in its own application areas. Compared with VSR, CSR features a step-down function, smaller filter size, in-rush current limiting capability, and better direct current control, reliability, and protection, resulting in its wide use in four-quadrant motor drive systems, new energy power generation systems, superconducting rectifier system systems, and data centers [5]-[8].

Setting the dead time for alternating pulses is necessary to avoid the shoot-through in any arm of the VSR [9], [10]. Similarly, the CSR is required to add the overlap time to PWM signals to prevent DC current interruption [11]-[14].

As pointed out in [15]-[17], overlap time causes errors in the current control and changes the pulse width of the AC-side current, which increases the low-order harmonics in the input current and influences device selection [20]-[22]. Therefore, the current ripple should be restricted within a certain range.

A compensation method for the overlap time is proposed in [23].Overlap time is added to the gate signal of the switch that bears a reverse voltage. Transition time is assumed to be very short and can be omitted. However, transition time is long when the device voltage crosses zero or the DC current is low at a light load. In that case, the compensation method will not work.

The scheme of low-voltage stress space vector PWM control for current-source PWM rectifiers is proposed in [24]. Although this scheme can keep switches in a natural commutation state, [24] does not provide an analysis of the influence of overlap time on the non-natural commutation process.

To restrain the current ripple caused by overlap time, a new overlap time compensation method that modulates the PWM carrier according to neutral voltages of phase legs is proposed in this study. Compared with the traditional scheme, the new compensation method adopts a sawtooth carrier

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instead of the traditional triangle carrier, making it flexible and effective in reducing the overlap current in a non-natural commutation process [25]. To illustrate the new compensation method further, detailed commutation processes with positive-going and negative-going sawtooth carriers are described separately. The proposed carrier modulation method is verified through simulation and experiments in a 3 kW all-SiC buck rectifier, which proves that the new modulation method is effective in the non-natural commutation process, and the overlap current can be reduced greatly with a suitable PWM carrier.

This paper is structured as follows. In Section II, the traditional commutation process with a triangle carrier is analyzed, and the overlap current distribution is listed to explain the influence of overlap time. The quantitative relationship between overlap time and grid current harmonics is also deduced based on the pulse equivalent principle. Section III introduces the sawtooth carrier modulation scheme to restrain the influence of overlap time. Finally, a 3 kW prototype is built to prove the effectiveness of the theoretical analysis and the proposed carrier modulation scheme.

II. INFLUENCE OF OVERLAP TIME ON THE GRID-SIDE CURRENT

A. CSR Commutation Analysis

Fig. 1 shows the topology of CSR, where a transistor is in series with a diode to block the voltage in both directions. The $e_i(x=a,b,c)$ is the voltage of the three-phase voltage source, and $u_a$ is the neutral potential of the phase leg. $i_{xu}$ is the grid-side current, and $i_{px}$ is the AC-side current. The

![Fig. 1. Topology of the three-phase current-source PWM rectifier.](image1)

![Fig. 2. Current commutation from $T_1$ to $T_3$.](image2)

![Fig. 3. AC-side current during commutation operation from $T_1$ to $T_3$ with overlap time.](image3)

AC-side filter is composed of $L_x$ and $C_x$. $T_1$ and $D_i (i=1, 2, \ldots, 6)$ represent the switches of the converter. $I_{dc}$ is the DC-link inductor, and $R_l$ is the load.

Ensuring a DC current path is compulsory because the inductor is adopted as the DC-link filter of the CSR.

Therefore, the commutation in the CSR happens between one of the switches in the three upper legs and one switch in the three lower legs. To keep a DC current loop, the signal to turn off the switch should be delayed for a period of time $t_o$, which is called the overlap time. During overlap time $t_o$, both the switches to be turned on and off are driven simultaneously by PWM pulses.

To assess the effect of overlap time on the grid-side current, the switching process from switch $T_1$ to switch $T_3$ is analyzed. The derivation of the commutation cell is shown in Fig. 2. This study assumed that the PWM signals are ideal and the switching process is instantaneous. Fig. 3 shows the waveform of current commutation from $T_1$ to $T_3$. $S_1$ and $S_2$ are the PWM signals without overlap time, and $S_1'$ denotes the PWM signals with added overlap time. $i_{pa}$ and $i_{pb}$ are the AC-side current of Phase A and Phase B without overlap time, respectively. The $i_{pa}'$ and $i_{pb}'$ are the AC-side current with overlap time. The $\Delta i_{pa}$ and $\Delta i_{pb}$, called overlap currents, are the differences of the AC-side with and without overlap time ($\Delta i_{pa}=i_{pa}'-i_{pa}$, $\Delta i_{pb}=i_{pb}'-i_{pb}$).

In simplifying the switching process analysis, the midpoint voltage of the phase leg $u_i(x=a,b,c)$ can be neglected because the forward voltage across switch $T_j$ and diode $D_i$ is considerably lower than $u_{ba}$, $u_{ba}=u_{bc}-u_{ab}$. Before the moment $t_1$, switch $T_1$, and diode $D_1$ are in the conducting state. At $t_1$, overlap time $t_o$ occurs between switches $T_1$ and $T_3$. Therefore, the conduction states of the switches $T_1$ and $T_3$ depend on the voltage across diode $D_3$, which is $u_{ba}$. When the voltage across $D_3$ is positive, switch $T_3$ is turned on at $t_1$. Otherwise, switch $T_3$ will be turned on until overlap time $t_o$ is over.
because the voltage across \( D_1 \) is negative.

According to the neutral voltage of \( u_a \) and \( u_b \), the commutation operation from \( T_1 \) to \( T_3 \) can be divided into two cases:

1) When \( u_a > u_b \)

As shown in Fig. 3(a), during \( t_1 \), diode \( D_3 \) bears the reverse voltage \( u_{mb} \). Therefore, during overlap time \( t_2 = t_1 - t_2 \), the DC current cannot flow through \( T_3 \) and continues to flow through \( T_1 \), which generates the negative overlap current \( \Delta i_{pa} \).

2) When \( u_a < u_b \)

During \( t_1 \), specifically \( u_{mb} > 0 \), diode \( D_3 \) is under forward bias at \( t_1 \) and switch \( T_3 \) can be turned on immediately. Overlap time has no influence on the communication process and will not produce an overlap current, which can be seen in Fig. 3(b).

B. Overlap Current Distribution

To obtain the overlap current distribution, the switching period is divided into six sectors according to the modulation signals \( u_{ma}, u_{mb}, \) and \( u_{mc} \). The commutation sequence among switches is identical in the same sector. Furthermore, the existence of an overlap current depends on the voltage across the diode to be turned on, which is the difference between bridge phase voltages \( u_c \). Theoretically, an angle offset exists between midpoint voltage \( u_a \) and modulation signal \( u_{ma} \) [23]. Therefore, two-bridge phase voltage distributions are present in each sector, and the modulation period can be further subdivided into 12 sectors (Fig. 4).

Take Sector I interval \([t_0, t_1]\) as an example. As \( u_{ma} > u_{mb} > u_{mc} \), the switching sequence is \( (T_1, T_2) \rightarrow (T_3, T_4) \rightarrow (T_5, T_6) \rightarrow (T_7, T_8) \rightarrow (T_9, T_{10}) \rightarrow (T_{11}, T_{12}) \), wherein \( (T_1, T_2) \) is the commutation from \( T_1 \) to \( T_2 \). According to the relationship among the neutral potential of the phase legs, Sector I can be subdivided into two intervals, \([t_0, t_1]\) and \([t_1, t_2]\). The relationship of the neutral potential is \( u_b > u_a > u_c \) in \([t_0, t_1]\) and \( u_b > u_a > u_c \) in \([t_1, t_2]\). Therefore, the current distribution should be analyzed in two cases in Sector I, namely, \( u_a > u_b > u_c \) and \( u_b > u_a > u_c \).

In interval \([t_0, t_1]\), the first commutation is from \( T_3 \) to \( T_1 \). During overlap time, switch \( T_3 \) and the PWM signal of switch \( T_1 \) are turned on. The voltage across diode \( D_1 \) is \( u_{mc} \), which changes in different intervals. In interval \([t_0, t_1]\), diode \( D_3 \) is in positive bias due to \( u_{mb} > u_c \). Therefore, the current flows immediately from \( T_3 \) to \( T_1 \). \( T_1 \) is turned on and does not produce the overlap current. The next commutation is from switch \( T_1 \) to switch \( T_3 \). During overlap time, switches \( T_1 \) and \( T_3 \) are turned on. The voltage across diode \( D_1 \) is \( u_{ab} \), which is positive in interval \([t_0, t_1]\). Therefore, the current flows immediately from \( T_3 \) to \( T_1 \) when \( T_1 \) is turned on and does not produce an overlap current.

The third commutation is from \( T_1 \) to \( T_3 \). Similarly, the voltage across diode \( D_3 \) is \( u_{ac} \), which is negative in interval \([t_1, t_2]\). With diode \( D_3 \) in reverse bias, diode \( D_3 \) is turned off during overlap time, and no current flows through switch \( T_3 \). Compared with the ideal commutation process, the turn on time in Phase A is the added overlap time \( t_o \), while the turn on time in Phase B is the reduced overlap time \( t_{of} \). Therefore, the overlap currents \( \Delta i_{pa} \) in Phase A and \( \Delta i_{pb} \) in Phase B are produced, as seen in Fig. 5(a). In a similar way, the commutation process with overlap time in Fig. 5(b) can be analyzed without the process being described in detail.

For convenient analysis, the commutation process in Sector
I is listed in Table 1 ([t_a–t_b]) and Table 2 ([t_c–t_d]). The commutation operation in other sectors can be obtained in a similar way. The characteristics of the overlap current can be obtained based on the commutation analysis in Sector I, where (1) the existence of overlap currents is determined by the voltage across the diode to be conducted, (2) the carrier is symmetrical in a switching cycle, and (3) overlap currents are shown in a positive-negative pair.

C. Harmonic Analysis of the AC-side Current

Dead time in the VSR influences the output voltage [24]. Similarly, overlap time in the CSR produces extra harmonic components in the AC-side current.

In interval [0, t_1], the overlap time will lead to two positive overlap currents in the grid side of Phase A. According to the principle of equivalent impulse, overlap currents can be replaced by the square wave when they have the same area. The amplitude of a square wave can be expressed as

$$\Delta i'_{pa} = \frac{2 \cdot I_{dc} \cdot t_a}{T_c} = 2 \cdot I_{dc} \cdot t_a \cdot f_s,$$  \hspace{1cm} (1)

where $T_c$ is the period of the carrier wave, $I_{dc}$ is the DC current, $t_a$ is the overlap time, and $f_s$ is the frequency of the carrier wave.

In intervals [t_1, t_2] and [t_2, t_3], two overlap currents occur in pairs, one positive current and one negative current, which can be expressed as

$$\Delta i'_{pa} = \left\{ \begin{array}{ll}
I_{dc} \cdot t_a \cdot f_s & (u_m > 0) \\
-I_{dc} \cdot t_a \cdot f_s & (u_m < 0)
\end{array} \right.,$$  \hspace{1cm} (2)

Similarly, the equivalent square wave of the overlap current in [t_3, t_4] can be expressed as

$$\Delta i'_{pa} = -2 \cdot I_{dc} \cdot t_a \cdot f_s.$$  \hspace{1cm} (3)

In [t_4, t_5], the expression of the equivalent square wave is shown in Formula (1).

Fig. 6 is the equivalent waveform of overlap time based on the above analysis. Fig. 6(a) is the equivalent square wave of the overlap current in Phase A, $\Delta i'_{pa}$, which is obtained from (1) to (3). The $\Delta i'_{pa}$ can be further divided into two parts, as shown in Figs. 6(b) and 6(c). The overlap current can be analyzed by comparing neutral voltages of the related phase legs. Therefore, when $u_a > u_b$ and $u_a > u_c$, the overlap current is high. When $u_a < u_b$ and $u_a < u_c$, a high negative overlap current exists. When $u_a$ is between $u_b$ and $u_c$, the overlap current will change from a positive value to a negative value or in reverse depending on the sign of $u_a$.

According to Fig. 6 and (1), (2), (3), the equivalent overlap current $\Delta i'_{pa}$ can be expressed as

$$\Delta i'_{pa} = \Delta i'_{pa1} + \Delta i'_{pa2},$$  \hspace{1cm} (4)

and

$$\Delta i'_{pa1} = \text{sign}(u_a) \cdot I_{dc} \cdot t_a \cdot f_s,$$  \hspace{1cm} (5)

where
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III. METHOD FOR RESTRAINING THE OVERLAP CURRENT

A. Commutation with Positive-going Sawtooth Carrier

The switching sequence is symmetric in a carrier period because the adopted carrier is a triangle wave in the above analysis. For example, the current commutation process in Sector I is as follows: T5 → T3 → T6 → T1 → T3 → T5.

The symmetric commutation process means that overlap currents exist only in half of the switching cycle and not the whole switching cycle. When the PWM carrier is a positive-going sawtooth carrier, which is asymmetric, the symmetric commutation process will not occur.

Take Sector I as an example. When the carrier is replaced by a positive slope sawtooth wave (Fig. 7), the distribution of the overlap current will be different from the distribution in Fig. 5(a). The existence of the overlap current is dependent on whether the voltage sign of the diode is turned on or not. Therefore, according to the relationship of phase bridge voltages in [t0, t1] and in [t1, t2], the commutation operation in Sector I should be discussed in two cases, \( u_a > u_b > u_c \) and \( u_b > u_c > u_a \).

In interval \([t_0, t_1]\), the first commutation is from T3 to T1. During this commutation, diode D3 is in positive bias due to \( u_b > u_c \). Therefore, the current immediately flows from T3 to T1. T3 is turned on and does not generate the overlap current. The next commutation is from switch T5 to switch T1. During this commutation, the voltage across diode D1 is \( u_{dc} \), which is positive. Therefore, the current flows immediately from T3 to T1 when T1 is turned on and does not generate the overlap current. The next commutation from T1 to T3 will be delayed for overlap time due to the negative voltage of diode D3, which generates overlap time. Compared with the triangle carrier in Fig. 5(a), the overlap current is reduced. The overlap current occurs twice in a triangle carrier period but occurs only twice in two positive-going carrier periods.

Similarly, in interval \([t_1, t_2]\), the commutation from T3 to T3 will be conducted immediately due to the forward voltage of diode D3. The next commutation from T1 to T3, and from T3 to
T₃ will be delayed for overlap time because diode D₃ bears a reverse voltage. A comparison of Fig. 7 with Fig. 5(a) reveals that the overlap current occurs three times during a triangle carrier period and four times during the two positive-going carrier periods. In this case, the positive-going carrier is unfavorable. The overlap current distributions in the two cases are listed in Tables III and IV, respectively.

On the basis of the distributions in the two tables, some commutation characteristics with positive-going sawtooth carrier can be concluded as follows. The first commutation is from zero state to non-zero state, the second commutation is between non-zero states, and the last commutation is from non-zero state to zero state. Overlap currents exist in the first commutation but are absent in the last commutation. The overlap current in the second commutation depends on the voltage across the diode to be turned on.

The existence of overlap currents in non-zero state is caused by a diode that is under reverse bias and is about to be turned on. As shown in Table III, overlap currents occur when the commutation is from T₃ to T₁. If the commutation is from T₁ to T₃ instead, then the diode to be turned on will be under positive bias and the overlap current will disappear.

### B. Commutation with Negative-going Sawtooth Carrier

As long as the turn on time of each switch remains unchanged in a carrier cycle, the change of the switching sequence has no influence on the fundamental component of the PWM pulse [14]. Therefore, the negative-slope sawtooth wave can also be adopted as the carrier to modulate the switching sequence.

Fig. 8 illustrates the current commutation in Sector I with the negative-going sawtooth carrier. When the carrier is replaced by a negative slope sawtooth wave (Fig. 8), the distribution of the overlap current will be different from the distribution in Fig. 5(b). According to the relationship of phase bridge voltages in [t₀, t₁] and in [t₁, t₂], the commutation operation in Sector I should be discussed in two cases, u₉ > u₀ > u₄ and u₀ > u₉ > u₄.

In interval [t₀, t₁], the voltage across diode D₃ is positive, and the current flows immediately from T₃ to T₁, which does not produce the overlap current. The next commutation is from switch T₁ to switch T₃. The voltage across diode D₁ is negative voltage u₉. The second commutation from T₁ to T₃ will be delayed for overlap time. So does the commutation from T₃ to T₁. Compared with Fig. 5(b), the overlap current is increased. The overlap current happens three times during a triangle carrier period and four times during two negative-going carrier periods.

In interval [t₁, t₂], both commutations from T₃ to T₁ and T₁ to T₃ occur immediately and do not generate an overlap current. By contrast, the commutation from T₁ to T₃ generates an overlap current for the negative voltage across diode D₃. Compared with Fig. 5(b), the overlap current is reduced. The overlap current occurs thrice during a triangle carrier period and twice during two negative-going carrier periods. The
TABLE V

<table>
<thead>
<tr>
<th>Commutation</th>
<th>Diode to be turned on</th>
<th>Overlap current</th>
<th>Overlap current waves</th>
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</thead>
<tbody>
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<td>T₅→T₁</td>
<td>D₁: uₐ&gt;0</td>
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<tr>
<td>T₁→T₃</td>
<td>D₃: uₐ&lt;0</td>
<td>∆Pₛ</td>
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<tr>
<td>T₃→T₅</td>
<td>D₅: uₐ&lt;0</td>
<td>∆Pₛ</td>
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TABLE VI

<table>
<thead>
<tr>
<th>Commutation</th>
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<th>Overlap current</th>
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<tbody>
<tr>
<td>T₁→T₃</td>
<td>D₃: uₐ&lt;0</td>
<td>∆Pₛ</td>
<td>no</td>
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<tr>
<td>T₃→T₅</td>
<td>D₅: uₐ&lt;0</td>
<td>∆P₣</td>
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Therefore, in Sector I, when \( uₐ>uₖ>uₙ \), the positive-slope sawtooth carrier is adopted. When \( uₕ>uₙ>uₙ \), the negative-slope sawtooth carrier is adopted. In this way, the overlap current can be prevented when commutation happens between non-zero states. The commutation in other sectors can be analyzed in a similar manner. The distribution of the positive-slope and negative-slope sawtooth carriers during one modulation period is presented in Fig. 9.

The steps for the proposed overlap current restraining method are summarized in Fig. 10. The main operation steps are listed as follows:

1) Sample the grid-side capacitor voltages, namely, the neutral voltages of three phase legs, to determine the voltage of diode to be turned on.

2) Compare the capacitor voltages and choose the suitable sawtooth carrier. When \( uₐ>uₖ>uₙ \), \( uₕ>uₙ>uₖ \), or \( uₖ>uₙ>uₖ \), the positive-slope sawtooth wave will be adopted. When \( uₕ>uₖ>uₙ \), \( uₕ>uₖ>uₙ \), or \( uₖ>uₙ>uₖ \), negative-slope sawtooth wave will be adopted.

Compared with commutation under triangle carriers, the proposed modulation method can reduce the overlap current that happens between non-zero commutation during a triangle carrier period. Therefore, the proposed modulation method can thoroughly restrain the overlap current and effectively reduce the harmonics in the AC-side current of the converter.

IV. SIMULATION AND EXPERIMENTAL VERIFICATION

A. Simulation Verification

To verify the validity of the theoretical analysis, the three-phase current-source rectifier system is established in MATLAB and related simulation results are conducted. The simulation parameters are listed in Table 7.

Due to the influence of overlap currents, extra odd harmonics...
are injected into the AC-side currents of the CSR. As analyzed in Section II, the low-order odd harmonics cannot be filtered out by the LC filter and will be amplified by the filter, which leads to the grid-side current distortion. Fig. 11 shows the grid-side current and the total harmonic distortion (THD) analysis waveform with different overlap times. Fig. 11(a) shows that the waveform of the grid-side current is sinusoidal without the overlap time. When the overlap time is added into driving signals, some unexpected influence will occur to the grid-side current. As shown in Figs. 11(b) and 11(c), the harmonic components increase proportionally with overlap time. The THD of grid-side currents is 1.53% without overlap time. When the overlap time is 5 μs, the THD of grid-side currents increases to 9.23%. When the THD of grid-side currents is 10 μs, the THD of AC-side currents increases to 13.73%. The third, fifth, and seventh harmonic components increase greatly as well, which is in agreement with the analysis in Section II that a great amount of odd harmonics as characteristic harmonics will be injected into the AC-side current with added overlap time. However, even non-characteristic harmonics account for a small fraction of total harmonics. The simulation results on even harmonic content with different overlap times are shown in Fig. 12. The even harmonic content is very small and shows few relations with different overlap times. In sum, the third, fifth, and seventh harmonic contents increase greatly and the second- and fourth-order harmonic contents are always kept small. This finding indicates that the overlap time only brings extra odd harmonics to the AC-side current and confirms that the formulas in Section II are reliable.

A comparison of Figs. 11(c) and 11(d) illustrate that the proposed modulation scheme can decrease THD from 13.73% to 8.07%, and the odd harmonics are decreased greatly, which

![Fig. 11. Waveforms of the grid-side current and FFT analysis. (a) 0 μs overlap time. (b) 5 μs overlap time. (c) 10 μs overlap time. (d) 10 μs overlap time with overlap current constraining method.](image)

<table>
<thead>
<tr>
<th>TABLE VII</th>
<th>SIMULATION PARAMETERS OF CSR</th>
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<tbody>
<tr>
<td>Parameter</td>
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<td>Fundamental frequency/Hz</td>
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<tr>
<td>Inductance/mH</td>
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The new modulation method can significantly improve the quality of the grid-side current. When the even harmonics slightly change, the second harmonic increases from 0.37% to 0.47% and the fourth harmonic increases from 0.09% to 0.18% with increasing overlap time. When the proposed modulation scheme is performed under 5 μs overlap time, the second harmonic decreases from 0.42% to 0.3% and the fourth harmonic decreases from 0.14% to 0.06%, which indicates that the overlap time has little influence on even harmonics.

Fig. 13 shows the relationship between the THD of grid-side current and overlap time. Under the traditional and proposed carriers, the harmonic contents increase with overlap time. The new modulation method can reduce the THD of grid-side current, and the improvement is noticeable when the overlap time is long. The new modulation method can significantly improve the grid-side current quality.

B. Experimental Verification

To verify the correctness of the theoretical analysis in Section II and the advantages of the proposed modulation method, a 3 kW experimental prototype is built with the specifications in Table 7. Fig. 14 shows a photograph of the current-source rectifier prototype.

First, the waveform of the grid-side voltage and current conducted under different overlap times and loads are obtained by using traditional modulation methods. Fig. 15(a) shows the grid-side voltage and current waveform of Phase A and harmonics distribution with 10 μs overlap time and 8A DC current, where an apparent current distortion exists in the grid-side current and the THD is 15.82%. Fig. 15(b) is obtained with 2 μs overlap time and 8A DC current, in which the quality of the grid-side current is improved and the THD is reduced to 8.31%.

Fig. 16 shows the THD of the grid current under different
Demonstrate that the odd harmonics can be reduced greatly with the overlap current constraining method and FFT analysis.THD appears at different load conditions and overlap times. A comparison of Figs. 15(a) and 15(b) shows the relationship of harmonic content under different DC currents in Fig. 16, where harmonic content increases linearly with overlap time and decreases with load currents, especially the low odd-order harmonic components. Fig. 17 shows the relationship between even order harmonics and overlap time, which indicates that even harmonics as a non-characteristic harmonic are independent of overlap time.

Fig. 18 shows the results with 10 μs overlap time and 8A loads when the overlap current constraining modulation is adopted. Compared with Fig. 15(a), THD decreases from 15.82% to 11.28%, especially the low-order odd harmonics. Moreover, the second harmonic decreases from 0.94% to 0.84%, and the fourth harmonic decreases from 0.31% to 0.29%. When the overlap time is 8 μs with the proposed modulation, the second harmonic increases from 0.79% to 0.81% and the fourth harmonic increases from 0.3% to 0.31%, which indicates that the overlap current constraining method has no influence on the even order harmonics.

Fig. 19 shows the relationship of THD with load current under different modulation methods. The THD of the grid-side current decreases with the increase of load current. The proposed modulation methods can improve the quality of the grid-side current, especially in light loads, which validates the effectiveness of the proposed modulation method.

In summary, the experimental results demonstrate that the overlap current would inject harmonics into the AC-side current, in which the low odd-order harmonics cannot be filtered by the LC filter and would worsen the grid-side current quality. The THD of the grid-side current increases with the overlap time because of the injection of the low odd order harmonics. The even harmonics are independent of the overlap time. The new modulation method can also restrain the overlap current in non-zero commutation and greatly reduce the odd harmonics. Notably, overlap time should also be reduced as much as possible to ensure the grid-side current harmonics meet the relevant standards better.

V. CONCLUSIONS

This paper presents an analysis of the causes and effects of overlap time during a modulation period. To improve the quality of the grid-side current, a new modulation method that combines positive-slope and negative-slope sawtooth carriers is proposed, which can restrain overlap current and improve the AC-side current quality. Simulation and experimental results demonstrate that the odd harmonics can be reduced greatly with the new modulation method.

The detailed conclusions are given as follows:

1) Overlap time brings extra harmonics to the AC-side current. The harmonics consist of low-frequency odd harmonics, which increase proportionally with the overlap time and
cannot be filtered by the LC filter.

2) When the positive and negative slope sawtooth waves are combined to act as the carrier, the new modulation method can effectively restrain the low-frequency current harmonics caused by the overlap time.

3) To ensure the AC-side current meets the relevant standards, in addition to adopting the overlap current harmonic suppression method, the overlap time must also be kept as short as possible.

ACKNOWLEDGMENT

This work is supported by the National Natural Science Foundation of China (51677089) and the Fundamental Research Funds for the Central Universities (NO. NJ20160047 and NO. NS2015039). The authors also appreciate the support of the Foundation of Graduate Innovation Center in NUAA (kjj20170308).

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