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비정현 계통 전압하에서 단상 인버터의 PLL 성능 개선 방법

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A Method to Improve the Performance of Phase-Locked Loop (PLL) for a Single-Phase Inverter Under the Non-Sinusoidal Grid Voltage Conditions

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Abstract

The phase-locked loop (PLL) is widely used in grid-tie inverter applications to achieve a synchronization between the inverter and the grid. However, its performance deteriorates when the grid voltage is not purely sinusoidal due to the harmonics and the frequency deviation. Therefore, a high-performance PLL must be designed for single-phase inverter applications to guarantee the quality of the inverter output. This paper proposes a simple method that can improve the performance of the PLL for the single-phase inverter under a non-sinusoidal grid voltage condition. The proposed PLL can accurately estimate the fundamental frequency and theta component of the grid voltage even in the presence of harmonic components. In addition, its transient response is fast enough to track a grid voltage within two cycles of the fundamental frequency. The effectiveness of the proposed PLL is confirmed through the PSIM simulation and experiments.

Key words: SRF-PLL(Synchronous Frame PLL), PLL(Phase Lock Loop), Synchronization, Single phase grid-tie inverter

1. Introduction

Grid connected power electronic systems such as Flexible AC Transmission Systems(FACTS), distributed power generation systems and power quality conditioners should be able to synchronize with the grid for the power transfer[1]-[5]. However, the grid voltage is not purely sinusoidal due to the presence of harmonics. Therefore the grid-tie inverter should have a capability to track the grid voltage with an acceptable amount of error even under the worst case of utility condition. Various kinds of synchronization techniques for the grid-tie inverters have been used to obtain the required performance under the non-sinusoidal grid condition such as Discrete Fourier Transforms (DFTs)[6], Adaptive Notch Filters(ANFs)[7], Zero-crossing -detection based methods[8], Kalman filtering techniques[9] and Phase-locked loops(PLLs)[10]. Among them the PLL technique is one of the most widely accepted synchronization techniques due to their simplicity, robustness and effectiveness.

The PLL technique is a closed loop system which synchronize the output signal to its reference signal in terms of frequency and phase. A typical PLL system is composed of three distinct parts: a Phase Detector(PD), a Loop Filter(LF) and a Voltage-Controlled Oscillator(VCO) as shown in Fig. 1. The function of PD is to compare the input grid voltage with the estimated output voltage of the PLL to provide the phase error. Then, this information is transferred to the LF to reduce the phase error to zero in the steady state. The VCO is a resettable integrator which resets the estimated theta(θ') to zero when it reaches 2π.

In three phase grid connected system the synchronous reference frame(SRF) based PLL has become the

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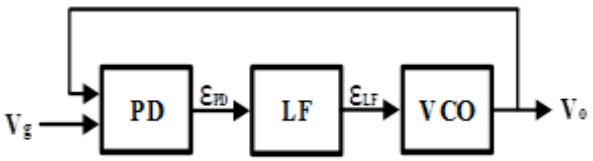

Fig. 1. Block diagram of a typical PLL.

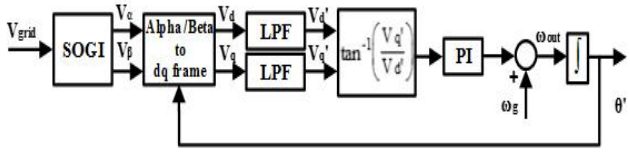

Fig. 2. Schematic diagram of proposed SOGI LPF SRF PLL.

most common and attractive technique due to its superiority in terms of performance[11]. However, it becomes more complex if applied to the single phase system since the information obtained from the grid is less than that of the three phase system[12],[13]. Thus, in order to generate the orthogonal signal from the single phase grid voltage some kind of additional technique should be employed.

One simple way to implement the Orthogonal Single Generator(OSG) is to use a transfer delay block[14]. This technique gives satisfactory performance when the grid voltage is purely sinusoidal. However, the output signal of OSG will not be exactly orthogonal when the grid frequency varies, hence it leads to an error in the estimated phase and frequency. Since the method provides no filtering capability, it is not suitable for the system operating under non-sinusoidal grid voltage condition. A new method of which name is Hilbert transformation(HT) is proposed to generate an OSG[15] In this method the type-3 Finite Impulse Response(FIR) filter is employed to generate the fictitious orthogonal signals. Though it provides satisfactory results under ideal conditions, it has two main drawbacks such as the unreliable performance under the frequency variation and the high computational burden[16],[17]. In[18], OSG is generated by differentiating the original signal. However, the main drawback of this approach is the high susceptibility to the noise due to the derivative function. The All Pass Filter(APF) technique is another method to generate the OSG[19]. Though it works fine under the sinusoidal grid condition, high rate of variations in frequency and phase are inevitable since it provides no attenuation or filtering for the harmonic components.

In order to overcome the above mentioned drawbacks such as frequency dependency, complexity and poor harmonic attenuation the Second Order Generalized Integrator(SOGI) based PLL have been proposed[20]. It has received much attention owing to its simplicity in digital implementation, low computational burden, good attenuation and satisfactory performance under frequency variation. The SOGI provide satisfactory performance when the grid voltage is sinusoidal. However it shows a variation in estimated frequency and phase since it is not able to provide enough attenuation under non sinusoidal grid voltage.

In this paper a SOGI based Low Pass Filter Synchronous Reference Frame Phase Locked Loop(LPF SRF-PLL) is proposed. In this proposed scheme the LPF is applied to the output of the Park's transformation block to provide more attenuation to the harmonic components. Due to the function of LPF the proposed PLL can estimate the frequency and phase more accurately under the presence of the harmonics in the grid voltage. Furthermore, its transient response is fast enough to track the grid voltage with in two cycles.

The paper is organized as follows. An overview of the proposed SOGI LPF PLL under sinusoidal and non-sinusoidal grid voltage conditions is presented in section 2. In section 3 implementation of the proposed PLL is detailed. In section 4 and 5 simulation and experimental results are presented and the performance comparison is completed. Finally, the performances of APF, conventional SOGI and the proposed SOGI LPF SRF PLL under sinusoidal and non-sinusoidal grid conditions are compared and the conclusion is given in section 6.

2. Proposed SOGI LPF SRF-PLL Under Sinusoidal and Non-Sinusoidal Grid Voltage Conditions

Fig. 2 shows the schematic diagram of the proposed single phase SOGI SRF-PLL, the SOGI generates virtual signals, V_α which has the same phase and magnitude as the fundamental of the grid voltage signal V_{grid} and V_β with a phase shift of 90 degree. The closed-loop Transfer Function(TF) of the SOGI based Quadrature Signal Generator(QSG) can be expressed as Eq. (1) and Eq. (2).

$$H_d(s) = \frac{v'}{v}(s) = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} \quad (1)$$

$$H_q(s) = \frac{qv'}{v}(s) = \frac{k\omega_n^2}{s^2 + k\omega_n s + \omega_n^2} \quad (2)$$

Where ω_n represents the resonant angular frequency i.e. $2\pi 60$ and k is the damping coefficient. $H_d(s)$ and $H_q(s)$ is the TF of the band pass filter(BPF) and the low pass filter(LPF), respectively. $H_q(s)$ shows a 90 degree phase shift with respect to $H_d(s)$ at ω_n.

The SOGI method has some advantages in creating the orthogonal signal as compared to the other conventional methods such as the Transport-Delay, Hilbert Transformation and All Pass Filter(APF). As shown in Fig. 3 it has a simple structure and a powerful characteristics to synchronize with the reference signal.

The bode plots of the closed-loop transfer functions $H_d(s)$ and $H_q(s)$ with different damping factors(k) are shown in Fig. 4. It can be observed from Fig. 4 that the higher attenuation can be obtained by decreasing the k gain but the dynamic response of the system gets worse. Fig. 5 shows the dynamic response of the $H_d(s)$ when the step command is given at t=0. The optimal value of k used for the simulation and experiments is 1.2, which provides a suitable attenuation and a suitable dynamic response as well.

The orthogonal signals V_α and V_β generated by SOGI with grid voltage V_{grid} is shown in Fig. 6. Once the orthogonal signal is generated then the park transformation is used to detect the d and q components in the rotating reference frame. The OSG is expressed as.

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \begin{bmatrix} V_m \cos\theta_g \\ V_m \sin\theta_g \end{bmatrix} \quad (3)$$

Where, V_m is the peak grid voltage, θ_g is the grid phase angle. The synchronous dq-axis voltage V_d and V_q can be obtained as followings.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta' & \sin\theta' \\ -\sin\theta' & \cos\theta' \end{bmatrix} \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m \cos\theta' \cos\theta_g + V_m \sin\theta' \sin\theta_g \\ -V_m \sin\theta' \cos\theta_g + V_m \cos\theta' \sin\theta_g \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} V_m \cos(\triangle\theta) \\ V_m \sin(\triangle\theta) \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} \approx \begin{bmatrix} V_m \\ V_m \triangle\theta \end{bmatrix} \quad (7)$$

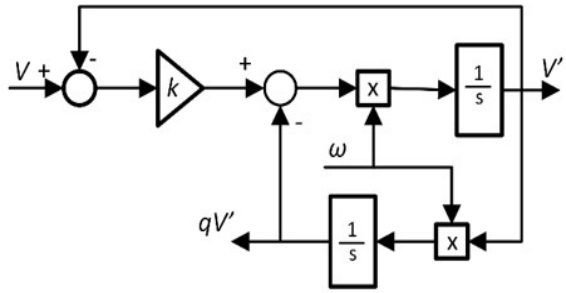

Fig. 3. Typical structure of the SOGI.

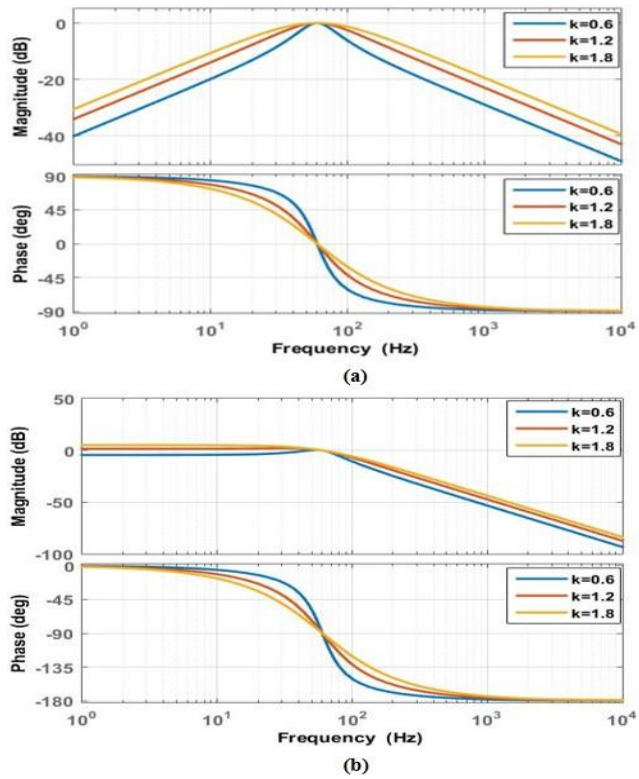

Fig. 4. Bode plots of SOGI with different damping factors. (a) H_d. (b) H_q.

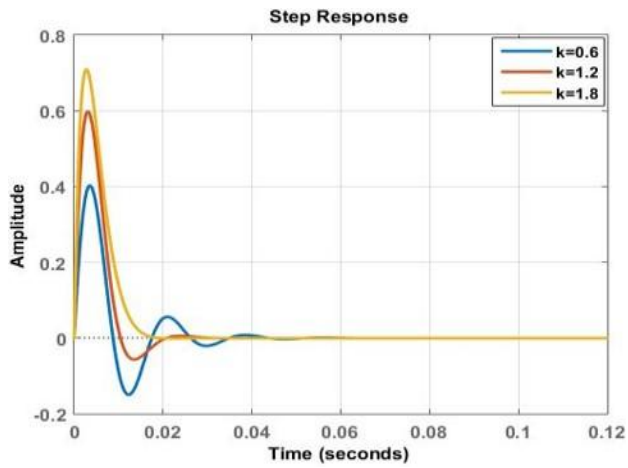

Fig. 5. Step response of $H_d(s)$ transfer function according to different K values.

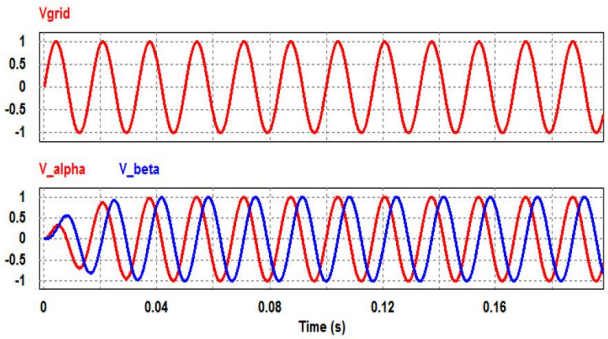

Fig. 6. Virtual signals generated by SOGI. (a) grid voltage. (b) V_α and V_β.

Where θ' is the estimated phase angle or locked phase angle and $\triangle\theta = \theta_g - \theta'$ is the locked phase error between the grid angle and the estimated phase angle. Since the locked phase error $\triangle\theta$ is very small in the steady state, Eq. (6) can be re-written as Eq. (7). It can be realized from Eq. (7) that V_q gives the locked phase error information and it is possible to make it zero at the steady state by using a LF that is actually a PI controller.

Though the PLL provides the satisfactory performances under the sinusoidal grid voltage condition, the most challenging issue associated with the PLL is its accuracy and speed to estimate the frequency and phase when the grid is non-sinusoidal condition due to the presence of the harmonics. In order to improve the filtering capability under the non-sinusoidal grid condition, the proposed PLL employs LPF to filter out the harmonics from two phase signals V_d and V_q. In the proposed scheme the LPF is applied to the output of the Park's transformation block to provide more attenuation to the harmonic components. Due to the function of the LPF the proposed PLL can estimate the frequency and phase more accurately under the presence of the harmonics. The proposed system employs the following first-order low-pass filter as shown in Eq. (8).

$$G_l(s) = \frac{\omega_c}{s+\omega_c} \tag{8}$$

Where ω_c is a cut-off angular frequency of the filter. The cut-off frequency of LPF is 35Hz, It is selected to get the optimal performance in terms of the harmonic attenuation and the dynamic response.

The dynamic response of the proposed PLL under sinusoidal and non-sinusoidal condition is shown in Fig. 7(a). The system starts with sinusoidal grid

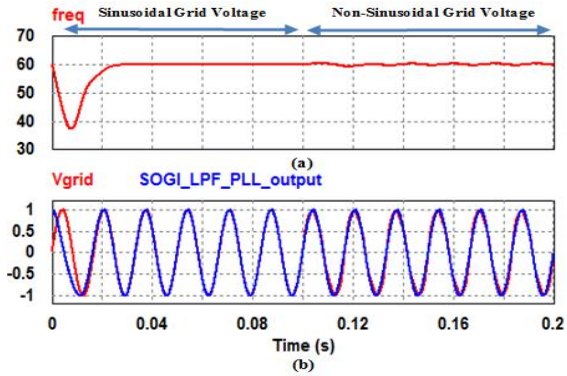

Fig. 7. Dynamic response of the proposed PLL. (a) Estimated frequency response. (b) Output response.

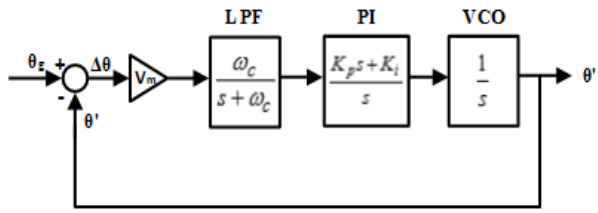

Fig. 8. Control block diagram of the proposed PLL.

condition up to 0.1s and then the non-sinusoidal grid voltage condition is applied. The proposed PLL shows a good dynamic characteristics and its transient response is fast enough to track the grid voltage within two cycles as shown in Fig. 7(b).

3. Implementation of the Proposed SOGI LPF SRF-PLL

In this section the implementation of proposed PLL is detailed. At first the TFs of the analog filters are transformed by using the trapezoidal approximation for the discrete implementation of OSG based SOGI. By using a discrete time operator Eq. (1) and Eq. (2) can be re-written as Eq. (9) and Eq. (10), respectively.

$$H_d(z) = \frac{(2k\omega_n T_s)(z^2-1)}{4(z-1)^2+(2k\omega_n T_s)(z^2-1)+(\omega_n T_s)^2(z+1)^2} \tag{9}$$

Similarly,

$$H_q(z) = \frac{k(\omega_n T_s)^2(z^2+1)^2}{4(z-1)^2+(2k\omega_n T_s)(z^2-1)+(\omega_n T_s)^2(z+1)^2} \tag{10}$$

The control block diagram of the proposed SOGI LPF SRF PLL is shown in Fig. 8. Therefore the open loop transfer function of the proposed PLL can be represented by using Eq (11).

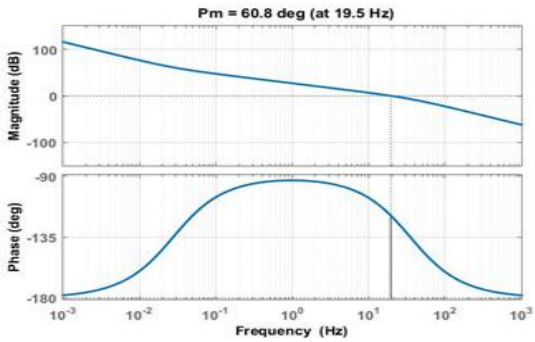

Fig. 9. Bode plot of the open-loop TF of the proposed SOGI LPF SRF.

$$\begin{aligned} G_{ol}(s) &= V_m \times LPF \times PI \times Plant \\ &= V_m \times \left(\frac{\omega_c}{s+\omega_c}\right) \times \left(\frac{K_P s + K_i}{s}\right) \times \left(\frac{1}{s}\right) \\ &= V_m \times \left(\frac{K_p \omega_c s + K_i \omega_c}{s^3 + \omega_c s^2}\right) \end{aligned} \quad (11)$$

Where $G_{ol}(s)$ is the open loop TF, K_p is proportional gain and K_i is the integral gain of the PI controller. Therefore the closed loop transfer function $G_d(s)$ can be expressed by using Eq (11) as Eq (12).

$$G_d(s) = \frac{G_{ol}(s)}{1+G_{ol}(s)} = \frac{V_m(K_p\omega_c s + K_i\omega_c)}{s^3 + \omega_c s^2 + V_m(K_p\omega_c s + K_i\omega_c)} \quad (12)$$

The PI controller is designed to have an enough bandwidth and phase and gain margins by using the SISOTOOL in MATLAB software. The bode plot of the open-loop TF of the proposed SOGI LPF SRF PLL designed is shown in Fig. 9. The parameters K_p and K_i are chosen to be 140.0 and 24.3, respectively. The phase margin(PM) is 60.7° at 19.5 Hz, which is good enough to ensure the stability of the system.

4. Simulation Results

In order to compare the performance of the proposed method to the other conventional methods such as APF SRF and SOGI SRF PSIM simulations are conducted. All three PLL algorithms have been implemented for the performance comparison and the results are compared under sinusoidal and non-sinusoidal grid voltage conditions. At the beginning of the simulation the performance of the proposed PLL method is tested under the sinusoidal grid voltage condition and the 2nd, 3rd and 5th harmonic of which

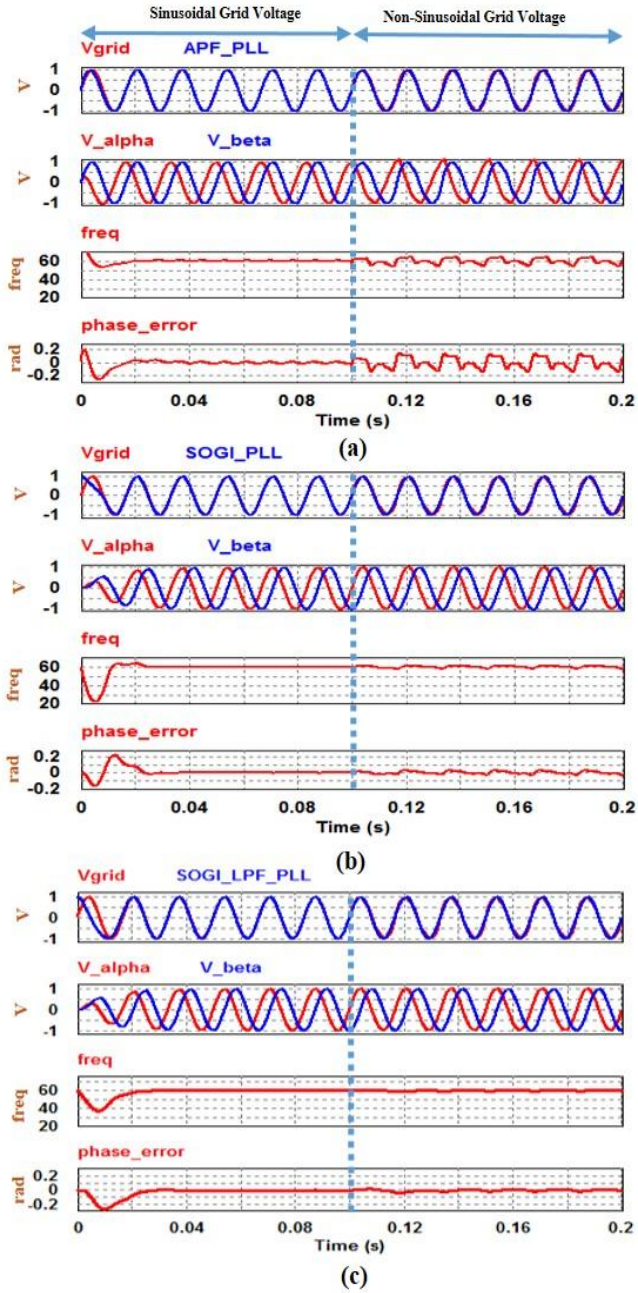

Fig. 10. Simulation results of each method for the performance comparison. (a) APF SRF PLL. (b) SOGI SRF PLL. (c) SOGI LPF PLL.

amplitudes are 10%, 6% and 3% of the fundamental components are added to make non-sinusoidal grid voltage condition after 0.1sec. The simulation results of three PLL algorithms are shown in Fig. 10. It can be observed from the waveforms that the frequency variations of APF SRF PLL, SOGI SRF PLL and the proposed PLL under the sinusoidal grid voltage conditions are 1.0, 0.17 and 0.03 Hz, respectively and the phase errors are 1.56, 0.21 and 0.07 degree, respectively.

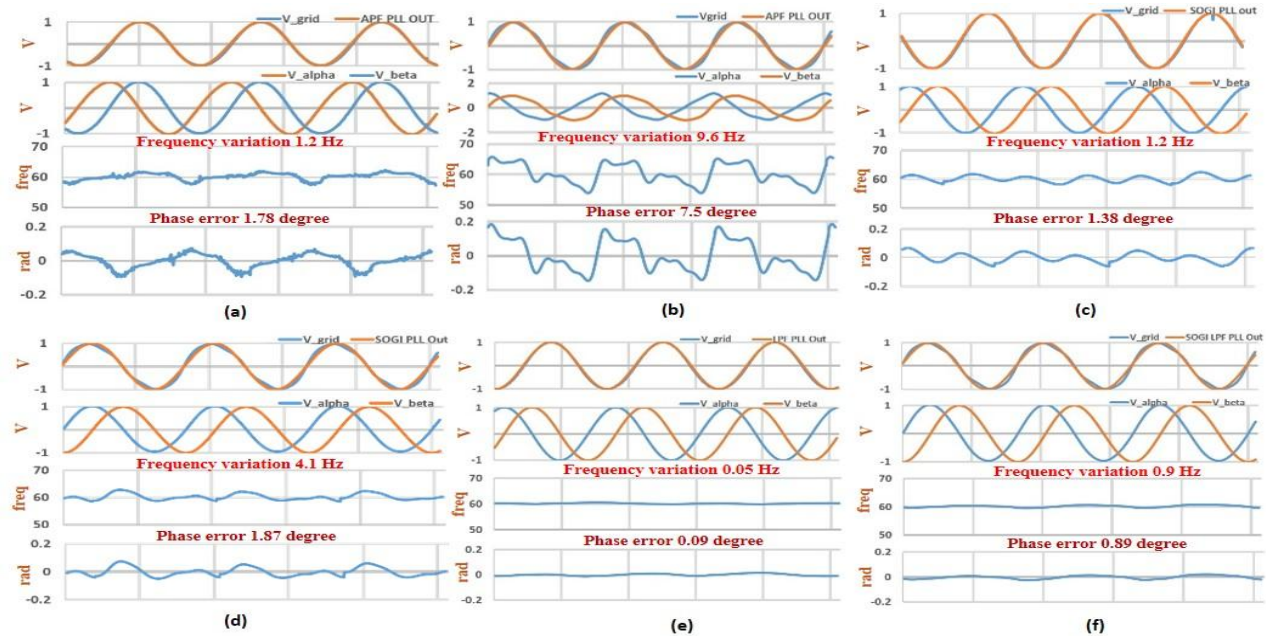

Fig. 11. Experimental results. (a) APF SRF PLL under sinusoidal grid condition. (b) APF SRF PLL under non sinusoidal grid condition. (c) SOGI SRF PLL under sinusoidal grid condition. (d) SOGI SRF PLL under non sinusoidal grid condition. (e) SOGI LPF SRF PLL under sinusoidal grid condition. (f) SOGI LPF SRF PLL under non sinusoidal grid condition.

Under the non-sinusoidal grid voltage conditions the frequency variations of APF SRF PLL, SOGI SRF PLL and the proposed PLL are 9.1, 3.8, 0.8 Hz, respectively, and the phase errors are 6.84, 1.64 and 0.75 degree, respectively. In the mean time the settling times of APF, SOGI and the proposed PLL are 22, 26 and 30ms, respectively. The proposed PLL took longer time than others to settle due to the addition of LPF which increases the settling time. However, it is still good enough to track the grid voltage within 2 cycles of the grid voltage. Compared to the conventional APF and SOGI SRF PLL, the proposed PLL is able to accurately estimate the fundamental frequency and phase of the grid voltage even in the presence of harmonic components.

5. Experimental Results

In order to prove the validity of the proposed algorithm it is implemented in a digital signal processor, TMS320F28335 from Texas Instruments. The experimental results of three PLL algorithms are shown in Fig. 11 including input grid voltage(V_{grid}) with PLL output, virtual signal V_α and V_β, estimated frequency(f_{req}) and phase error $\theta_g - \theta'$, respectively.

Fig 11. shows the experimental results under the sinusoidal grid voltage conditions. The frequency variations of APF SRF PLL, SOGI SRF PLL and proposed PLL are 1.21, 1.2, 0.05 Hz, respectively and the phase errors are 1.78, 1.38 and 0.09 degree, respectively. Under non-sinusoidal grid voltage conditions, however, the frequency variations of APF SRF PLL, SOGI SRF PLL and proposed PLL are 9.6, 4.1, 0.9 Hz respectively and the phase errors are 7.5, 1.87 and 0.89 degree, respectively.

Fig. 12 shows the performance comparison of APF SRF PLL, SOGI SRF PLL and proposed PLL under non-sinusoidal grid voltage conditions in terms of frequency variation

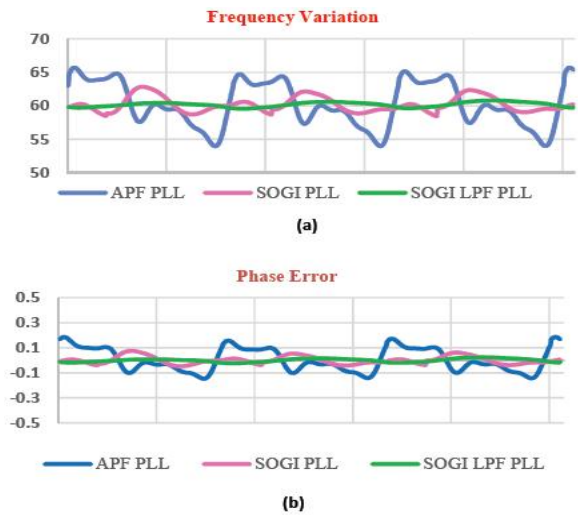

Fig. 12. Performance comparison of APF SRF PLL, SOGI SRF PLL and proposed PLL under non-sinusoidal grid voltage conditions.

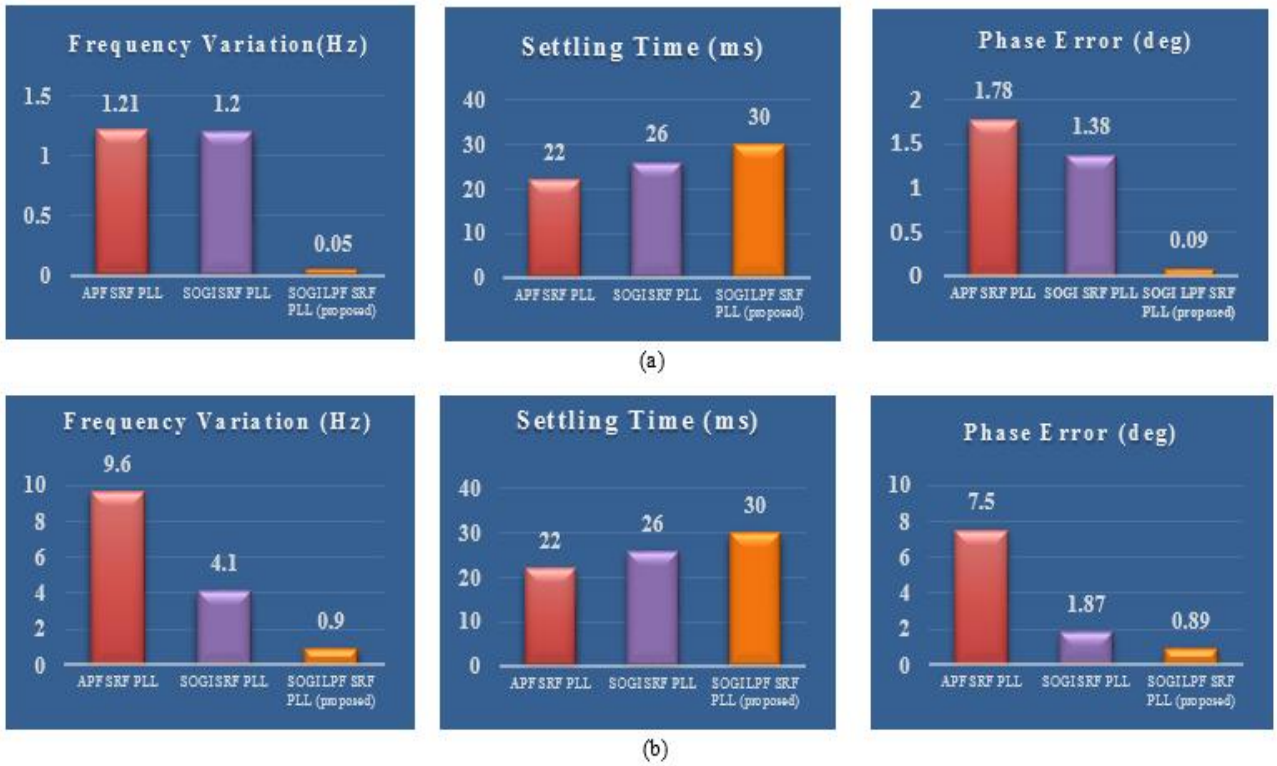

Fig. 13. Comparison of three PLL algorithms in terms of frequency variation, settling time and phase error. (a) under sinusoidal voltage condition. (b) under non-sinusoidal grid voltage condition.

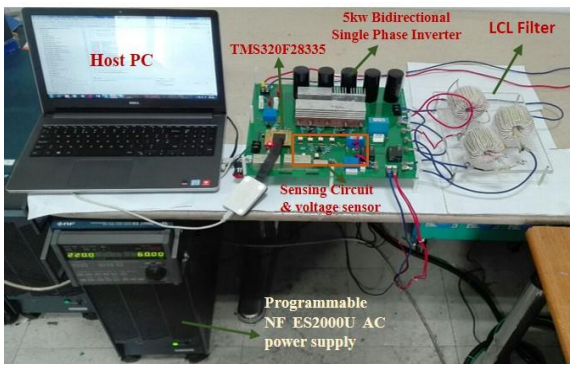

Fig. 14. Experimental setup of the 5kW single phase inverter for the PLL performance test.

TABLE I
RESULTS SUMMARY FOR THREE PLL METHODS UNDER SINUSOIDAL GRID VOLTAGE CONDITION

TECHNI-QUES	FREQUENCY VARIATION (Hz)		STEADY STATE TIME(s)	PHASE ERROR (deg)		CONDITIONS
	SIM.	EXP.		SIM.	EXP.	
APF SRF PLL	1.0	1.21	22ms	1.56	1.78	Kp=222.1,Ki=25181
SOGI SRF PLL	0.17	1.2	26ms	0.21	1.38	Kp=330, Ki=68759
SOGI SRF LPF PLL	0.03	0.05	30ms	0.07	0.09	Kp=140,Ki=24.3 LPF cut-off freq. 35 Hz

TABLE II
RESULT SUMMARY FOR THREE PLL METHODS UNDER NON-SINUSOIDAL GRID VOLTAGE CONDITION

TECHNI QUES	FREQUENCY VARIATION (Hz)		STEADY STATE TIME(s)	PHASE ERROR (deg)		CONDITIONS
	SIM.	EXP.		SIM.	EXP.	
APF SRF PLL	9.1	9.6	22ms	6.84	7.5	Kp=222.1, Ki=25181 2nd,3rd,5th grid harmonic
SOGI SRF PLL	3.8	4.1	26ms	1.64	1.87	Kp=330, Ki=68759 2nd,3rd,5th grid harmonic
SOGI LPF SRF PLL	0.8	0.9	30ms	0.730	0.89	Kp=140,Ki=24.3 LPF cutt-off freq. 35 Hz 2nd,3rd,5th grid harmonic

and phase error. As shown in the Fig. 11 the proposed PLL shows minimum frequency variation and phase error even in the presence of harmonic components. Table 1 and 2 show the comparison in terms of main performance indices such as transient time, frequency variation and phase errors under sinusoidal and non-sinusoidal grid voltage condition. The results obtained by the simulation and experiments are shown together for the comparison. Fig. 13 shows the Graphical comparison of three PLL

algorithm responses under sinusoidal and non-sinusoidal grid voltage condition. The experimental setup is shown in Fig. 14.

6. Conclusion

In this paper, a method to improve the performance of the PLL for single phase inverter has been proposed and its effectiveness has been verified through simulation and experiments. The performances of the three kinds of different PLL techniques are compared under the sinusoidal and non-sinusoidal grid voltage conditions through the simulation and experiments. It has been proved that the proposed technique is superior than other techniques in terms of frequency variation and phase error.

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