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All-optical Integrated Parity Generator and Checker Using an SOA-based Optical Tree Architecture

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The Semiconductor Optical Amplifier (SOA)-based Mach-Zehnder interferometer is a major contributor in all-optical digital processing and optical computation. Optical tree architecture provides one of the new, alternative schemes for integrated all-optical arithmetic and logical operations. In this paper, we propose an all-optical 3-bit integrated parity generator and checker using SOA-MZI-based optical tree architecture. The proposed scheme, able to process input signals at a desired operating wavelength, has been characterized using RZ-modulated signals at 10 Gbps. The maximum extinction ratios achieved at the output of the parity generator and checker are 10 dB and 8 dB respectively.

Keywords : Semiconductor optical amplifier (SOA), SOA-MZI, Parity generator, Parity checker, Optical tree architecture (OTA), Optical computing
OCIS codes : (060.1155) All-optical networks; (060.1810) Buffers, couplers, routers, switches and multiplexers; (060.2320) Fiber optics amplifiers and oscillators

I. INTRODUCTION

The data communication industry demands a major increase in the bandwidth of the transmission channel. Electronic systems are not capable of processing a large amount of data at high frequencies (above GHz), but this limitation can be overcome if the traditionally used electrons are replaced by photons, for digital circuits based on switching and data processing [1, 2].

Many distinct techniques have been proposed to implement all-optical digital devices using nonlinear effects in either optical fiber or a semiconductor optical amplifier (SOA). Compared to the nonlinearity of optical fiber, SOA-based all-optical switches exhibit tremendous performance in terms of low power consumption, optical integration, and high speed [3, 4]. Out of the different types of all-optical switches that are used to design combinational circuits, the SOA-based Mach-Zehnder Interferometer (SOA-MZI) has been widely preferred, due to its fast operational speed and easy integration with active and passive components [5-7].

In optical computing, the optical interconnecting systems are the primary elements constituting various architectures and algorithms. Optical tree architecture (OTA) plays a significant role in optical interconnecting networks, and SOA-MZI-based OTA can be used to realize all-optical digital devices by selection of the suitable branch of the tree [8].

To verify the integrity of recovered digital data, parity generation and checking has been the most widely used method in digital communication systems. A parity-generator circuit plays an important role in analyzing the discrepancy between transmitted and received bit patterns simultaneously. A parity bit is included in the binary message, which is sent from the transmitting end and then checked for errors at the receiving end. If the received bits do not correspond to the transmitted bits, error is detected. A parity-checker circuit thus contributes by checking for errors in the number of bits transmitted and received, and therefore is used in data computing systems [9].

Poustie *et al*. reported an all-optical parity checker with

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optical memory, where input is given bit by bit in a repeated pattern [10]. Subsequently, different schemes for parity generation and checking have been proposed using other techniques [11-17]. Dimitriadou *et al*. proposed a parity generator and checker using a quantum-dot semiconductor optical amplifier (QD-SOA)-based Mach-Zehnder Interferometer (MZI) [11]. A parity generator and checker circuit has also been proposed using a polarization-encoded light signal in [12]. In 2016, Kumar *et al*. demonstrated an even-bit parity checker and optical gray-code converter employing the electro-optic effect in a lithium niobate-based MZI, which experienced the disadvantage of high insertion loss [13].

In the parity checker where a bit-by-bit repeated pattern has been employed to provide the input, the round-trip delay across the device increases the time-of-flight latency of the output [14]. The operation of devices based on encoded light signals depends purely on the intensities of optical beams. Polarization-encoded and optically encoded techniques have limited use, as it is difficult to maintain the threshold intensity of the data signals in long-haul communication.

Interferometric gates based on MZIs using SOAs have shown tremendous advantages, due to their fast switching activity and ability to integrate with active and passive devices, which results in low power consumption and higher stability [18-20]. The optical tree architecture provides one of the new, alternative schemes for computation of all-optical arithmetic and logical operations [21].

In this paper, we propose an all-optical 3-bit integrated parity generator and checker using an SOA-MZI-based optical tree architecture. The proposed architecture can operate as a parity generator as well as a checker, depending upon the value of the parity bit. The output from the parity generator is given directly to the parity checker, without requiring any extra input terminal for generation of the parity bit. Numerical simulation confirming the described logic devices has been performed at 10 Gbps using RZ-modulated signals. As the device utilizes SOA-based MZI switches, it is apt for integrated solutions.

II. TREE ARCHITECTURE FOR ALL-OPTICAL 3-BIT PARITY GENERATOR AND CHECKER

The basic theory for the design is similar to that for the conventional parity generator and checker designed in the electronic domain. The truth table of the even-parity circuit, without and with error, is shown in Tables 1(a) and 1(b) respectively. The output from the parity generator is directly given as an input to the parity checker, and hence no additional bits are required for parity-generator output. When the number of 1's in a particular row is odd, the parity bit generated is '1' (in the case of even parity), and when the number of 1's is even, the parity bit generated is '0'. Thus when the parity bit generated is passed along with the rest of the bits through the communication channel, the number of 1's at the receiving end remains even, which shows that the information received is correct, and the parity checker gives '0' at its output. When the number of 1's received is odd, an error is detected, and the parity checker gives '1' at its output.

TABLE 1. Truth table for the 3-bit parity generator and checker, without error

(a)

A	B	C	Parity bit (P)	Parity checker
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

(b)

A	B	C	Parity bit (P)	Parity checker
0	0	0	0	0
1	0	1	1	1 (error)
0	1	1	1	1 (error)
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	0

The Boolean expression for the parity generator and checker can be expressed as:

$$\text{P (Parity Generator)} = \text{A XOR B XOR C} = \overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$$

$$\text{Parity Checker} = \text{A XOR B XOR C XOR P} = \overline{A}\overline{B}\overline{C}P + \overline{A}B\overline{C}\overline{P} + A\overline{B}\overline{C}\overline{P} + ABCP + A\overline{B}CP + AB\overline{C}P + \overline{A}BCP$$

This all-optical 3-bit integrated parity generator and checker uses OTA architecture, which comprises SOA-based MZI optical switches. A single SOA-based MZI optical switch is shown in Fig. 1. In this switch, two identical SOAs are placed, between two couplers, one connected to the incoming signal λ_1 and the other connected to pulsed light of different wavelength λ_2.The pulsed light acts as a control signal. The presence or absence of this signal alters the performance of the switch. The basic mechanism used for the behavior is cross-phase modulation (XPM). Due to the gain saturation developed by the pulsed light λ_2, the carrier density is reduced in one SOA, which further

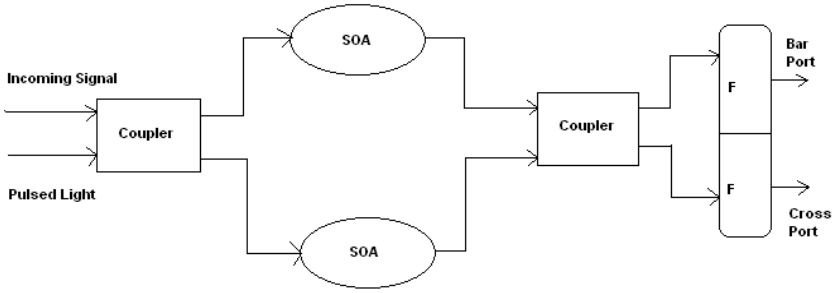


FIG. 1. SOA-based MZI optical switch.

increases the refractive index in the arm through which the λ_2 signal passes. As a result, the incoming signal λ_1 goes through an additional phase shift π because of the XPM, and the λ_1 beam starts moving toward the bar port for each number of 1's in the input signal. Thus when the pulsed light λ_2 is absent, the signal passes through the cross port and light is not present in the bar port. When the pulsed light λ_2 and incoming signal λ_1 are both present, the signal passes through the bar port.

The proposed 3-bit all-optical integrated parity generator and checker using OTA is shown in Fig. 2. There are three input signals: A, B, and C.

The output of the parity generator is directly fed to the parity-checker circuit, without any requirement of a fourth input P. The design consists of 15 SOA-based MZI optical switches, where each switch has a high or low output, depending on the presence or absence of input signals A, B, and C respectively.

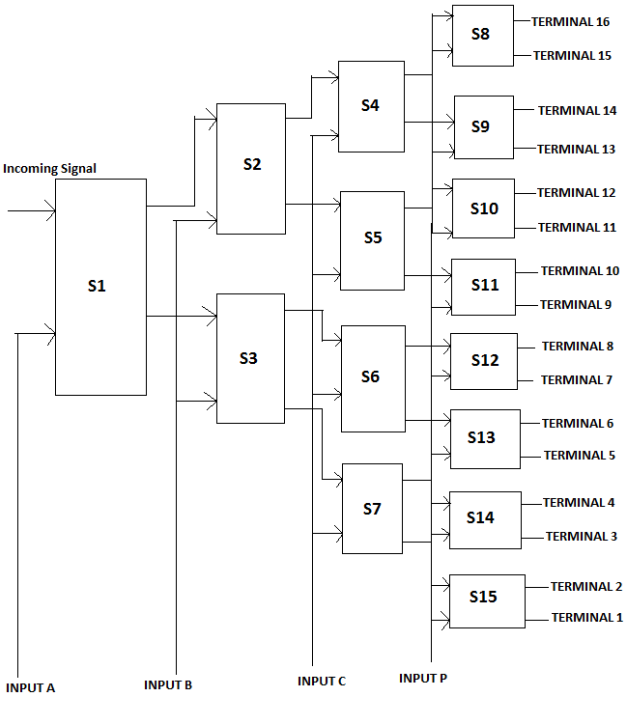


FIG. 2. Schematic of the all-optical 3-bit integrated parity generator and checker using OTA.

The different output states of parity generator and checker for different input combinations, without error and with error, are shown in Tables 2 and 3 respectively.

Table 2 shows the output states at the different terminals when different input combinations are applied to the proposed architecture. When the input bit combination communicated through the channel along with the parity bit is correct, the parity checker terminals each have no error at the output, and this is shown in the form of the '0' state.

Similarly, Table 3 shows the output states of the different terminals when different input combinations are applied to the proposed architecture. When the input bit combination communicated through the channel along with the parity bit shows some error at the receiver terminal, the parity checker terminal turns its output from 0 to 1, which is shown for the cases of two input combinations in Table 3.

Based on different input bit combinations, the output is obtained from terminal 1 to terminal 16 respectively. The four cases in which the parity bit is high are described as follows.

Case 1: When input A = 0, B = 0, and C = 1, the first switch S1 becomes active and produces high output from its cross-port terminal. This activates switch S3, and high output is generated from the cross port of this switch. In the same manner the signal is passed through the bar ports of switches S7 and S15, thus giving the output at terminal 4 of the parity generator and checker.

Case 2: Similarly, when input A = 0, B = 1, and C = 0, the first switch S1 becomes active and produces high output from its cross-port terminal. This further activates switch S3, and high output is generated from the bar port of this switch. In the same manner the signal is passed through the cross port and bar port of switches S6 and S13 respectively, thus giving the output at terminal 6 of the parity generator and checker.

Case 3: When input A = 1, B = 0, and C = 0, the first switch S1 becomes active and produces high output from its bar port terminal. This activates switch S2, and high output is generated from the cross port of this switch. In the same manner the signal is passed through the cross ports of switches S5 and S11, thus giving the output at terminal 10 of the parity generator and checker.

Case 4: Likewise, when input A = 1, B = 1, and C = 1, the first switch S1 becomes active and produces high

TABLE 2. Output states of the parity generator and checker, without error

Input				Output states for different input combinations															
				Output terminals															
A	B	C	P	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TABLE 3. Output states of the parity generator and checker, with error

Input				Output states for different input combinations															
				Output terminals															
A	B	C	P	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	1 (error)	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	1 (error)	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

output from its bar port terminal. This further activates switch S2, and high output is generated from the bar port of this switch. In the same manner the signal is passed through the bar ports of switches S4 and S8, thus giving the output at terminal 16 of the parity generator and checker. Likewise the output is obtained for different input combinations.

III. RESULTS AND DISCUSSIONS

This section describes the results obtained from the realization of an all-optical parity generator and checker using an SOA-based Mach-Zehnder interferometer. The operation of the device has been verified for different input combinations, confirming the successful operation of the circuit.

3.1. Parity Generator and Checker, without Error

In the proposed model we have considered lasers for the incoming and control signals with wavelengths of 1550 and 1500 nm respectively. The lasers used have random phase, 10 full width at half maximum (FWHM) linewidth, ideal laser noise bandwidth, and 0 dBm continuous-wave power. Optical attenuators and amplifiers have been used at different points in the setup, to adjust the power levels of the signals. Simulation in Optisystem 15.0 for output waveforms has been performed using RZ-modulated signals, at a data rate of 10 Gb/s. The traveling-wave SOA has been used in the proposed model, with simulation parameters as shown in Table 4.

An input coupler with two SOAs plus an output coupler with a Gaussian filter form a single SOA switch. The

TABLE 4. Simulation parameters

S. No.	Parameters	Value
1	Injection current	150 mA
2	Amplifier length	500 μm
3	Active layer width	3 μm
4	Active layer thickness	0.8 μm
5	Optical confinement factor	0.3
6	Linewidth enhancement factor	5
7	Carrier density at transparency	1.4×10^{18} cm^{-3}

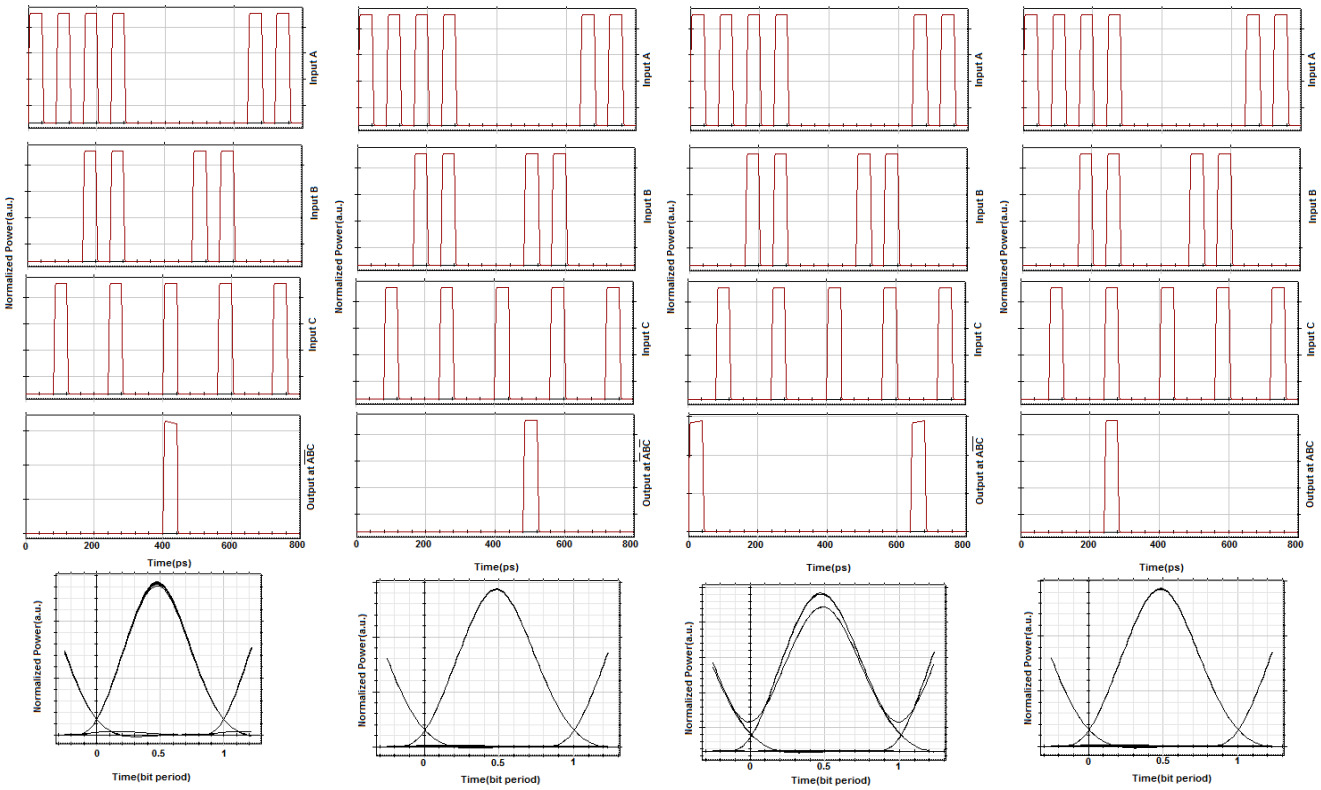


FIG. 3. Parity-generator output for four different input combinations: (a) $\overline{A}\overline{B}C$, (b) $\overline{A}B\overline{C}$, (c) $A\overline{B}\overline{C}$, and (d) ABC.

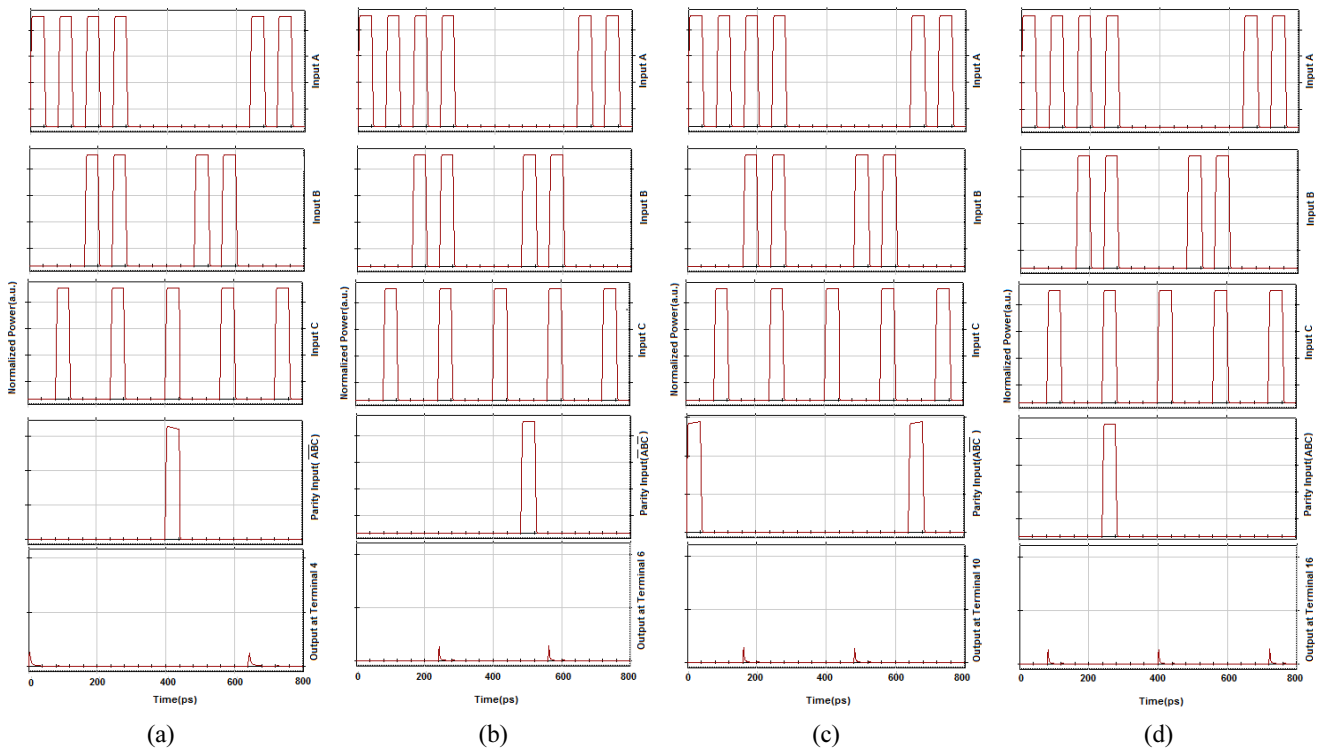


FIG. 4. Input and output waveforms of the parity checker, without error. Output at (a) terminal 4, (b) terminal 6, (c) terminal 10, and (d) terminal 16.

outputs of the first coupler are fed to the semiconductor optical amplifier. Outputs from each arm of the SOA are finally connected to an output optical coupler. The output coupler is further connected to a Gaussian filter, which blocks the pulsed light at the wavelength of 1500 nm. There are a total of 15 switches, and final outputs of the parity checker are obtained from terminals 1 to 16 respectively.

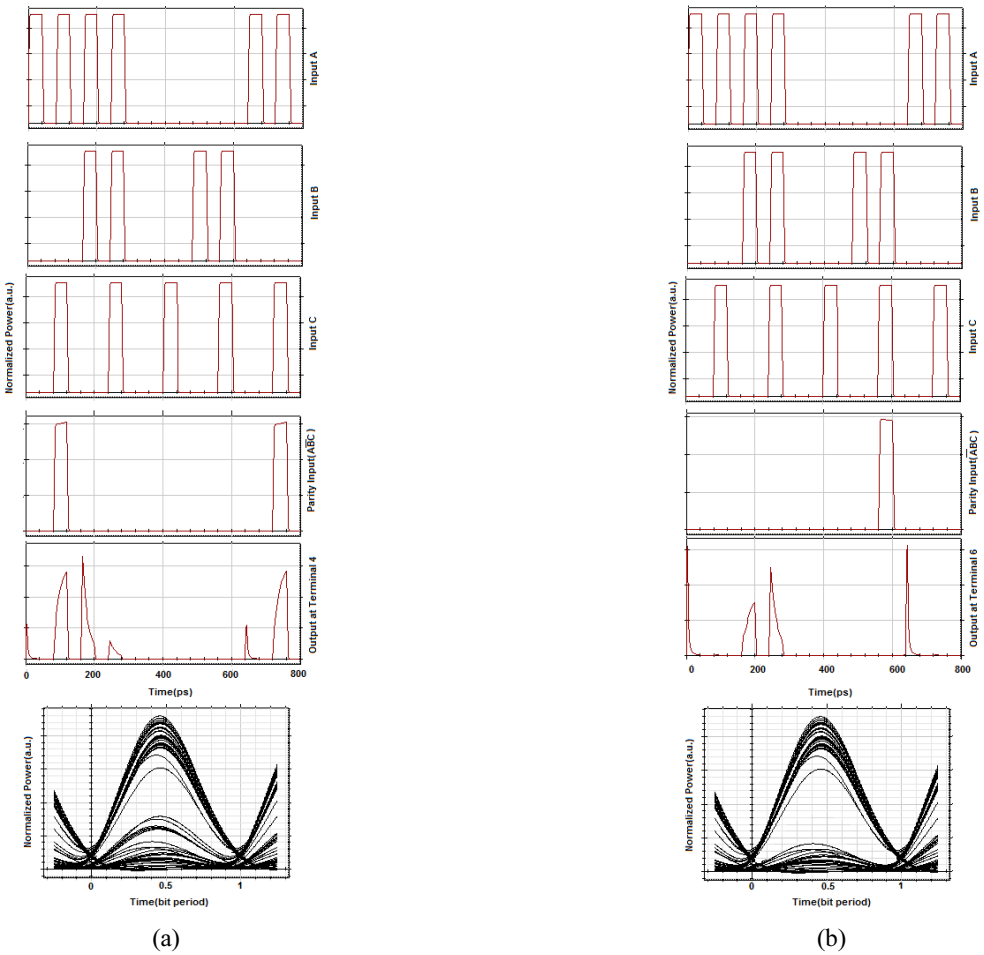
For a 3-bit parity generator, we need three input terminals A, B, and C and eight output terminals. Eight outputs are required to represent output parity bits for all possible input combinations. As shown in Table 1(a), in the parity-generator circuit, for the case of an odd number of 1's the parity bit is always high. The simulation timing diagrams have been obtained for the parity bit in the cases of input combinations $\overline{A}\overline{B}C$, $\overline{A}B\overline{C}$, $A\overline{B}\overline{C}$, and ABC respectively. Figure 3 shows the resulting input and output timing-diagram curves for the four input combinations, along with the eye diagrams of the outputs, for the situation when the parity bit is high. The extinction ratio of the signals generated at the output of the parity generator, when the parity bit is high, has been observed as above 10 dB.

For input combinations with an odd number of 1's, when all the bits are correctly received and there is no error in the bits, the parity checker gives '0' as the output. The simulation timing diagram has been obtained at the output of the parity checker in the cases of the four input combinations $\overline{A}\overline{B}C$, $\overline{A}B\overline{C}$, $A\overline{B}\overline{C}$, and ABC respectively. Figure 4 shows the output waveforms corresponding to the input combinations $\overline{A}\overline{B}C$, $\overline{A}B\overline{C}$, $A\overline{B}\overline{C}$, and ABC obtained at terminals 4, 6, 10, and 16 respectively.

3.2. Parity Generator and Checker, with Error

For input combinations with an even number of 1's, when all of the bits for a given combination are not correctly received and there is an error in the received bits, the parity checker gives '1' as the output. In the present case we consider the two input combinations $\overline{A}BC$ and $\overline{A}B\overline{C}$, for which there is an error at the output of the parity checker.

Instead of input combination $\overline{A}\overline{B}C$, if the received incoming bits are $A\overline{B}C$ and the parity bit remains unchanged, the logic output at terminal 4 flips from '0' to



(a) (b)

FIG. 5. Input and output waveforms of the parity checker, with error. Output (a) at terminal 4 when $A\overline{B}C$ input combination is given instead of $\overline{A}\overline{B}C$, and (b) at terminal 6 when $\overline{A}BC$ input combination is given instead of $\overline{A}B\overline{C}$.

'1', indicating an error at the output. Similarly, for the input combination $\overline{A}B\overline{C}$, if we receive the incoming bits as $\overline{A}BC$ and the parity bit remains the same, the output at terminal 6 flips from '0' to '1'. Figures 5(a) and 5(b) show the input and output timing diagrams, along with eye diagrams of the output signals, depicting error at the output of the parity checker for input combinations $\overline{A}\overline{B}C$ and $\overline{A}B\overline{C}$ at terminals 4 and 6 respectively. The extinction ratio of the signals at the output of the parity checker, in case of an error in the input bit combination, has been observed to be about 8 dB.

V. CONCLUSION

An optical 3- bit parity generator and checker has been proposed and realized, using an SOA-MZI-based optical tree architecture. The proposed scheme reduces the size of the device by taking the output parity bit from the parity generator and giving it as an input to the parity checker. It is able to process input signals at a desired wavelength, thus making it wavelength-independent. The maximum extinction ratios achieved at the output of the parity generator and checker are 10 dB and 8 dB respectively. As the device utilizes SOA-based MZI switches, it is apt for integrated solutions. Parity checking of a higher number of input bits may be achieved by cascading several SOA-based MZI switches, with proper selection of the tree and its suitable branches.

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