ISSN : 1226-7244 (Print)
ISSN : 2288-243X (Online)
논문번호 19-01-39

j.inst.Korean.electr.electron.eng.Vol.23,No.1,273~279,March 2019
http://dx.doi.org/10.7471/ikeee.2019.23.1.273

A Novel Negative-Output High Step-up Ratio DC-DC Converter Based on Switched-Inductor Cell

Ho-Yeon Kim*, Eun-A Moon*, Minh-Khai Nguyen**★

Abstract

A high boost dc-dc converter based on the switched-inductor cell (SL-cell) is suggested in this paper. The suggested converter can provide a high voltage gain that is more than 6. Moreover, the voltage gain can be easily increased by extending a SL cell or a modular voltage boost stage. This paper shows the key waveforms, the operating principles at the continuous conduction mode (CCM), and a comparison between the suggested converter and the other non-isolated converters. In addition, the extension of the suggested converter is presented. The simulation results were shown to reconfirm the theoretical analysis.

Key words : non-isolated dc-dc converter; high-voltage gain; switched-inductor; boost converter; continuous conduction mode

I. Introduction

Nowadays, we are facing pressure from environment protection and global surface temperature. The energy sources are depleting, hence the development of renewable energy is the most-effective solution. However, the available renewable energies such as wind power, solar cells, and fuel cells are dependent on the weather conditions, and their output voltages are low and instability. Thus, a high boost voltage conversion should be used to convert a low voltage to a high voltage for grid-connected inverter. The functional block diagram of the power-conversion system is shown in Fig. 1. A high boost dc-dc converter is used to convert a low voltage into a high voltage dc bus [1].

Fig. 1. Functional diagram of power-conversion system.

Many high boost dc-dc converters have been researched and obtained a high-voltage gain in both isolated and non-isolated topologies. For the isolated topologies [2][3], a high-frequency transformer is used to isolate the input and the output with a two-stage dc-ac-dc power conversion. The converter circuit's size and cost are increased. Moreover, the leakage inductances can be caused a voltage spike on switches. Owing to these limitations, the transformer-based topologies cannot achieve a high efficiency as non-isolated topologies. For the non-isolated topologies, many high boost dc-dc converters have been proposed in [4-15].

* Graduate School, Chosun University, Gwangju, Korea
** Dept. of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City, Viet Nam
★ Corresponding author
E-mail : nmkhai00@gmail.com, Tel : +84-8-3896 1333
Manuscript received Feb. 24, 2019; revised Mar. 7, 2019; accepted Mar. 28, 2019.

The high boost converters with coupled-inductor are proposed in [4][5] can obtain the high voltage gain; however, the leakage inductance of the coupled inductor causes high voltage spike on switches. The non-coupled-inductor converters can achieve a high-voltage gain with a high efficiency because of lacking the leakage inductance. Different structure and techniques including cascaded [6], switched-inductor [7], switched-capacitor [8], interleaved [9][10], and voltage-lift [11-15] techniques have been introduced. In switched-capacitor technique [8], by combining several switches and capacitors with minimum inductor achieving a higher output voltage can be obtained. However, this technique uses a large of number of switches and capacitors, which increase the current stress of switching. In [12], series and parallel combinations of converters have been verified to improve the voltage gain of the converter. However, they can increase size, cost, and complexity of control. Thus, it was not very interesting to researchers. Moreover, the voltage lift techniques based on inductor and capacitor elements was proposed in [13][14] to decrease the voltage stress of switch, as shown in Fig. 2. The voltage lift technique can use for the applications with high efficiency, simple structure, and cheapness when compared with other techniques. In addition, the lack of additional switches that lead to the complexity of the control system of a dc - dc converter is an important feature of this technique. The non-isolated dc - dc boost converters using the voltage technique has been presented in [15] with the higher voltage gain. In this topology, the output voltage of the proposed converter is negative with respect to input ground. However, the voltage gain is not high.

This paper presents a dc-dc converter based on switched-inductor technique with high-boost conversion ratio. The following characteristics of the proposed converter are: easy to increase the voltage gain, high-boost voltage gain, and using the small duty cycle. The content of the paper is

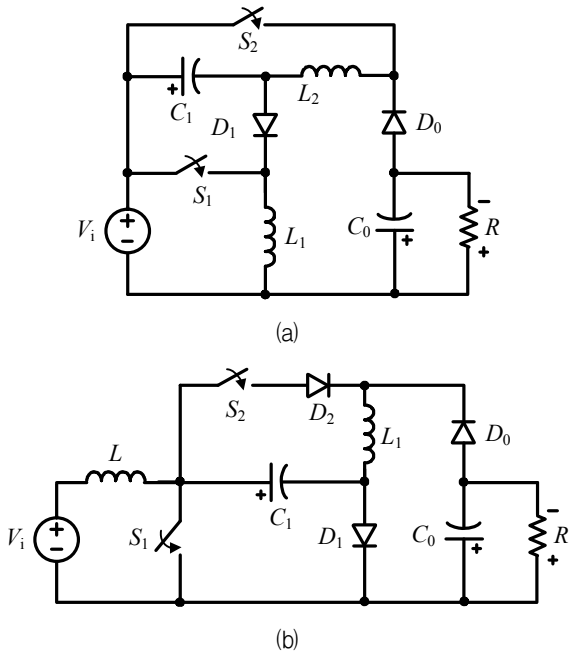

Fig. 2. Voltage-lift technique based non- isolated dc-dc converter in (a) [14] and (b) [15].

organized as follows. In Section II, the suggested topology is presented along with the circuit operation principle and steady-state analysis in continuous conduction mode (CCM). Some comparisons with other converters are shown in Section III. The design procedure along with the simulation results in PLECs software is given in Section IV. Finally, some conclusions are discussed on Section V.

II. Proposed Converter

Fig. 3 shows the suggested dc-dc converter. It consists of one SL cell (L_a, L_b, D_a, D_b, and D_c), two power switches (S_1-S_2), modular voltage boost stage (L_1, D_1, D_2, and C_1), one diode (D_0), one capacitors (C_o), and a resistive load (R). Fig. 4 shows the key waveforms of the suggested converter operating in the CCM. The operation of switches is controlled by the PWM technique and opposes each other. The switches, S_1 and S_2, are turned on and off alternately. To simplify the circuit analyses of the suggested converter in the CCM, the following assumptions were made: 1) all devices are ideal and lossless; 2) the capacitance

of the capacitors is large enough to maintain the constant capacitor voltage; and 3) the current flow to the inductor increases or decreases linearly.

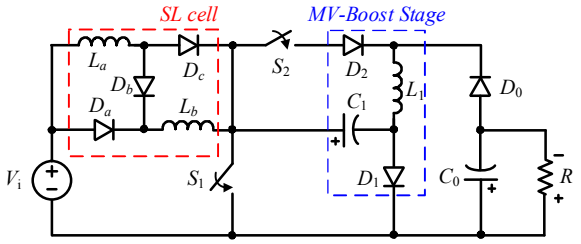

Fig. 3. Proposed dc-dc converter.

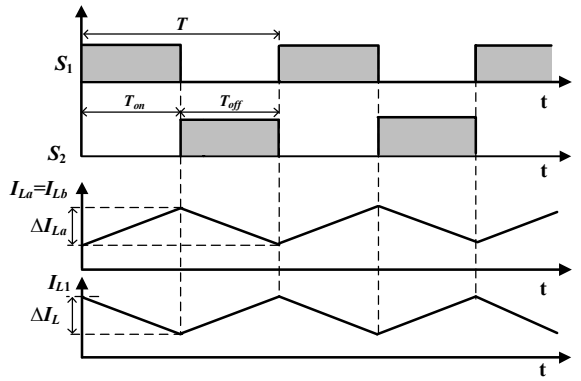

Fig. 4. Key waveforms of the suggested converter.

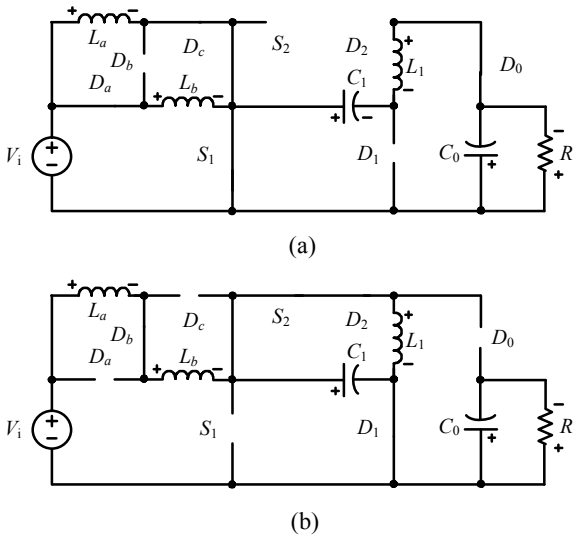

Fig. 5. Operating modes of the suggested converter: (a) state 1 and (b) state 2.

A. Converter Analysis in CCM

Fig. 4 shows the key waveforms of the suggested converter in the CCM. Fig. 5 shows the operating state of the suggested converter.

State 1-[$0 \le t \le DT$, Fig. 5(a)]: S_1 is turned "ON". The L_a and L_b inductors are charged. The D_a, D_c diodes are forward-biased, while the D_b diode is reverse-biased. The D_0 diode is forward-biased and D_1 is reverse-biased. The time interval in this mode is $T_{on} = DT$, where D and T are the duty cycle of switch S_1 and the switching period, respectively.

$$\begin{cases} L_a \dfrac{di_{La}}{dt} = L_b \dfrac{di_{Lb}}{dt} = V_i \\ L_1 \dfrac{di_{L1}}{dt} = V_{C1} - V_o. \end{cases} \tag{1}$$

State 2-[$DT < t \le T$, Fig. 5(b)]: S_1 is switched "OFF" and S_2 is switched "ON"; the D_0 diode is reverse-biased while the D_1 diode is forward-biased. The time interval in this mode is $T_{off} = (1-D) \cdot T$. During this mode, the L_a and L_b inductors are discharged, while the L_1 capacitor is charged. The following formulas are derived as

$$\begin{cases} L_a \dfrac{di_{La}}{dt} + L_b \dfrac{di_{Lb}}{dt} = V_i - V_{C1} \\ L_1 \dfrac{di_{L1}}{dt} = V_{C1}. \end{cases} \tag{2}$$

Through the application of the volt-second balance law to the inductors L_a, L_b, and L_1 in a steady state, (1) to (2) yield the following equations:

$$\begin{cases} DV_i + (1-D)\left(V_i - V_{C1} - V_{Lb\_off}\right) = 0 \\ DV_i + (1-D)V_{Lb\_off} = 0 \\ D\left(V_{C1} - V_o\right) + (1-D)V_{C1} = 0, \end{cases} \tag{3}$$

By substituting (3) into (1), the capacitor C_1 voltage and output voltage of the suggested converter are as follows:

$$\begin{cases} V_{C1} = \dfrac{1+D}{1-D} V_i \\ V_o = \dfrac{1+D}{D(1-D)} V_i, \end{cases} \tag{4}$$

B. Extension of the Suggested Converter

According to Fig. 6, the suggested converter

is possible to verify an n-stage boost converter by adding the modular voltage boost stage (one inductor, one capacitor and two diodes). The voltage gain with n from 1 to 4 is shown in Fig. 7. The extension with n-stage boost structure, the SL-cell and two switches are kept in the power circuit, and $(n + 1)$ inductors, $(n + 1)$ capacitors, and $(2n + 1)$ diodes are used for modular voltage boost stage.

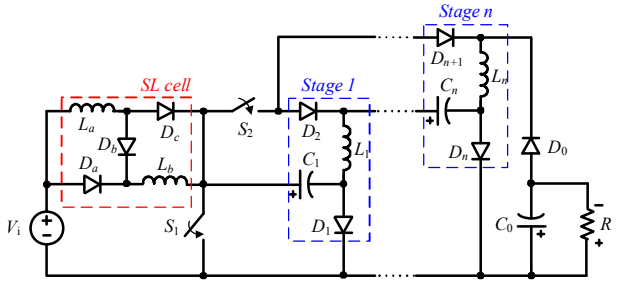

Fig. 6. Suggested converter with n-stages.

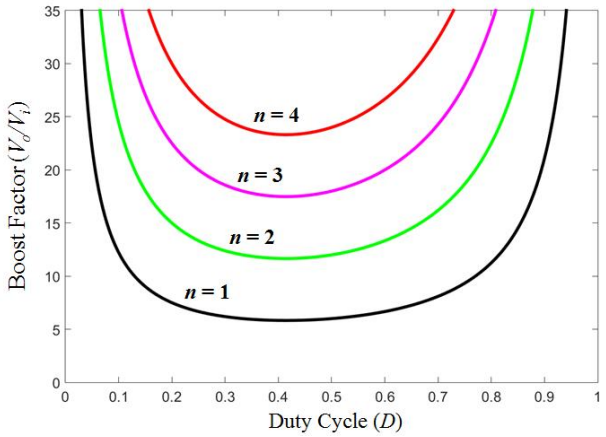

Fig. 7. Voltage gain comparison.

For analysis, S_1 is ON and S_2 is OFF, D_0 is conducted, and D_1, D_2, ⋯, D_n are Off. Moreover, L_2, L_3, ⋯, L_{n+1} and C_1, C_2, ⋯, C_n are in series connection. The series connection of n-capacitors increases V_o. When S_1 is OFF and S_2 is OFF, and D_1, D_2, ⋯, D_n are directly biased and D_0 is reversely biased. The voltage gain of the n-stage converter in CCM is given

$$V_o = \frac{n(1+D)}{D(1-D)} V_i \tag{5}$$

III. Comparison with Other Non-Isolated High-Boost Converters

The comparison between the suggested converter and other non-isolated high-boost dc-dc converters is shown in Table 1. When compared with the non-isolated dc-dc converters in [13]-[15], the suggested converter uses one more inductor and diodes. Moreover, the suggested converter has less one switch and one capacitor than the non-isolated converter in [14]. Although, the suggested converter uses more components, the suggested converter can save the size of the inductor in SL cell and has higher voltage gain. Fig. 8 shows a comparison between the voltage gains of the non-isolated high boost dc-dc converters in the CCM. As shown in Fig. 8, the voltage gain of the proposed converter is the highest at the same duty cycle.

Table 1. Comparison between the suggested converter and other high boost dc-dc converters.

	Switch	Inductor	Capacitor	Diode	Voltage gain
Converter in [13]	2	2	2	2	$\frac{1}{D(1-D)}$
Converter in [14]	3	1	3	2	$\frac{1-D+D^2}{D(1-D)}$
Converter in [15]	2	2	2	3	$\frac{1}{D(1-D)}$
Suggested converter	2	3	2	6	$\frac{1+D}{D(1-D)}$

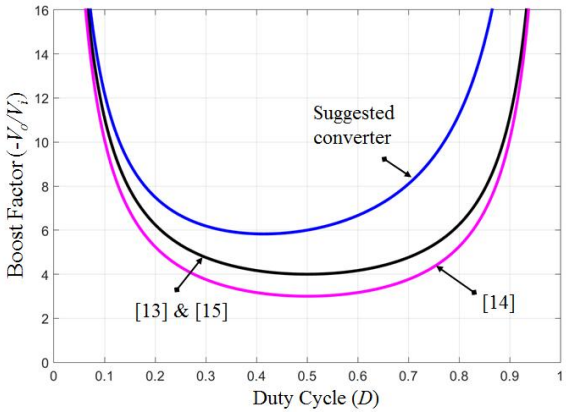

Fig. 8. Operating modes of the suggested converter: (a) state 1 and (b) state 2.

IV. Simulation Verification

To confirm properties and the presented analysis of the proposed converter, the simulation results based on PLECS software were presented. Table 2 indicates a list of parameters of the proposed converter used in the simulation.

Fig. 9 presents the simulation results of the proposed converter with D = 0.5 and V_i = 20 V. As shown in Fig. 9(a), the capacitor C_1 voltage and the capacitor C_0 voltage was boosted to 60 V and 120 V, respectively. The output voltage is 120 V. The average inductors current, I_{La} and I_{Lb} is 6.7 A and with peak-peak ripple of 0.7 A, while the average inductor current, I_{L1} is 3.3 A with peak-peak ripple of 1 A as shown in Figs. 9(a) and 9(c). The voltage stress across active switches, S_1 and S_2 is 60 V and 120V, respectively.

Fig. 10 shows the simulation results with D = 0.814 and V_i = 10V. As shown in Fig. 10(a), the capacitor C_1 voltage and the capacitor C_0 voltage was boosted to 97 V and 120 V, respectively. The output voltage is 120 V. The average inductor current, (I_{La} = I_{Lb}) is 7.89 A and with a peak-peak ripple of 0.82 A, while the average inductor current, I_{L1} is 1.47 A and with peak-peak ripple of 0.92 A as shown in Figs. 10(a) and 10(c). The voltage stresses across active switches, S_1 and S_2 are 97 V and 120V, respectively.

Table 2. List of parameters

Parameter		Value
Input/out voltage		20 V/120V
Output power		200W
Capacitor C_1		330 μF
Capacitor C_0		220 μF
Inductor	(L_a = L_b)	1000 μH
	L_1	2000 μH
Resistor load		72 Ω
Switching Frequency		10 kHz

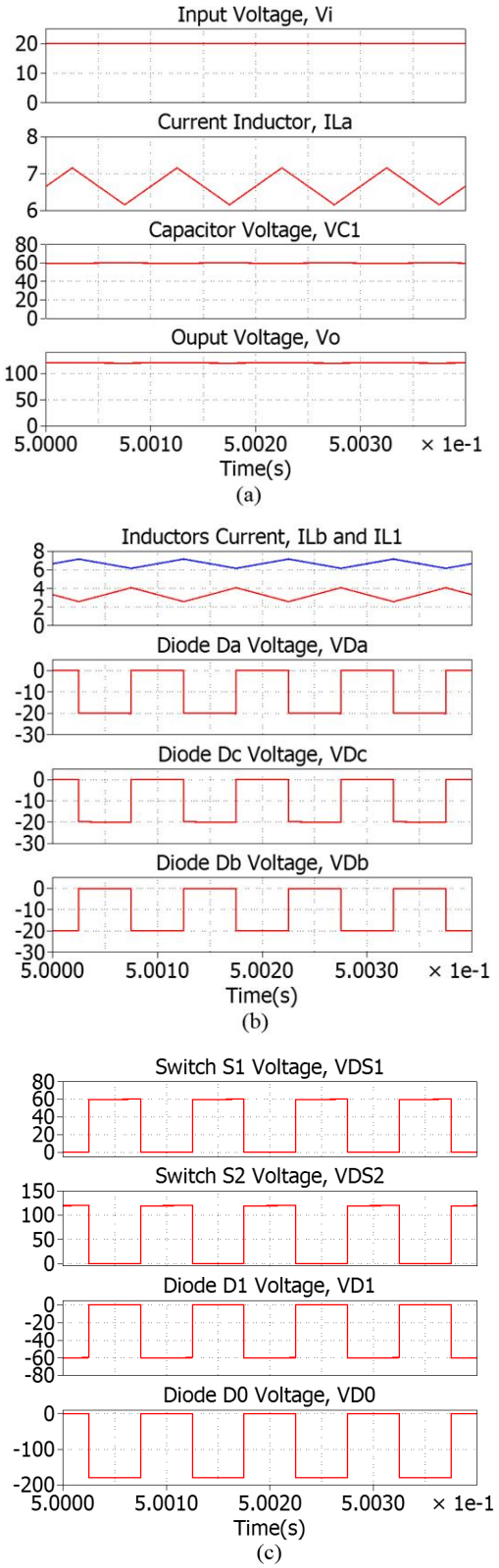

Fig. 9. Simulation waveforms when V_i = 20 V. From top to bottom: (a) input voltage, inductor L_a current, capacitor C_1 voltage, output voltage; (b) inductor current, D_a, D_b and D_c voltages; and (c) S_1, S_2, D_1, and D_0 voltages.

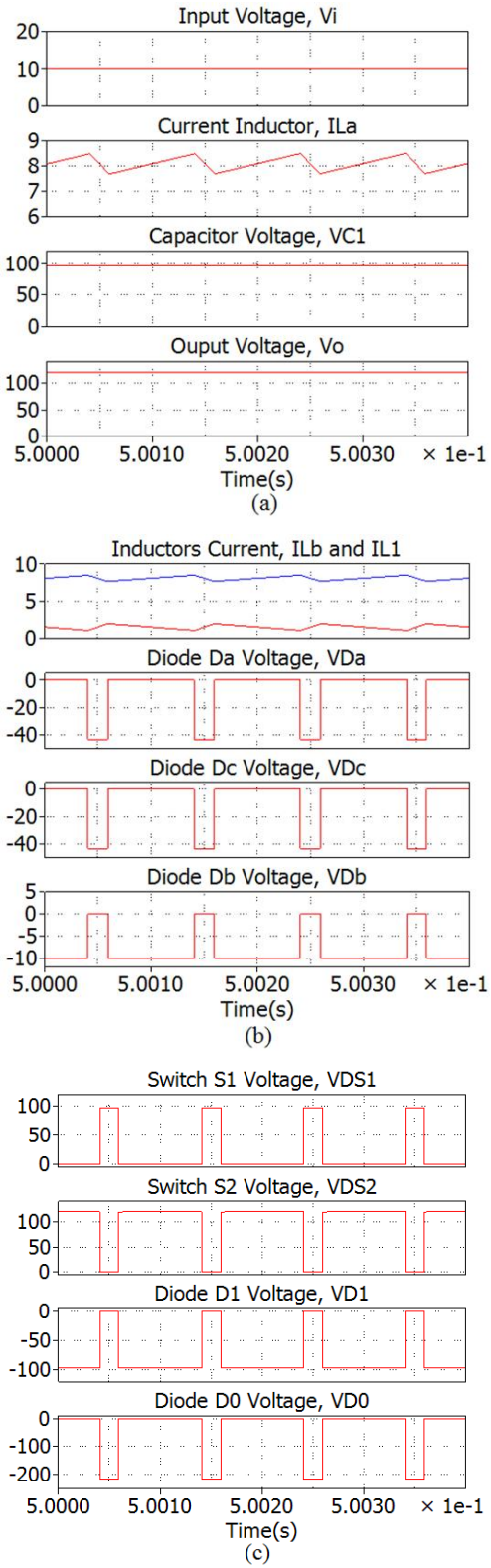

Fig. 10. Simulation waveforms when V_i = 10 V. From top to bottom: (a) input voltage, inductor L_a current, C_1 capacitor voltage, output voltage; (b) inductors current, D_a, D_b and D_c voltages; and (c) S_1, S_2, D_1, and D_0 voltages

V. Conclusions

The novel high gain dc-dc boost converter based on the switched-inductor cell was suggested in this paper. The suggested converter features were presented by its development for *n*-stage with a modular voltage boost circuit; it can improve the voltage gain and efficiency. The structure of suggested converter was compared in CCM with other conventional non-isolated boost converters from the standpoint of number of switches, inductors, capacitors and diodes, and voltage gain. For same operating condition, it was shown that the suggested converter improves the voltage gain. The simulation results from PLECS Software match those obtained from the theoretical analysis.

References

[1] K.C. Tseng and C.C.Huang, "High step-up high-efficiency interleaved converter with voltage multiplier module for renewable energy system," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1311-1319, 2014. DOI: 10.1109/TIE.2013.2261036

[2] C. Mi, H. Bai, C. Wang, and S. Gargies, "Operation, design and control of dual H-bridge-based isolated bidirectional DC-DC converter," *IET Power Electron.*, vol. 1, no. 4, pp. 507-517, 2008. DOI: 10.1049/iet-pel:20080004

[3] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89-98, 2015. DOI: 10.1109/TPEL.2014.2305976

[4] G. Wu, X. Ruan, and Z. Ye, "High step-up dc-dc converter based on switched-capacitor and couple inductor," *IEEE Trans. Ind. Electron.*, vol. 65, no. 7, pp. 5572-5579, 2018. DOI: 10.1109/TIE.2017.2774773

[5] M. Forouzesh, Y. Shen, K. Yari, Y. P. Siwakoti, and F. Blaabjerg, "High-efficiency high step-up

dc-dc converter with dual couple inductors for grid-connected photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5967-5982, 2018. DOI: 10.1109/TPEL.2017.2746750
[6] A. I. Bratcu, I. Munteanu, S. Bacha, D. Picault, and B. Raison,, "Cascaded dc - dc converter photovoltaic systems: power optimization issues," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 403-411, 2011. DOI: 10.1109/TIE.2010.2043041
[7] H. C. Liu, F. Li, "A novel high step-up converter with a quasi-active switched- inductor structure for renewable energy systems," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 5030-5039, 2016. DOI: 10.1109/TPEL.2015.2480115
[8] G. Wu, X. Ruan, and Z. Ye, "Nonisolated high step-up DC - DC converters adopting switched-capacitor cell," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 383-393, 2015. DOI: 10.1109/TIE.2014.2327000
[9] F. S. Garcia, J. A. Pomilio, and G. Spiazzi, "Modeling and control design of the interleaved double dual boost converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3283-3290, 2013. DOI: 10.1109/TIE.2012.2203770
[10] K. C. Tseng, C. A. Cheng, and C. T. Chen, "High step-up interleaved boost converter for distributed generation using renewable and alternative power sources," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 2, pp. 713-722, 2017. DOI: 10.1109/JESTPE.2016.2611641
[11] C. T. Pan, C. F. Chuang and C. C. Chu, "A novel transformer-less adaptable voltage quadrupler dc converter with low switch voltage stress," *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp. 4787-4796, 2014. DOI: 10.1109/TPEL.2013.2287020
[12] P. Saadat and K. Abbaszadeh, "A single-switch high step-up dc-dc converter based on quadratic boost," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7733-7742, 2016. DOI: 10.1109/TIE.2016.2590991
[13] F. M. Shahir, E. Babaei, and M. Farsadi, "A new structure for non-isolated boost dc-dc converter," *J. Circuits, Syst., Comput.*, vol. 1, no. 1, 2017. DOI: 10.1109/PEDSTC.2017.7910373
[14] J. Li, and J. Liu, "A negative-output quadratic conversion ratio dc-dc converter with dual working modes," *IEEE Trans. Power. Electron.*, vol. 99, pp. 1-1, 2018. DOI: 10.1109/TPEL.2018.2870421
[15] F. M. Shahir, E. Babaei, and M. Farsadi, "Extended topology for a boost dc-dc converter," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2375-2384, 2019. DOI: 10.1109/TPEL.2018.2840683

BIOGRAPHY

Ho-Yeon Kim (Member)

1999 : BS degree in Economics, Chonnam University.
2011 : MS degree in Software Engineering, Honam University.
2018 : Ph.D. Cand in Electrical Engineering, Chosun University.
2007~2011 : DELLEMC Sr. Engineer.

Eun-A Moon (Member)

1991 : BS degree in Electrical Engineering, Chosun University.
2005 : MS degree in Electrical Engineering, Chosun University.
2014 : PhD degree in Electrical Engineering, Chosun University.

Minh-Khai Nguyen (Member)

2005 : BS degree in Electrical Engineering, Ho Chi Minh City University of Technology.
2007 : MS degree in Electrical Engineering, Chonnam National University.
2010 : PhD degree in Electrical Engineering, Chonnam National University.