Journal of Semiconductor Engineering Vol. 1, Issue 3, December 2020
https://doi.org/10.22895/jse.2020.0103
Received 30 November 2020, Accepted 21 December 2020 ISSN(On-line) 2733-6719

Recent Advances in Radiation-Hardened Sensor Readout Integrated Circuits

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Funding Information: This research was supported by the National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science & ICT (NRF-2017M1A7A1A01016260). This work was also supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. NRF-2020M3F3A2A01081238). The chip fabrication and EDA tool were supported by IC Design Education Center (IDEC), Korea.

ABSTRACT

An instrumentation amplifier (IA) and an analog-to-digital converter (ADC) are essential circuit blocks for accurate and robust sensor readout systems. This paper introduces recent advances in radiation-hardening by design (RHBD) techniques applied for the sensor readout integrated circuits (IC), e.g., the three-op-amp IA and the successive-approximation register (SAR) ADC, operating against total ionizing dose (TID) and singe event effect (SEE) in harsh radiation environments. The radiation-hardened IA utilized TID monitoring and adaptive reference control to compensate for transistor parameter variations due to radiation effects. The radiation-hardened SAR ADC adopts delay-based double-feedback flip-flops to prevent soft errors which flips the data bits. Radiation-hardened IA and ADC were verified through compact model simulation, and fabricated CMOS chips were measured in radiation facilities to confirm their radiation tolerance.

KEY WORDS

Radiation-hardened, sensor readout, integrated circuit, single event effect, soft error, total ionizing dose, instrumentation amplifier, SAR ADC.

1. INTRODUCTION

It is important to control the sensor system stably and accurately by measuring environmental signals such as temperature, pressure, and electromagnetic field. Those sensor signals can be measured and converted from analog signals to digital bits in the readout circuits as shown in Figure 1. The instrumentation amplifier (IA) and the analog-to-digital converter (ADC), which consist of both digital and analog circuit blocks, suffer from radiation effects that severely degrade system performance in harsh radiation environments [1]-[3]. Such radiation effects can be critical issues in space, aviation, automotive semiconductors, nuclear power, etc. The sensor systems in those environments can be susceptible to performance degradation and malfunction caused by radiation effects [2].

Silicon-based transistors in ICs, such as CMOS and bipolar junction transistor (BJT), can be affected by

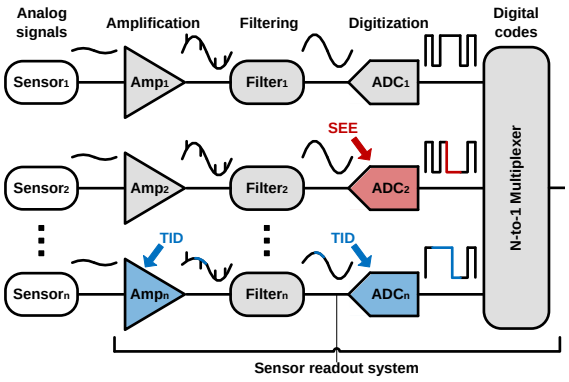


Figure 1. Block diagram of the sensor front-end readout integrated circuit (IC) system

electrons, neutrons, and protons in radiation environments, which change the transistor parameters and circuit operation. Total ionizing dose (TID) and single event effect (SEE) are two main causes that degrade

the performance of CMOS integrated circuits [4], [5]. TID occurs when high energy particles penetrate through CMOS transistors and generate electron-hole pairs, leading the generated holes to be trapped in the gate oxide. TID effects are long-term exposure, gradually changing the threshold voltage and leakage current of CMOS transistors, which mainly affect the performance of analog circuits. In contrast to TID, SEE is an instantaneous disturbance that disrupts the circuit operation when high energy particles impact the CMOS transistor in a moment, which instantaneously changes the voltages at surrounding nodes. SEE mainly affects digital, memory, and switched capacitor circuits, in which voltage values can be flipped or changed.

Recent advances in radiation-hardened ICs include radiation-hardening by shielding (RHBS), radiation-hardening by processing (RHBP), and radiation-hardening by design (RHBD) [6]-[8]. While those methods can be utilized together to maximize the radiation tolerance, this paper focuses on circuit design methods that can be robust against radiation effects, by reviewing recent papers about radiation-hardened IA and ADC [9], [10].

In addition, it is important to estimate the circuit performance against TID and SEE during the design stage. To accurately reproduce radiation effects on CMOS simulations, a compact transistor models can be used for SPICE simulation. This compact model-based simulation methodology enables the precise estimation of the IC performance before conducting experiments in actual radiation environments.

2. RADIATION-HARDENED IA

Various topologies exist on instrumentation amplifiers (IA), such as capacitive-feedback IA, current-feedback IA, and three-op-amp IA. To design a radiation-hardened IA, it is important to determine the IA topology that produces robust and accurate results in the radiation environment.

The capacitive-feedback IA uses a couple of capacitors in the feedback loop, and the voltage gain is determined by the ratio between the capacitors. However, the voltage values across the capacitors can vary because of unwanted charge injection by SEE, which results in inaccurate output voltages. The current-feedback IA utilizes transconductance amplifiers at input and feedback paths to define its voltage gain with the ratio of transconductance (Gm). The current-feedback IA has the advantages of high common-mode rejection ratio (CMRR) and large input range, but the gain accuracy suffers from TID effects, which change the transconductance values.

Compared to those IAs, the three-op-amp IA has advantages such as good linearity, high input impedance. In addition, it is robust to TID because the gain is determined by the resistor ratio [9]. It is also robust to SEE because the DC bias is well held by the feedback loop. Figure 2 shows the radiation-hardened IA including TID-effect monitoring, V_{th}-insensitive current generator, and adaptive reference control. The TID effect monitoring circuit, which is reliably biased by the V_{th}-insensitive current generator, senses the V_{th} variation due to TID effects. Then, the adaptive reference control circuit automatically adjusts the sensor reference voltage, V_{REF}, keeping the tail current transistors in op-amps, A_1 and A_2, to operate in saturation regions regardless of V_{th} variation in the transistors.

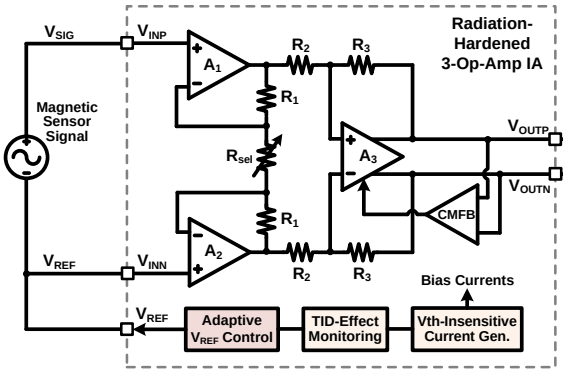


Figure 2. Conceptual diagram of the radiation-hardened IA [9]

TID changes the V_{th} of the MOSFET (the V_{th} of the PMOS increases, the V_{th} of the NMOS decreases), degrading the performance of the op-amp. To solve the V_{th} variation, adaptive reference control is used to automatically provide the sensor reference voltage V_{REF} to A_1 and A_2 in common-mode input level, as shown in Figure 3. The adaptive reference control utilizes the TID effect monitoring and the additional resistor R_1 to generate V_{REF} as $V_{DD}-V_{SG,MM}-I_{REF}R_1$. For example, if V_{th} of PMOS transistors increases due to TID, which decreases the maximum input level of the op-amps, V_{REF} also adaptively decrease to ensure that input stages are operating properly in saturation regions.

TID monitoring circuit is required to adaptively

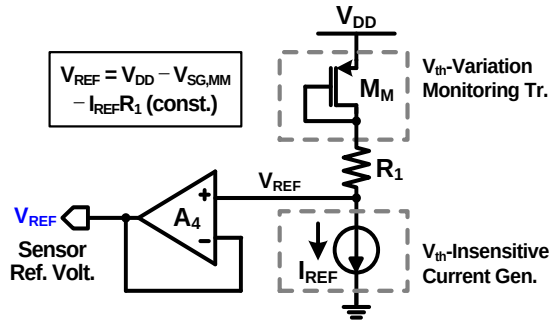


Figure 3. Conceptual diagram of the adaptive reference control [9]

change V_{REF} according to radiation effect. In order to implement the TID monitoring circuit, constant I_{REF} is required because a constant current must be passed to the M_M Transistor. In Figure 4, only part of M_M is TID-effect monitoring, and the other part is V_{th}-insensitive current generator. The monitoring voltage, V_M, can be expressed as follows:

$$V_M = V_{DD} - V_{SG,MM} = V_{DD} - V_{ov,MM} - V_{th,MM} \quad (1)$$

where V_{DD} is the supply voltage, and $V_{ov,MM}$ and $V_{th,MM}$ are the overdrive and threshold voltages of M_M, respectively. If I_{REF} has little variation against TID, then $V_{ov,MM}$ can be relatively constant, and $V_{th,MM}$ variation can be observed by monitoring V_M, which changes as TID increases.

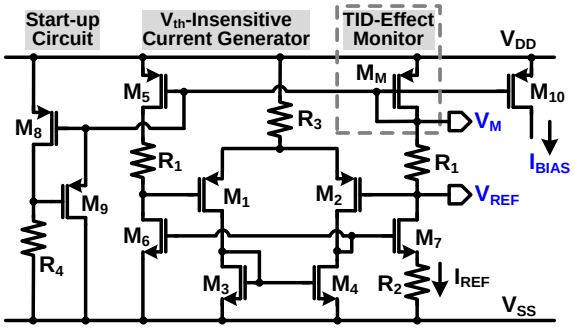


Figure 4. Schematic diagram of the TID effect monitoring circuit with the V_{th}-insensitive current generator [9]

3. RADIATION-HARDENED ADC

ADCs have various structures, such as flash ADC, pipelined ADC, successive approximation register (SAR) ADC, and sigma-delta ADC, depending on the operation method and required performance. ADC performance used in typical sensor systems (temperature, pressure, magnetic fields, etc.) requires more than 8-bit resolution and sampling rate above tens of kHz. Among them, SAR ADCs can realize the high resolution of 8 bit or above, while its sub-blocks can be mostly implemented with digital circuits, which is relatively robust to TID [10]. The flip-flops or capacitors used in conventional SAR ADCs may be vulnerable to SEE, but it can be addressed by adopting the radiation-hardened flip-flops and SAR ADC structure.

In Figure 5, the radiation-hardened SAR ADC utilizes a strong-arm digital comparator and a resistor-type digital-to-analog converter (DAC) to tolerate the radiation effects [10]. Conventional flip-flops used in the SAR logic circuit suffer from data flip due to SEE, which leads to soft errors [11]. To reduce the soft error rate, the radiation-hardened flip-flops were adopted in the SAR logic circuit.

Figure 6 shows a basic flip-flop made with latches in a cross-coupled inverter structure. When the clock (CLK) is low, the slave latch stores data while the master latch receives the incoming data. However, this structure has a limitation that the stored data value can be changed by instantaneous SEE. Dice latches and Quatro latches, which are robust to soft errors because it utilizes four memory nodes, have been proposed to improve SEE tolerance, but these structures suffer from the racing issue [11].

In order to solve the racing problem and enhance radiation tolerance, a latch with dual feedback structure has been proposed as shown in Figure 7 [12]. In this structure, soft errors occurring at QB_1 and QB_2

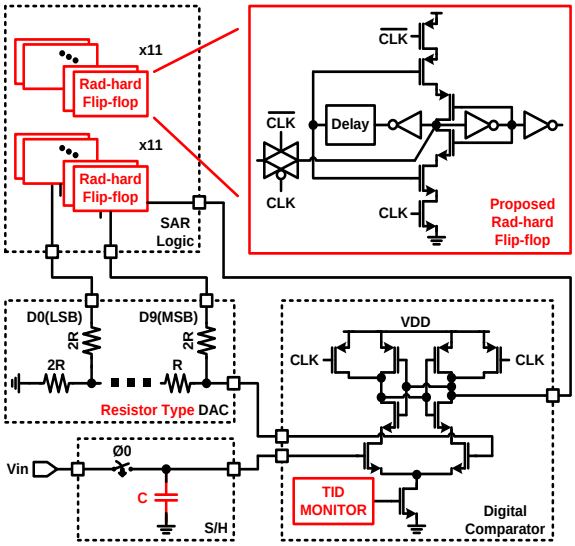
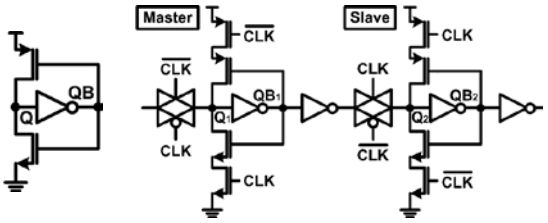


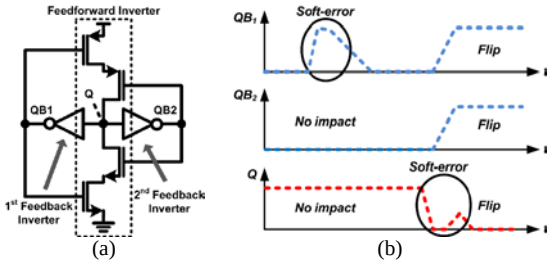
Figure 5. Block diagram of the radiation-hardened SAR ADC [10]



(a) (b)

Figure 6. Schematic diagrams of (a) conventional latch and (b) conventional flip-flop [11]

nodes do not affect the stored values when latched, but Q nodes are still vulnerable to soft errors, leading to data flip. As shown in the timing diagram in Figure 7(b), when SEE occurs at the Q node, the instantaneous glitch temporarily activates the pull-up or pull-down path of the feedforward inverter by changing the voltage at the QB_1 and QB_2 nodes simultaneously. In this case, a significant amount of charge is injected into the Q node through a pull-up or pull-down path, resulting in data flip.



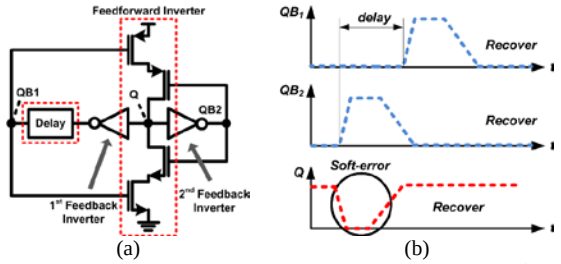
(a) (b)

Figure 7. (a) Conventional dual feedback latch [12] and (b) timing diagram when the soft error occurs

The flip-flops of SAR logic, which stores the output data of the ADC, can be affected by radiation, degrading performance. The radiation-hardened latch with delay-based dual feedback loops can be used to prevent the data flip [10]. The proposed radiation-hardened latch adjusts the delay time of the feedback path

by adding the delay cell to the 1st feedback inverter output as shown in Figure 8. As a result, the first feedback path in the latch has a longer delay time than the second feedback path.

The timing diagram in Figure 8(b) clearly shows how the proposed radiation-hardened latch can be robust to soft errors. Even if SEE occurs at the Q node of the proposed latch and instantaneous glitch occurs, the pull-up or pull-down path of the feedforward inverter is still not activated due to the delay difference between the first and second feedback paths. As a result, no additional charge is transferred to the Q node through the feedforward inverter, and the voltage value of the Q node can be recovered quickly.



(a) (b)

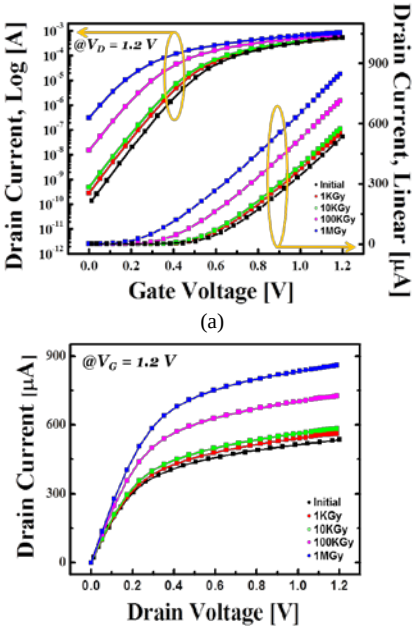
Figure 8. (a) Radiation-hardened latch with delay-based dual feedback loops [10] and (b) timing diagram when the soft error occurs

4. COMPACT MODEL SIMULATION

In order to observe the circuit performance with the TID effects, the Berkeley short-channel IGFET Model (BSIM) 4 SPICE model was used in this work. The BSIM4 model is widely used as a standard compact model in the industry and has been developed for silicon based MOS transistors [13], [14].

Figure 9 shows the electrical characteristics of the device with TID effects for each Gy level. To obtain compact models for each TID quantity, several levels of TID effects were applied to CMOS transistors through the TCAD simulation with the Silvaco Victory Device software, which generated corresponding I-V curves. Then, BSIM parameters, such as V_{TH0} (long channel threshold voltage), V_{FB} (flatband voltage), V_{SAT} (saturation velocity), CIT (interface trap capacitance), etc., which affect the threshold voltage, subthreshold swing, and leakage current, were extracted from those I-V curves and utilized to develop the compact models for each TID. The V_{th} shift phenomenon and the off-current increase, which were caused by the TID effects, were confirmed.

The I-V curve in Figure 9 was used for compact modeling in the BSIM4 parameter extraction process for each cumulative dose. The BSIM4 parameters were extracted by using Silvaco Utmost IV software. The flow chart of BSIM4 model parameter extraction was detailed in a previous work [14]. In order to extract the BSIM4 parameters, the V_{GS} versus I_D curve in linear and log scales and the V_{DS} versus I_D curve in linear scale were simultaneously considered. The BSIM4 parameters were extracted by matching the linear and saturation regions of the I-V curve by adjusting parameters such as V_{th0}, V_{sat}. [15], [16].

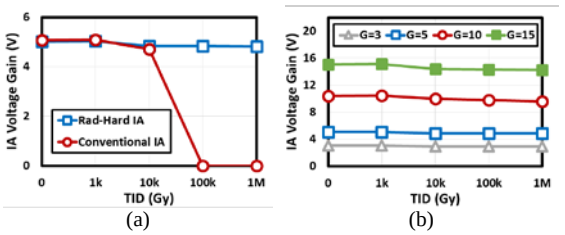


(a)

(b)

Figure 9. CMOS transistor characteristics depending on TID effects: (a) V_{GS} vs. I_D and (b) V_{DS} vs. I_D

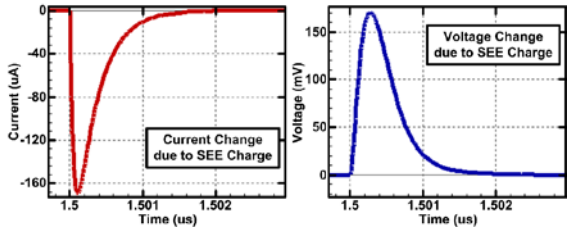
Figure 10 shows the voltage gain of the radiation-hardened IA against the TID effects [9]. In Figure 10(a), the voltage gain of the radiation-hardened IA was set to 5 and showed a little variation as TID increased. However, the conventional IA, which also had the three-op-amp structure, but its sensor reference level (V_{REF}) was fixed to half V_{DD}, had a significant drop of the voltage gain with TID above 10 kGy, because some transistors in the op-amps could operate in triode regions, and their bias currents significantly changed. On the contrary, the radiation-hardened IA could provide an adjustable voltage gain between 3 and 15 over high TID effects, as shown in Figure 10(b).



(a) (b)

Figure 10. Model simulation results showing (a) voltage gain comparison between proposed and conventional IAs by TID and (b) adjustable voltage gain (3, 5, 10, and 15) of the proposed IA by TID.

Figure 11 shows the simulated current and voltage waveforms generated by SEE when the SEE function of the radiation simulator CAD tool is applied to the specific CMOS transistor. These radiation simulations can be used to verify radiation tolerance and optimize performance at the circuit design stage.



(a) (b)

Figure 11. Simulated waveforms of the (a) current and (b) voltage changes due to SEE.

The TID effect was applied to the proposed flip-flop using the compact transistor model to verify the radiation tolerance against the TID [10]. To consider both TID and SEE in model simulation, the SEE charge was also applied to the flip-flop using the radiation simulator CAD tool, in addition to the compact transistor models, and then the amount of flip charge (Q_{flip}), which leads to data flip, was checked. Figure 12 is a graph showing Q_{flip} leading to a data flip and average power of flip-flop according to TID levels. The flip-flop maintains Q_{flip} until the TID goes up to 1MGy, while power consumption is slightly increased.

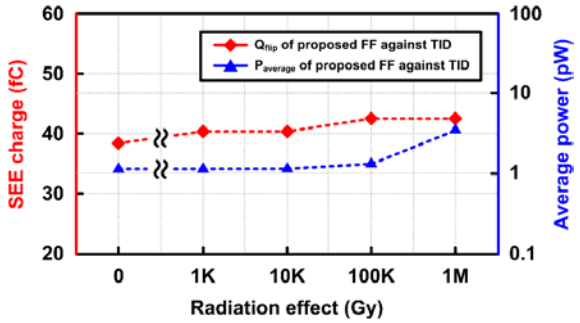


Figure 12. Flip charge (Q_{flip}) and average power of the proposed flip-flop depending on TID

5. MEASUREMENTS

Figure 13 shows the test setup to measure the radiation-hardened performance of the test chip in a high-level radiation facility. Radiation experiments were performed in the gamma ray environment. Radiation-hardened sensor readout test chips were measured with a high dose rate of 15 kGy/h, resulting in a total dose of 50 kGy for 200 minutes.

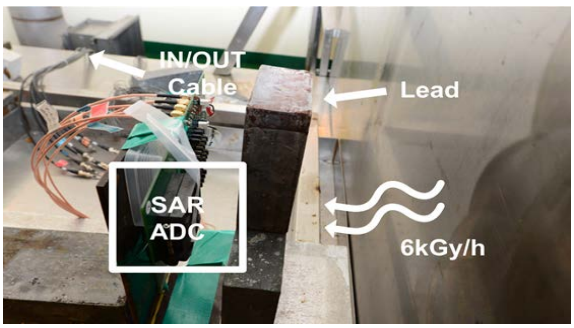


Figure 13. Chip test setup in the high-level radiation facility

Figure 14 shows the reference voltage and current of the TID monitor circuit according to the TID level, which describes the change in device characteristics such as the V_{th}. It can be observed that the reference voltage and current are almost constant up to TID 50 kGy, ensuring little TID effects to radiation-hardened IA and ADC circuits.

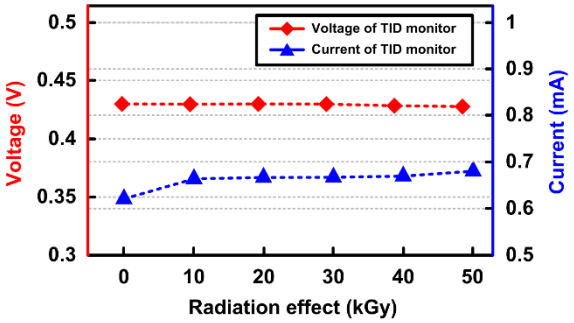


Figure 14. Performance changes of the TID monitor circuit against TID levels.

To verify and compare the flip-flop performance in the radiation environment, the error rates of the flip-flop outputs were measured when the radiation time was 60 s, 90 s, 120 s, and 150 s. The experiment for each radiation time was repeated five times, and the number of measured errors was summed. Consequently, we could obtain the number of flipping errors for 50,000 flip-flops.

For our radiation test, we use a 45 MeV proton beam gun, which has 22 mm diameter and a 1 nA flux. The distance between the proton beam gun and our test-chip is 2.5 m, and the effective energy of the proton becomes 41.16 MeV. At this time, each flip-flop operates with a supply voltage of 2.3 V.

The chip verification results are shown in Figure 15. The proposed radiation-hardened flip-flop shows robust operations with 50–60% fewer soft errors compared to the conventional flip-flop. As the radiation exposure time increased, conventional flip-flops suffer from a significant increase in the data flip errors. On the other hand, the proposed radiation-hardened flip-flop shows a relatively smaller increase in the errors as radiation time increases, verifying radiation tolerance against SEE.

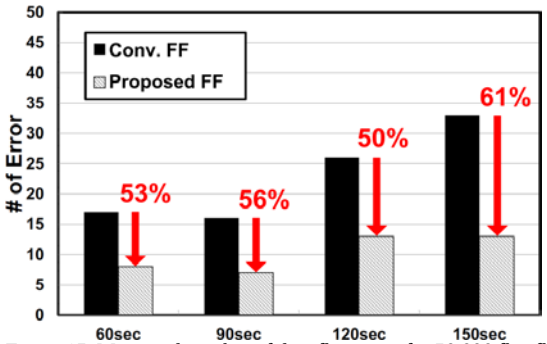


Figure 15. Measured number of data flip errors for 50,000 flip-flops (10,000 FF × 5 times = 50,000) in radiation environments.

Radiation-hardened IA and SAR ADC chips were fabricated in 65nm CMOS process, and the total area is 1.32mm^2 and 0.17 mm^2, respectively. Table 1 summarizes the measured performance of radiation-hardened IA and SAR ADC. The IA provides adjustable voltage gain from 3 to 15, which was robust against the TID level up to hundreds of kGy. The ADC achieves the measured SNDR and ENOB as 50 dB and 8.01 bit, respectively.

Table 1. Performance of the radiation-hardened IA and SAR ADC

IA		**SAR ADC**	
Supply Voltage (V)	1.2	Supply Voltage (V)	1.2
Technology (nm)	65	Technology (nm)	65
Power (mW)	0.2	Power (mW)	0.9
Voltage Gain (V/V)	3-15	Input Range (V_{P-P})	1.2
Bandwidth (kHz)	200	Sampling Rate (kS/s)	25
Input Noise ($\mu V/\sqrt{Hz}$)	2.87	ENOB (bit)	8.01
Offset Voltage (mV)	2.32	SNR / THD (dB)	51.9/-54.6
PSRR (dB)	81	SNDR / SFDR (dB)	50/56.35

6. CONCLUSION

Sensor systems used in flight, space, nuclear power plants, and nuclear fusion reactors suffer from performance degradation and system malfunction due to radiation effects. For stable and accurate sensor readout systems, it is essential to improve radiation tolerance of the core circuit blocks by utilizing radiation-hardening by design (RHBD) in addition to shielding and CMOS process techniques. This paper reviews recent advances in radiation-hardened sensor readout ICs, such as IA and ADC, which ensure robust operation against radiation effects including TID and SEE.

ACKNOWLEDGMENT

This research was supported by the National R&D Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science & ICT (NRF-2017M1A7A1A01016260). This work was also supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. NRF-2020M3F3A2A01081238). The chip fabrication and EDA tool were supported by IC Design Education Center (IDEC), Korea.

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