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Review of Injection-Locked Oscillators

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ABSTRACT

Handling precise timing in high-speed transceivers has always been a primary design target to achieve better performance. Many different approaches have been tried, and one of those is utilizing the beneficial nature of injection locking. Though the phenomenon was not intended for building integrated circuits at first, its coupling effect between neighboring oscillators has been utilized deliberately. Consequently, the dynamics of the injection-locked oscillator (ILO) have been explored, starting from R. Adler. As many aspects of the ILO were revealed, further studies followed to utilize the technique in practice, suggesting alternatives to the conventional frequency syntheses, which tend to be complicated and expensive. In this review, the historical analysis techniques from R. Adler are studied for better comprehension with proper notation of the variables, resulting in numerical results. In addition, how the timing jitter or phase noise in the ILO is attenuated from noise sources is presented in contrast to the clock generators based on the phase-locked loop (PLL). Although the ILO is very promising with higher cost effectiveness and better noise immunity than other schemes, unless correctly controlled or tuned, the promises above might not be realized. In order to present the favorable conditions, several strategies have been explored in diverse applications like frequency multiplication, data recovery, frequency division, clock distribution, etc. This paper reviews those research results for clock multiplication and data recovery in detail with their advantages and disadvantages they are referring to. Through this review, the readers will hopefully grasp the overall insight of the ILO, as well as its practical issues, in order to incorporate it on silicon successfully.

KEY WORDS

Adler's equation, frequency offset tuning, injection-locked, injection-locked clock multiplication (ILCM), injection-locked clock and data recovery (ILCDR), injection-locked oscillator (ILO), phase-locked loop (PLL), phase noise.

1. INTRODUCTION

A clock generator is an essential element in many applications such as serial links, local oscillators, memory interfaces, embedded microprocessors, and so on [1]–[53]. A free-running oscillator is typically built using a resonating crystal with a piezo-electric effect. However, a more important type of oscillator is the oscillator, of which its frequency and phase are precisely controlled by the external reference. The purpose of such managed oscillation is to multiply clock frequency, to produce multi-phase clocks, to exhibit the effect of a zero-delay buffer, to extract the exact phase for data sampling, and so on. The controlled oscillator is more of a concern in this paper rather than the free-running oscillator. A dominant method of clock generation is to use the phase-locked loop (PLL) where a voltage controlled oscillator (VCO) locks to the external reference in a feedback loop composed of a phase detector (PD) and a loop filter. Many performance metrics are used to evaluate its performance, such as jitter, phase noise, power, and cost. To obtain better performance beyond the PLL offers, an alternative type of controlled clock generators has been explored, dating back to the 1940s [1]. When two oscillators with similar frequencies are close by and interact with each other, they end up oscillating at the same frequency by injecting one's phase information into the other through the shared power supply.

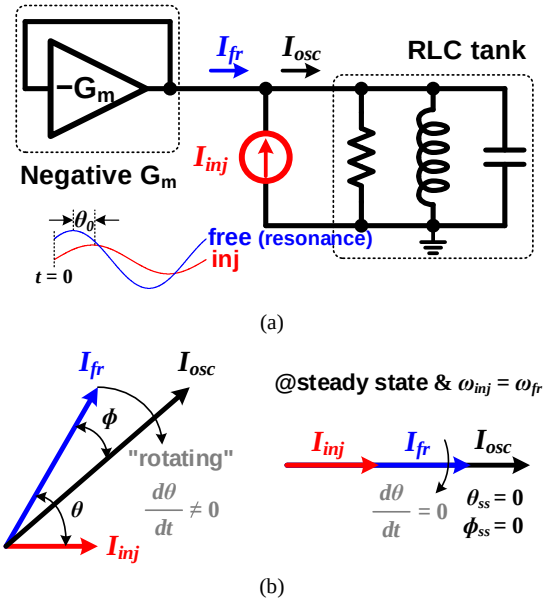


Figure 1. (a) Conceptual block diagram of LC oscillator with injection current. (b) "Rotating" phasor diagram while frequency difference between two signals is tiny but not zero. (c) "Static" phasor diagram at steady state if the frequency offset is zero.

Intuitively, such phenomenon can be explained in the following way: when one clock makes its transition, it affects its power supply, and the supply fluctuation strikes the other oscillator's phase in such a way to move its oscillation phase to either slow down or speed up in a convergent manner. The other direction is equally valid as well in a mutual way. For that to happen, two conditions must be met: the two frequencies must be closely adjacent, and the interaction strength must be large enough to overcome the frequency difference.

In most of the injection-locked oscillators (ILOs), an injection source and the oscillator are separated: one is an injector, and the other is an injectee; mutual injection is found only rarely, thereby out of concern in this paper. The first paper on the analysis of injection locking was presented by R. Adler with very complicated but elegant equations [1]. Many others followed and extend the historical document with more analytical results [2]–[10], [13], [20]. Based on [1], this paper reviews the basic fundamentals of ILO with straightforward and easy way assisting the understanding of its complicated behavior.

Many different types of injection methods and their theoretical analysis have been presented with a wide range of applications: frequency multiplication [4], [7], [11]–[29], frequency division [49]–[53], clock and data recovery [30]–[40], [44]–[47], clock distribution [41]–[43], multi-phase clock generation [48], and so on. Among those diverse applications, this review focuses on the clock multiplication and clock recovery with tuning methods reported in the previous works.

2. BACKGROUND

The first paper by R. Adler [1] introduces sinusoidal injection where both the injection and the oscillation signals are sinusoids. In an LC oscillator at resonance, as shown in Figure 1(a), the LC tank inevitably loses its energy through its parasitic resistance (R) but sustains oscillation by negative resistance ($-\boldsymbol{G_m}$) as an energy source that compensates for the loss. At the steady-state without injection ($\boldsymbol{I_{inj} = 0}$), the amplitude of oscillation is sustained where the energy loss and its supply is balanced. In that state, the oscillation and its loss in the resistor are in the same phase. When the voltage of the oscillation is at maximum, the current through the resistor is at the maximum while they are in phase. When the oscillator undergoes external injection at the same frequency, the energy from the signal is added up to the oscillator, and the oscillator maintains its frequency, but its phase gradually converges to the injector's phase if not at the same phase initially ($\boldsymbol{\theta(t = 0) =: \theta_0 \neq 0}$). Such a case when the free-running and the injector's frequencies are identical, we say they are "tuned." However, when they are "detuned," i.e., the injector's frequency ($\boldsymbol{\omega_{inj}}$) is slightly off from the oscillator's free-running resonant frequency ($\boldsymbol{\omega_{fr}}$), some deviation occurs between phases. Of course, the disturbed oscillation frequency ($\boldsymbol{\omega_{osc}}$) converges to $\boldsymbol{\omega_{inj}}$ unless injection fails to lock. When the lock is reached, which is usually the subject of analysis, the phase difference between the injection and the oscillation is non-zero. Since the LC tank is forced to oscillate off from its resonance frequency, its voltage and current phases do not match. When $\boldsymbol{\omega_{fr}}$ is higher than the forced $\boldsymbol{\omega_{inj}}$, the phase of the voltage leads the current. The externally injected sinusoid produces the phase shift.

The injection mechanism can be explained quite nicely with a so-called phasor diagram, as shown in Figure 1(b). In general, the phasor diagram analysis is performed assuming all of the given vectors exhibit the same frequency and shows the steady-state result, i.e., the vectors do not represent the transient behavior. However, in this study, we assume quasi-static dynamics where all the transients of the difference between $\boldsymbol{\omega_{inj}}$ and $\boldsymbol{\omega_{fr}}$ are represented as the sequence of the steady states in the infinitesimal time interval. Thus, the vectors shown in Figure 1(b) are slowly rotating as a function of time, just like frequency drifts in the clocking system. For example, if the frequency offset ($\boldsymbol{\Delta\omega := \omega_{inj} - \omega_{fr}}$) is zero, the phase between the injector and other signals, $\boldsymbol{\theta(t)}$ and $\boldsymbol{\phi(t)}$, converges to all zero when enough time passes as shown in Figure 1(c).

The dynamics of the injection behavior can be derived from the following differential equations. The solution is neatly represented in a closed-form. Note that the solution is periodic with $\boldsymbol{2\pi}$ and, time-vary-

ing variables are expressed as $*(t)$ to avoid confusion such as $\phi(t)$, $\theta(t)$, and $\omega_{osc}(t)$. From Figure 1(b),

$$\begin{aligned} sin\big(\phi(t)\big) &= \frac{I_{inj}\, sin\big(\theta(t)\big)}{I_{osc}} \\ &= \frac{I_{inj}\, sin\big(\theta(t)\big)}{\sqrt{I_{inj}^2 + I_{fr}^2 + 2I_{inj}I_{fr}cos(\theta(t)}}, \end{aligned} \tag{1}$$

when weak injection as assumed, $I_{inj} \ll I_{fr}$.
Thus, (1) can be approximated as

$$\frac{I_{inj}}{I_{fr}} \cdot \frac{sin\big(\theta(t)\big)}{\sqrt{\frac{I_{inj}^2}{I_{fr}^2} + 1 + 2\frac{I_{inj}}{I_{fr}}cos\big(\theta(t)\big)}} \approx \frac{I_{inj}\, sin\big(\theta(t)\big)}{I_{fr}}. \tag{2}$$

Assuming $\phi(t) \ll 1$, since $sin\big(\phi(t)\big) \approx \phi(t)$, $\phi(t)$ is expressed as

$$\phi(t) \approx \frac{I_{inj}\, sin\big(\theta(t)\big)}{I_{fr}}, \tag{3}$$

where I_{inj} and I_{fr} are fixed and given at the beginning of the injection operation.
To derive the relation between instantaneous frequency, $\omega_{osc}(t)$, and $\phi(t)$, we bring the phase relations of the LC tank analysis. For an LC tank with a loss of R, the impedance of Z can be written as

$$Z = R\big||sL|\big|\frac{1}{sC} = \frac{j\omega RL}{j\omega L + R - \omega^2 RLC}. \tag{4}$$

Then, the phase angle of Z is

$$\begin{aligned} \angle Z &= \frac{\pi}{2} - tan^{-1}\left[\frac{\omega L}{R - \omega^2 RLC}\right] \\ &= \frac{\pi}{2} - tan^{-1}\left[\frac{\omega L}{R}\cdot\frac{\omega_{fr}^2}{\omega_{fr}^2 - \omega^2}\right] \\ &\approx \frac{\pi}{2} - tan^{-1}\left[\frac{1}{2Q}\cdot\frac{\omega_{fr}}{\omega_{fr} - \omega}\right] \\ &= tan^{-1}\left[\frac{2Q}{\omega_{fr}}\cdot\big(\omega_{fr} - \omega\big)\right], \end{aligned} \tag{5}$$

where $\omega_{fr} = 1/\sqrt{LC}$, and $Q = R/\omega L$. Then,

$$tan(\angle Z) = tan\big(\phi(t)\big) \approx 2Q \cdot \frac{\omega_{osc}(t) - \omega_{fr}}{\omega_{fr}}. \tag{6}$$

Since $\phi(t) \ll 1$ again, $tan\big(\phi(t)\big) \approx \phi(t)$, (6) is rederived as

$$\phi(t) = 2Q \cdot \frac{\omega_{osc}(t) - \omega_{fr}}{\omega_{fr}}. \tag{7}$$

Substituting (3) into (7), $\omega_{osc}(t)$ is arranged as

$$\omega_{osc}(t) = \frac{I_{inj}}{I_{fr}} \cdot \frac{\omega_{fr}}{2Q} \cdot sin\big(\theta(t)\big) + \omega_{fr}. \tag{8}$$

Before solving (8) with respect to time to discover its dynamics, we will first derive the steady-state behavior of this system. In the steady state after the LC tank catches the injection signal, the disturbed frequency, $\omega_{osc}(t)$, converges to ω_{inj}, i.e., $\omega_{osc}(t = \infty) \rightarrow \omega_{inj}$. Then, from (8), $sin\big(\theta(t)\big)$ is arranged as

$$sin\big(\theta(t)\big) = -2Q \cdot \frac{I_{fr}}{I_{inj}} \cdot \frac{\big(\omega_{inj} - \omega_{fr}\big)}{\omega_{fr}}. \tag{9}$$

Since $|sin(*)| \leq 1$,

$$\left|\frac{\omega_{inj} - \omega_{fr}}{\omega_{fr}}\right| \leq \frac{I_{inj}}{I_{fr}} \cdot \frac{1}{2Q}. \tag{10}$$

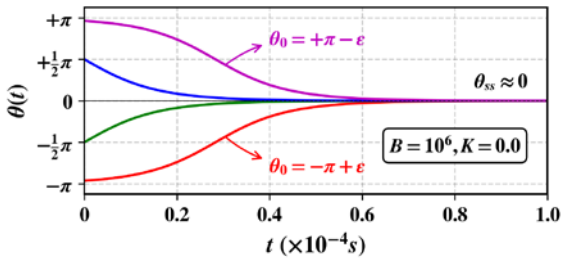
From (10), the normalized locking range increases as the injection current increases, and the tank's quality factor decreases. Since the higher quality factor indicates that the peak energy stored in the resonator is much larger than the loss caused by resistance, it is tough to perturb its frequency from the stronghold resonant frequency to other external frequency. It is noted that when the injection amplitude is fixed, there is a maximum bound of the phase shift. The maximum phase shift determines how much off the injection frequency can be from the free-running resonant frequency. When the injection frequency is far from the resonant frequency, the required phase shift between the voltage and current can be close to $\pm\pi/2$, in which case the necessary injection energy must be a lot greater than the tank itself, which destroys the purpose of the injection locking. Injection locking is supposed to control a high-energy oscillator with a tiny injector. Therefore, in this example, when the frequency discrepancy is about 10%, the injection amplitude must be greater than 10% of the tank amplitude. Otherwise, the LC tank will not “lock” to the injector.

Looking back to (8), two variables $\omega_{osc}(t)$ and $\theta(t)$ are relayed: the derivative of the phase is the angular frequency. Thus, the following relations are obtained.

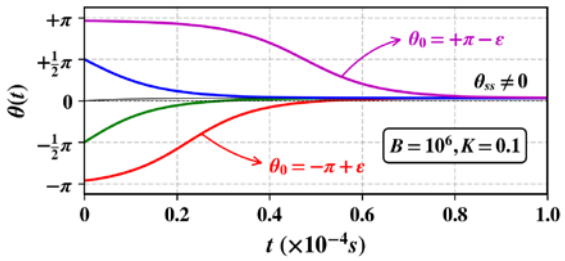
$$\frac{d\theta(t)}{dt} = \omega_{osc}(t) - \omega_{inj}. \tag{11}$$

Substituting $\omega_{osc}(t)$ from (11) into (8),

$$\frac{d\theta(t)}{dt} = -\frac{I_{inj}}{I_{fr}} \cdot \frac{\omega_{fr}}{2Q} \cdot sin\big(\theta(t)\big) - \big(\omega_{inj} - \omega_0\big).$$



(a)



(b)

Figure 2. Phase between injection and free-running vectors ($\theta(t)$) with respect to time for various initial phase (θ_0) ranging $(-\pi,+\pi)$ when B=10^6, (a) K=0.0 ($\Delta\omega = 0$), and (b) K=0.1.

(12)

Arranging (12) with the substitution of constants,

$$\frac{d\theta(t)}{dt} = -B\big(sin\big(\theta(t)\big) - k\big),$$
$$B = \frac{I_{inj}}{I_{fr}} \cdot \frac{\omega_{fr}}{2Q}, K = -2Q \cdot \frac{I_{fr}}{I_{inj}} \cdot \frac{\omega_{inj} - \omega_{fr}}{\omega_{fr}}, \tag{13}$$

where B and K are constants. If $K = 0$, meaning that $\omega_{inj} = \omega_{fr}$, its analytic solution becomes

$$tan\left[\frac{\theta(t)}{2}\right] = e^{-Bt} \cdot tan\left[\frac{\theta_0}{2}\right]. \tag{14}$$

While $\theta_0 \approx 0$, (14) is degenerated to the first-order low-pass filter as

$$\theta(t) \approx \theta_0 e^{-Bt}. \tag{15}$$

Therefore, when the injector has timing jitter, the ILO filters the injector's jitter out with a first-order transfer function. The general solution of (13) can be retrieved symbolically in (16), with the help of CAD tools such as Mathematica [54], and quite nicely displayed numerically by the library named of SciPy [55] in Python language (see Figure 2).

As shown in Figure 2(a), when the frequency offset, $\Delta\omega$ is zero, regardless of initial phase difference, θ_0, the steady-state phase difference, θ_{ss} converges to zero. However, its settling time differs; as $|\theta_0|$ increases toward $|\pi|$, it takes super linearly more time to converge toward θ_{ss}. When $|\theta_0| = |\pi|$, meta-stability causes the locking to occur in an unbounded time just like synchronization failure in a flip-flop when the setup- or hold-time violation occurs. Even the white noise in the source cannot prevent its abnormal behavior but its probability can be reduced rapidly by just allowing more settling time. When $|\theta_0|$ is smaller than $\pi/2$ (see green and blue colored lines in Figure 2(a)), it exhibits a close to a first-order settling behavior as in (15). However, when $\Delta\omega$ is non-zero, the steady-state phase error, θ_{ss} is not zero as well (see Figure 2(b)) when analyzed from the phasor-diagram derived behaviors above.

3. PHASE NOISE

Main reason for employing the ILO in clock synthesis is that it offers a wider loop bandwidth compared with the feedback-based clock generators. In this section, the phase noise is compared between various clock generators qualitatively, and the relative superiority of the ILO-combined PLL is addressed with a graphical illustration. Assuming that PLL has a 2nd-order loop, the jitter transfer function from the reference input to the output is described as

$$H(s) = \frac{\omega_n^2(1 + s/\omega_z)}{s^2 + 2s\zeta\omega_n + \omega_n^2}, \tag{17}$$

where ζ is the damping ratio, ω_n is the natural frequency, and ω_z is the stabilizing zero [56]. It has two poles and one zero and, thus, depending on their location, $H(s)$ exhibits varied characteristics. In this section, for simplicity, ζ is sufficiently high, not exhibiting peaking around the corner frequency. Since the primary noise sources are the reference and the local oscillator, phase noise profiles of the two sources must be known before applying the PLL transfer function of (17). The noise configurations of the two oscillators are

$$tan\left[\frac{\theta(t)}{2}\right] = \frac{1 - \sqrt{-1+K^2} \cdot tan\left[\frac{1}{2} \cdot \left[-B\sqrt{-1+K^2} \cdot t - 2 \cdot arctan\left[\frac{-\sqrt{-1+K^2} + K\sqrt{-1+K^2} \cdot tan\left[\frac{\theta_0}{2}\right]}{-1+K^2}\right]\right]\right]}{K} \tag{16}$$

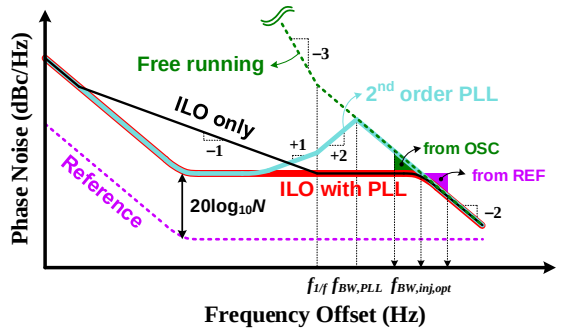


Figure 3. Conceptual phase noise illustration for various clock multipliers.

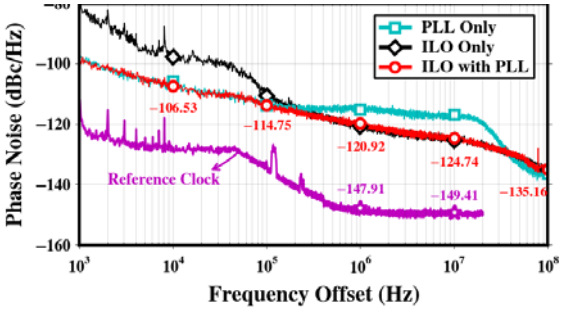


Figure 4. Measured phase noise results for various clock multipliers in [26].

illustrated in Figure 3. For the phase noise of the free-running oscillator, it exhibits flicker noise with a slope of –30 dB/dec at the modulation frequency lower than $f_{1/f}$ [57], [58]. Generally, the noise level of the reference is much lower than the one of the local oscillator as seen in the Figure 3; that's why we use the ILO. In the case of the PLL, the phase noise of the local oscillator over the PLL bandwidth ($f_{BW,PLL}$) is directly transferred to the output but is attenuated below that frequency with the +40 dB/dec slope, with the transfer function of $1 - H(s)$. Therefore, the noise from the local oscillator is shaped, showing the +20 dB/dec slope between the PLL bandwidth down to the point where the flicker noise dominates. In the flicker noise dominant region, the phase noise is not attenuated as much, thereby producing the +10 dB/dec slope. Phase noise from the reference clock, with multiplication factor of N, is up-converted as $\mathcal{L}_{ref} + 20\log_{10}N$. Therefore, the shaped phase noise from the local flicker noise is combined with the up-converted noise floor as seen in Figure 3. Depending on the phase noise spectrum of the reference and local oscillators, the output phase noise is determined by many design parameters mainly from the PLL bandwidth.

The case of the ILO incorporated PLL is presented as follows. The maximum achievable bandwidth of the PLL guaranteeing a stable operation is usually limited to around $1/10 \times f_{ref}$ as a rule of thumb [59]. On the other hands, the ILO can offer higher bandwidth compared with the PLL as discussed in [60].

$$f_{BW,inj} = \frac{\beta}{2} \times f_{ref}, \tag{18}$$

where β denotes injection strength. Equation (18) indicates that the ILO-based clock synthesis is able to offer a larger bandwidth than one of the PLL. However, since the ILO has the first-order characteristic from the injection input to the output of the oscillator, as shown in (15) of Section 2, the phase noise of the free-running oscillator is attenuated up to the flicker noise region ($f_{1/f}$), flattening the noise floor. Below this frequency, the phase noise is not filtered properly, resulting in residual phase noise with the slope of –10 dB/dec. Thus, the standalone ILO has a severe low-frequency phase noise below $f_{1/f}$. In order to reduce the overall phase noise from the local oscillator, the PLL can be incorporated to take advantage of the excellent low-frequency attenuation capability of the PLL. As shown in the simplified illustration in Figure 3, if $f_{BW,inj}$ is designed to be the frequency where the $\mathcal{L}_{ref} + 20\log_{10}N$ meets $\mathcal{L}_{fr}$, marked as $f_{BW,inj,opt}$, optimum phase noise is obtained. It is quite possible since $\mathcal{L}_{ref}$ is generally low and the primary goal is widening the overall bandwidth. In this example, if $f_{BW,inj}$ is lower than $f_{BW,inj,opt}$, phase noise from the local oscillator contributes more to the resultant output phase noise.

Typical measured results of the phase noise in various ILO-related configurations are shown in Figure 4 [26]. As demonstrated, the ILO-incorporated clock generators exhibit better noise performance than the one by the PLL-only structure. Each case is set to have the best jitter performance in its own. The PLL shows higher phase noise compared with the ILO-incorporated PLL from 200 kHz to 30 MHz, where the phase noise from the oscillator is not sufficiently filtered out. The standalone ILO exhibits almost the same noise curve down to 200 kHz where the flicker-noise starts to show up in the free-running oscillator. It is noted that the phase noise spectra of the reference clock and the free-running oscillator are typical ones presented in [26] but this case should not be construed as applying to all the configurations[1]. In summary, the injection locking, with higher bandwidth, can offer an excellent phase noise shaping of the free-running oscillator than that of the PLL can offer for the high-frequency phase noise. For the slowly-drifting phase noise such as flicker noise, the PLL removes it using the 2nd or higher-order filter embedded in the feedback system[2].

[1] Measuring the free-running frequency is challenging since it drifts over time.

[2] In this review, we simplified the analysis of the phase noise, which has very complicated equations and theories, as it has

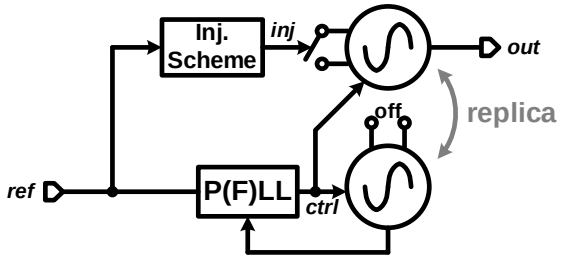
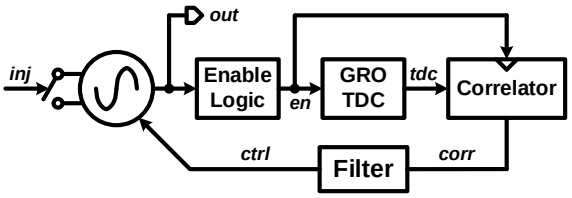


Figure 5. Block diagram of replica-based ILCM [7], [18].



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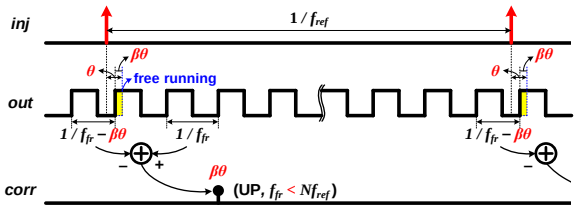


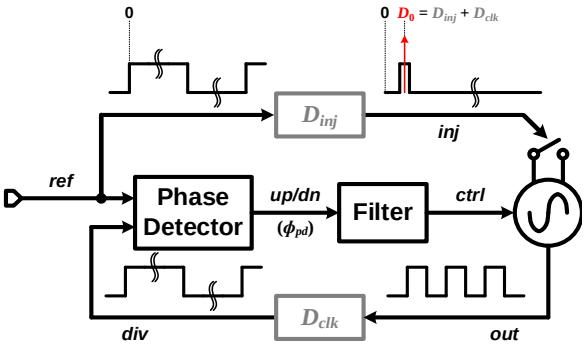
(b)

Figure 6. (a) Block diagram, and (b) timing diagram of TDC-based ILCM [11].

4. TUNING MECHANISMS

Tracking of the free-running frequency toward the injection frequency called as tuning is crucial to fully take advantage of the ILO, no matter what the ILO application is. In this section, the calibration methodology of ILCM and ILCDR is mainly discussed with several reported papers. For ILCM, effect of the mismatch called as the offset manifests itself as the reference spur, which can be a major concern in RF applications; unwanted spur at the frequency spectrum can encroach the other channels appearing as interference. In the same manner, the spur problem can be seen in the ILCDR as well. However, the most concerns in the ILCDR is the degradation of the sampling margin for incoming data, which results in poor jitter tolerance (JTOL), if the offset is not reduced adaptively.

strong bandwidth to overcome the PLL configuration has. Also, the other noise contributions from PD, charge pump, and divider are neglected.



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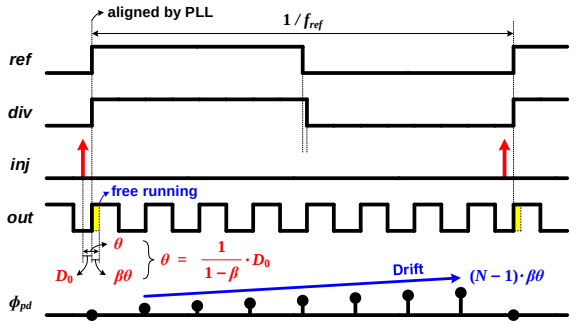

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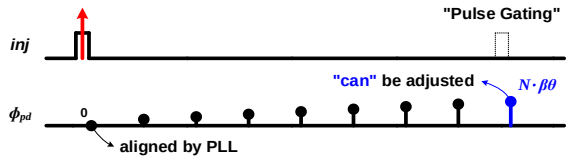
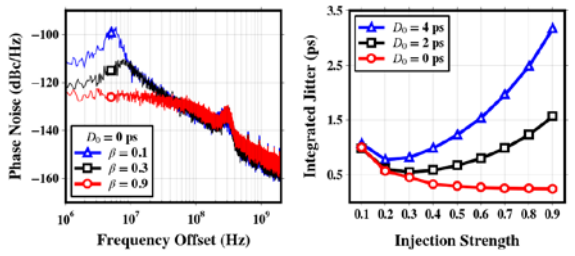


(c)

Figure 7. (a) Block diagram, and (b) timing diagram of PLL-based ILCM. (c) Timing explanation of pulse gating scheme [20],[26].

A. ILCM

The first is to use the two identical VCOs sharing the same control voltage, as shown in Figure 5 [7], [18]. One is used as a dummy oscillator whose sole purpose is to generate the control voltage in the PLL or frequency locked loop (FLL) and forward it to the main injection-locked oscillator. However, the two frequencies of the two oscillators are not identical even if closely placed in the same die due to device mismatches caused by the proximity effect and random variation. Moreover, doubled power consumption and chip area hinder it from being employed in high-performance applications.

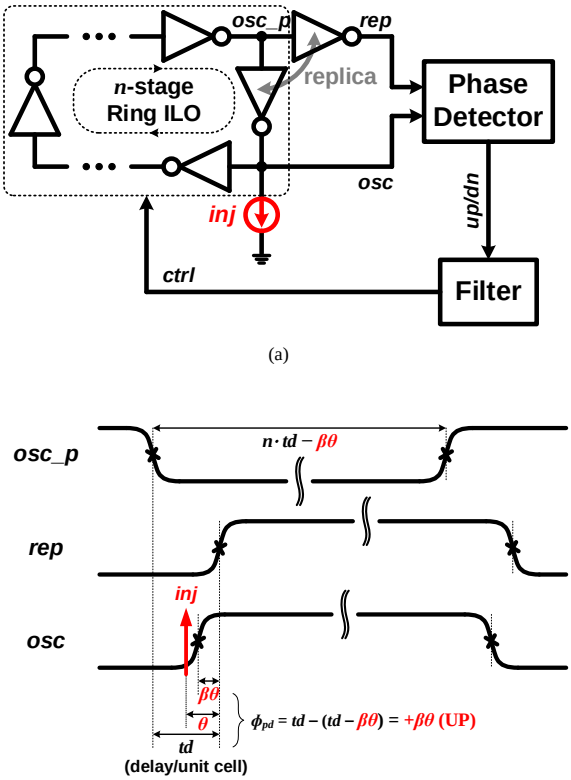


(a) (b)

Figure 8. (a) Behavioral phase-noise simulations while D_0 is zero, and (b) calculated jitter with respect to β. (N = 16, f_{ref} = 312.5 MHz, $\mathcal{L}_{fr}$ @ 1 MHz = –95 dBc/Hz, and $\mathcal{L}_{ref}$ = –160 dBc.)

In another tuning scheme shown in Figure 6(a) [11], the time-to-digital converter (TDC) is utilized for extracting injection-affected timing information. When the free-running frequency f_{fr} is smaller than the injected oscillation frequency Nf_{ref}, the injection pulls the original edges to compensate for the accumulated phase deviation during $(N-1)$ cycles. In the timing diagram of Figure 6(b), the injection causes the phase shift of $-\beta\theta$ for sustaining the lock. In other words, when the free-running oscillation frequency is low, the injection should speed up the oscillation phase to match the rate of the multiplied reference clock to maintain a locked state. When an en signal is enabled, the TDC compares two successive periods. In this case, an UP sign is generated to boost the frequency of the ILO since f_{fr} is less than Nf_{ref}. Although the offset is cancelled this way, a trade-off between the jitter performance and power dissipation must be made; the TDC resolution determines the jitter characteristic.

The third scheme is to incorporate the injection with the PLL, as illustrated in Figure 7(a) [20], [23], [25]–[27]; it is a typical erroneous concept for obtaining tuning although it is recommended for better phase noise reduction of flicker noise as described in Section 3. By directly forcing the pulse into the oscillator, which is already locked to the target frequency inside the PLL, it is falsely believed that the frequency tuning is done. However, as shown in Figure 7(a), before the injection corrects the oscillation phase, phase align is already achieved at the PD between ref and div. When the injection incurs phase deviation, there are two locations where phase alignment is tried; PLL and injection. Thus, if this two-phase modulation path is not managed correctly, the frequency offset is inevitable and unnoticed; for the worst case, it could lose the locked state. The delay D_{inj} denotes the propagation time of injection-related circuits such as pulse generator or buffers. The other delay D_{clk} indicates the delay of divider and clock buffers from the output clock (*out*) to



(a)

(b)

Figure 9. (a) Block diagram, and (b) timing diagram of replica-delay-cell based ILCM [21], [22].

the PD (*div*). Since both the delays affect the *div* signal, the delay affecting injectee can be defined as

$$D_0 = D_{inj} + D_{clk}. \tag{19}$$

This delay of D_0 should be designed carefully, having integer multiples of a period of 2π to avoid generating the frequency offset in the PLL-based ILCM. From [26], the phase offset between injection and injectee (θ) as in Figure 1(a) is obtained with respect to D_0 as

$$\theta = \frac{1}{1-\beta} \times D_0, \tag{20}$$

where β indicates the injection strength, which is less than one, assuming θ is sufficiently small[3]. Phase errors at first and N-th harmonics are zero thanks to the PLL feedback; strictly speaking, its averaged values are zero. Between that edges modified by the injection, the phase errors are piled up during $(N-1)$ cycles, but the PD does not notice whether they have the offset or not at the N-th edge (see Figure 7 (b)). To overcome the two modulation-path problem, [25] insists that zero delays of D_{inj} and D_{clk} both using direct injection

[3] For more analytic results for the effect of D_0, please refer to one of our works [26].

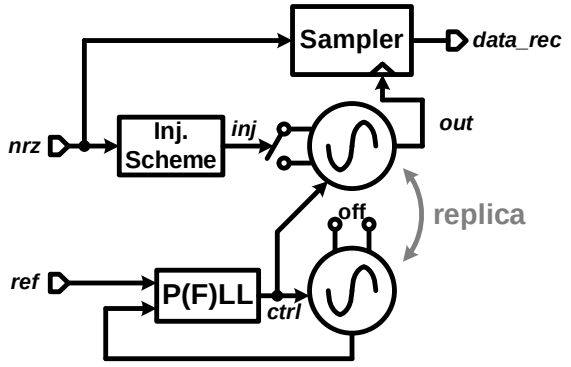


Figure 10. Block diagram of replica-based ILCDR [32], [35]–[37].

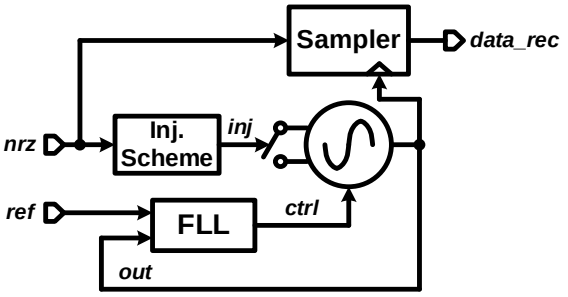


Figure 11. Block diagram of FLL-based ILCDR [34].

and sub-sampling phase detection. In [20], [26], the more refined approach is introduced as for pulse gating. As seen in typical PLL-based ILCM, the PLL loop forces the phase error to zero at the reference rate. If some of the reference edges skipped from injection by so-called pulse gating, the accumulated phase errors can be detected. At specific reference edges, one of them is missing for injection, thereby accumulated phase errors by N cycles are recognized in the PD, and we can detect the frequency drift and correct it (see Figure 7(c)). The idea itself is robust and straightforward. However, it loses the injection information with the specifically reduced rate, resulting in loss of bandwidth, and additional circuits should be incorporated, such as a delay line or a programmable edge selector.

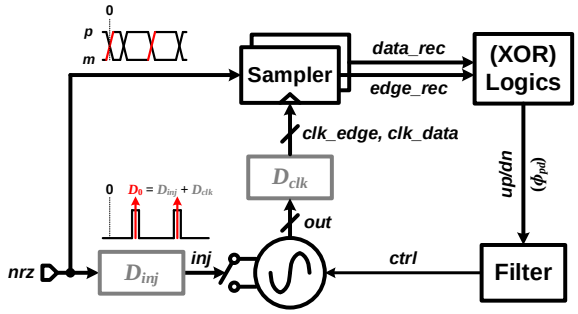
The effect of injection strength (β) and delay mismatch (D_0) on PLL-based ILCM can be found in Figure 8. As analyzed in Section 2, phase noise of the oscillator is better attenuated while the injection is strong (see Figure 8(a)). However, when D_0 is present, the accumulated jitter during $(N-1)$ cycles shows up, resulting in degradation of jitter performance (see Figure 8(b)). From these results, we can say that best jitter performance on PLL-based ILCM can be achieved with strong injection and calibration of path alignment.

In Figure 9(a), in another elaborate scheme using the ring-based ILO and duplicating a unit delay cell in the oscillator, the frequency difference can be collected [21], [22]. Unlike using a replica oscillator, as in Figure 5, it only copies one delay unit minimizing the mismatch and the area overhead. Its basic idea looks similar to the TDC-based detection by comparing two consecutive periods. However, it replicates the signal inside the oscillator, making it as a reference. The operational timing is illustrated in Figure 9(b). In the previously explained timing diagrams (Figures 6 and 7), we indicate the imaginary free-running (or undisturbed) edges with dotted lines. In the replica-delay-cell type, they realize the undisturbed edge information using the practical circuit by propagating one clock signal embedded in the oscillator. The signal of *rep* implies the untouched one under given propagation delay, td, which can be changed from the control circuits (*ctrl*). If the injection makes a negative phase shift, comparing *rep* with *osc*, which is the inverted version of *rep* with injection, the PD recognizes the polarity, whether it pulls or pushes from rep. To avoid the mismatch issues resulting from the two cells or routing layout, in [21], [22], they introduce some tricky ideas to calibrate the mismatches for more robust operation.

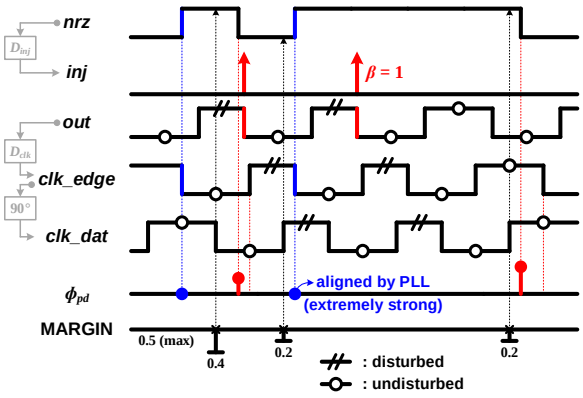
B. ILCDR

Although most of the literature [31]–[37], [39], [40] use the term CDR in ILCDR, data recovery is separate from clock recovery in the ILO, unlike the PLL-based CDR, where data recovery is achieved simultaneously with phase detection. In [30]–[38], the incoming data stream is not recovered until the ILO gains the locked state. The injection signal must be generated from the transitions of the non-return-to-zero (NRZ) data stream to integrate the ILO in the CDR efficiently. Therefore, the injection mechanism is inevitably pulse-based, which requires high bandwidth.

When an edge from the NRZ data stream is detected, a pulse is generated and injected to the oscillator to make a direct current path between the oscillator's differential nodes. The NRZ data is random and non-periodic, meaning many identical bits might persist without any transitions. While the injection pulses are regularly placed in the frequency multipliers, the ILCDR only intermittently synchronizes with the phase of the clock-recovered oscillator. Since there could be a long absence of the injecting pulses during identical bits, run-length limitation with 8B10B coding might be necessary. Between the random events, the free-running oscillator must maintain the same frequency and phase as those when an injection event occurs in between. That means injection must not interfere with the frequency and phase when injection-locked. While ILCDR has residual frequency offset, the margin for data sample is severely degraded, critical for data recovery.



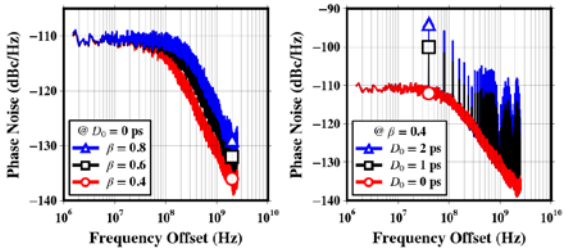
(a)



(b)

Figure 12. (a) Block diagram, and (b) timing diagram of PLL-based ILCDR [40].

Similar to the replica-based ILCM in Figure 5, replica-based ILCDR was tried in its early years [32], [35]–[37] since it is very intuitive to implement. However, it is vulnerable to device mismatches, and it consumes extra power and area. Also, the control voltage comes from the external reference clock, not the NRZ data stream of interest, resulting in the offsets. Although it has an apparent structural weakness, the fact that the NRZ stream is directly injected to the local oscillator without any filtering as in PLL-based CDR enables the ILCDR as one of the possible solutions to achieve an extremely high JTOL in some applications requiring burst-mode nature. In [35], short pulses on the rising and falling transitions of the NRZ data are produced and injected to the oscillator tuned with the replica oscillator. They use two ILOs in series for some reason: Since the recovered clock contains input jitter due to random intermittent injection events with deviated frequency, a second oscillator filters the jitter from the first oscillator. One of the shortcomings is that sampling the data with the recovered clock, the right sampling phase is not found in the loop, but selected manually. The other example of the ILCDR design for the inductively coupled interface is presented in [38]. Thanks to the inherent derivative property of the inductive link, edge pulses are generated automatically, simplifying the layout, and doubling the achievable



(a) (b)

Figure 13. Behavioral phase-noise simulations with (a) various injection strengths (b) delay offsets while skipping technique in [40] is not activated. ($\mathcal{L}_{fr}$ @ 1 MHz = –95 dBc/Hz without flicker noise.)

speed; generally, a pulse generator is speed bottleneck in ILO-based applications, since it requires a quarter of target period for successful injection [27], [35], [37]. The control voltage is sourced from one replica PLL, receiving the data stream using an overlapped transmitter/receiver chips.

As illustrated in Figure 11, the FLL-based ILCDR is reported in [34]. Since the FLL only offers the frequency acquisition, phase conflict with the injection does not happen, which is already observed in PLL-based ILCM. Like replica-based ILCDR, the main feedback loop operates under the external reference clock, not the input data stream. The frequency difference between the two causes the frequency offset, resulting in a degraded sampling margin, and worse JTOL is inevitable. In addition, even if there is no frequency offset between injector and injectee, it does not guarantee the best data sampling position; since it only generates recovered clock and delays it to sample the data with manually adjusted delay as same in the replica-based ILCDR.

As seen in Section 3, the ILO's wide bandwidth and the PLL's filtering capability of the flicker noise offer suitability of its use in the data recovery. The principal metric for evaluating the CDR's performance is JTOL, which shows how much input jitter can be tolerated, satisfying the given bit error rate (BER). For these reasons, the ILO combined with the PLL has been adopted to exhibit excellent JTOL performance. In [38], for the first time, they combine the ILO and the PLL for data recovery. However, the delay offset causing the frequency deviation is manually adjusted. To detect and to collect the mismatch information, [39] proposes a simple detecting algorithm examining successive UP/DN information from the PD. With careful selection of the injection pattern and judicious separation of conventional phase detection from offset extraction, data sampling at the middle of unit interval (UI) can be achieved. A full-functional embedded ILCDR with tuning capability of the free-running frequency and clock phase alignment is described with the injection skipping technique (see Figure 12(b)) [40].

Since it has almost the same structure as the PLL-based ILCM except for the PD algorithm, the two-point phase modulation problem is easily resolved, resulting in obtaining the highest possible performance. The PD does not detect whether it has the frequency offset or not if both transitions of the data stream are injected into the oscillator. For that to be solved, only one of the data transitions is used to injection, as noted in Figure 12(a). Since the injected signal is random, it is not as simple as in the ILCM to describe the operating principle using the timing diagram without introducing proper assumptions. In Figure 12(b), both phase alignment mechanisms exhibit the maximum adjustment strength ($\phi_{pd} = 0$ when the PLL is active and $\beta = 1$ replacing the original edge with the injector's timing), and f_{fr} is smaller than the target frequency. When $D_0 = D_{inj} + D_{clk}$ which is the same as (19) is not integer multiples of 1 UI, the phase difference caused by the frequency offset is accumulated in absence of transitions, as in the clock multiplier. In this example, the accumulated phase offset and the frequency offset also degrade the instantaneous sampling margin. As seen in Figure 12(b), the sampling margin for given NRZ streams degrades severely (in this case, 0.2 for the worst) even when the injection successfully replaces the misplaced edge unless the path delay is not controlled properly. In addition, it is noted that the consecutive identical digits (CID) also affect the overall locking range of the ILO when random data stream is injected. Adler's equations [1] are derived under assumption that the injection is made with the same frequency. However, this case deals with sub-harmonic injection with random transitions. Thus, the tolerance on how the ILO in the CDR can endure is determined by the number of CIDs, as well. The analytical expression of the locking range of the ILCDR is analyzed [40] and as follows.

$$f_L = \frac{f_{osc}^2}{\pi} \cdot \frac{\theta_{in,max}}{CID_{max}}, \tag{21}$$

assuming $f_L \ll f_{osc}$, and $\theta_{in,max}$ indicates the maximum input phase without losing lock in the given oscillator. From (21), if the CID increases, the lock may fail in the worst case.

The behavioral simulation of the PLL-based ILCDR is shown in Figure 13. In this simulation, 10 Gbs with PRBS7 NRZ stream is sourced with various β and D_0. Similar to the PLL-based ILCM, as β increases, the jitter tracking bandwidth increases. If the path delay of D_0 is non-zero, spurious tone is observed at the frequency of 40 MHz, which is equal to $10^{10}/(2^7 - 1)/2$ Hz, and its harmonics; the factor of 2 indicates that it operates with half-rate clock recovery. From these results, it is shown that the detuned PLL-based ILCDR does not guarantee the maximum sampling margin.

5. OTHER MISCELLANEOUS TOPICS

Although we have focused on ILCM and ILCDR in the previous sections, there remain more topics to be addressed. Mostly in very high-speed clock generators like U-band or K-band, the extremely high-frequency clock is usually generated using an LC resonance. Although it is possible to synthesize that high frequency clock, dividing it to a lower frequency (usually embedded in PLL) is also challenging to accomplish. The injection-locked frequency divider (ILFD) is a promising candidate for this case [49]–[53]. Next, for huge chip size, transferring clock signal from one edge to the end is of a large burden since it dissipates lots of power sometimes more than the core circuits. To mitigate such high power consumption, the injection-locked technique could be used to distribute a clock signal over the entire chip [42], [43] minimizing the cost. In addition, the ILO can be used to generate quadrature or more phases. A quadrature LC oscillator is one of the examples. Also, quadrature clock generation based on the delay-locked loop (DLL) can use ILO when its application requires a high loop bandwidth [48]. Lastly, by using the phase shift by deliberately making the frequency offset, ILO can be used in forwarded-clock system[4]. As studied in Section 2, the ILO can deliver phase-shift ranging $(-\phi/2, +\phi/2)$; thus, several works [44]–[47] use it as a delay element for data sampling in the forwarded-clock system due to its high loop bandwidth compared with the conventional CMOS delay chain.

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REFERENCES

[1] R. Adler, "A Study of Locking Phenomena in Oscillators," *Proceedings of the IRE*, vol. 34, no. 6, pp. 351–357, June 1946.

[2] K. Kurokawa, "Noise in Synchronized Oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 16, no. 4, pp. 234–240, Apr. 1968.

[3] X. Zhang, X. Zhou, and A. S. Daryoush, "A theoretical and experimental study of the noise behavior of subharmonically injection locked local oscillators," *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 5, pp. 895–902, May 1992.

[4] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

[4] In general, forwarded clocking can be categorized as CDR. However, in ILO-applied aspects, it is more suitable excluding it in ILCDR, since its injection behavior is more like ILCM, where N is 1.

[5] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sept. 2004.

[6] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi, and A. A. Abidi, "The Quadrature LC Oscillator: A Complete Portrait Based on Injection Locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sept. 2007.

[7] J. Lee and H. Wang, "Study of Subharmonically Injection-Locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[8] M. Farazian, P. S. Gudem, and L. E. Larson, "Stability and Operation of Injection-Locked Regenerative Frequency Dividers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 2006–2019, 2010.

[9] D. Dunwell and A. C. Carusone, "Modeling Oscillator Injection Locking Using the Phase Domain Response," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 2823–2833, Nov. 2013.

[10] N. D. Dalt, "An Analysis of Phase Noise in Realigned VCOs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 3, pp. 143–147, Mar. 2014.

[11] B. M. Helal, C.-M. Hsu, K. Johnson, and M. H. Perrott, "A Low Jitter Programmable Clock Multiplier Based on a Pulse Injection-Locked Oscillator With a Highly-Digital Tuning Loop," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1391–1400, May 2009.

[12] E. Monaco, M. Pozzoni, F. Svelto, and A. Mazzanti, "Injection-Locked CMOS Frequency Doublers μ-Wave and mm-Wave Applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 8, pp. 1565–1574, Aug. 2010.

[13] Y.-C. Huang and S.-I. Liu, "A 2.4-GHz Subharmonically Injection-Locked PLL With Self-Calibrated Injection Timing," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.

[14] I.-T. Lee et al., "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in ISSCC, Dig. Tech. Papers, Feb.2013, pp. 414–415.

[15] A. Musa et al., "A Compact, Low-Power and Low-Jitter Dual-Loop Injection Locked PLL Using All-Digital PVT Calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 1, pp. 50–60, Jan. 2014.

[16] J.-C. Chien et al., "A pulse-position-modulation phase-noise-reduction technique for a 2-to-16GHz injection-locked ring oscillator in 20nm CMOS," in ISSCC, Dig. Tech. Papers, Feb. 2014, pp. 52–53.

[17] A. Li, S. Zheng, J. Yin, X. Luo, and H. C. Luong, "A 21–48 GHz Subharmonic Injection-Locked Fractional-N Frequency Synthesizer for Multiband Point-to-Point Backhaul Communications," *IEEE J. Solid-State Circuits*, vol. 49, no. 8, pp. 1785–1799, Aug. 2014.

[18] W. Deng et al., "A Fully Synthesizable All-Digital PLL With Interpolative Phase Coupled Oscillator, Current-Output DAC, and Fine-Resolution Digital Varactor Using Gated Edge Injection Technique," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 68–80, Jan. 2015.

[19] C.-L. Wei, T.-K. Kuan, and S.-I. Liu, "A Subharmonically Injection-Locked PLL With Calibrated Injection Pulsewidth," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, no. 6, pp. 548–552, June 2015.

[20] A. Elkholy, M. Talegaonkar, T. Anand, and P. K. Hanumolu, "Design and Analysis of Low-Power High-Frequency Robust Sub-Harmonic Injection-Locked Clock Multipliers," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3160–3174, Dec. 2015.

[21] S. Choi, S. Yoo, Y. Lim, and J. Choi, "A PVT-Robust and Low-Jitter Ring-VCO-Based Injection-Locked Clock Multiplier With a Continuous Frequency-Tracking Loop Using a Replica-Delay Cell and a Dual-Edge Phase Detector," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1878–1889, Aug. 2016.

[22] S. Kim et al., "A 2.5GHz injection-locked ADPLL with 197fsrms integrated jitter and –65dBc reference spur using time-division dual calibration," in ISSCC, Dig. Tech. Papers, Feb. 2017, pp. 494–495.

[23] H. C. Ngo et al., "A 0.42ps-jitter –241.7dB-FOM synthesizable injection-locked PLL with noise-isolation LDO," in ISSCC, Dig. Tech. Papers, Feb. 2017, pp. 150–151.

[24] D. Coombs, A. Elkholy, R. K. Nandwana, A. Elmallah, and P. K. Hanumolu, "A 2.5-to-5.75GHz 5mW 0.3psrms-jitter cascaded ring-based digital injection-locked clock multiplier in 65nm CMOS," in ISSCC, Dig. Tech. Papers, Feb. 2017, pp. 152–153.

[25] S.-Y. Cho et al., "A 2.5–5.6 GHz Subharmonically Injection-Locked All-Digital PLL With Dual-Edge Complementary Switched Injection," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 9, pp. 2691–2702,Sep. 2018.

[26] M.-S. Choo, H.-G. Ko, S.-Y. Cho, K. Lee, and D.-K. Jeong, "An Optimum Injection-Timing Tracking Loop for 5-GHz, 1.13-mW/GHz RO-Based Injection-Locked PLL With 152-fs Integrated Jitter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 12, pp. 1819–1823, Dec. 2018.

[27] M.-S. Choo et al., "A 15-GHz, 17.8-mW, 213-fs Injection-Locked PLL With Maximized Injection Strength Using Adjustment of Phase Domain Response," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 12, pp. 1932–1936, Dec. 2019.

[28] D. Liao, Y. Zhang, F. F. Dai, Z. Chen, and Y. Wang, "An mm-Wave Synthesizer With Robust Locking Reference-Sampling PLL and Wide-Range Injection-Locked VCO," *IEEE J. Solid-State Circuits*, vol. 55, no. 3, pp. 536–546, Mar. 2020.

[29] J. Zhang et al., "A 21.7-to-41.7-GHz Injection-Locked LO Generation With a Narrowband Low-Frequency Input for Multiband 5G Communications," *IEEE Trans. Microw. Theory Tech*., vol. 68, no. 1, pp. 170–183, Jan. 2020.

[30] H.-T. Ng et al., "A second-order semidigital clock recovery circuit based on injection locking," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp.2101–2110, Dec. 2003.

[31] J.-B. Begueret, Y. Deval, C. Scarabello, J.-Y. L. Gall, and M. Pignol, "An innovative open-loop CDR based on injection-locked oscillator for high-speed data link applications," in IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2003, June 2003, pp. 313–316.

[32] M. Nogawa et al., "A 10 Gb/s burst-mode CDR IC in 0.13μm CMOS," in ISSCC, Dig. Tech. Papers, Feb. 2005, pp. 228–595.

[33] J.-H. C. Zhan, J. S. Duster, and K. T. Kornegay, "Full-rate injection-locked 10.3Gb/s clock and data recovery circuit in a 45GHz-f_T SiGe process," in Proc. IEEE Custom Integr. Circuits Conf., Sept. 2005, pp. 552–555.

[34] J. Terada et al., "A 10.3125Gb/s Burst-Mode CDR Circuit using a ΔΣ DAC," in ISSCC, Dig. Tech. Papers, Feb. 2008, pp. 226–609.

[35] J. Lee and M. Liu, "A 20-Gb/s Burst-Mode Clock and Data Recovery Circuit Using Injection-Locking Technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 619–630, Mar. 2008.

[36] K. Maruko et al., "A 1.296-to-5.184Gb/s Transceiver with 2.4mW/(Gb/s) Burst-mode CDR using Dual-Edge Injection-Locked Oscillator," in ISSCC, Dig. Tech. Papers, Feb. 2010, pp. 364–365.

[37] Y. Take, N. Miura, and T. Kuroda, "A 30 Gb/s/Link 2.2 Tb/s/mm^2 Inductively-Coupled Injection-Locking CDR for High-Speed DRAM Interface," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2552–2559,Nov. 2011.

[38] W.-S. Choi, T. Anand, G. Shu, A. Elshazly, and P. K. Hanumolu, "A Burst-Mode Digital Receiver With Programmable Input Jitter Filtering for Energy Proportional Links," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 737–748, Mar. 2015.

[39] T. Masuda et al., "A 12 Gb/s 0.9 mW/Gb/s Wide-Bandwidth Injection-Type CDR in 28 nm CMOS With Reference-Free Frequency Capture," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3204–3215, Dec. 2016.

[40] M.-S. Choo et al., "A 10-Gb/s, 0.03-mm^2, 1.28-pJ/bit Half-Rate Injection-Locked CDR With Path Mismatch Tracking Loop in a 28-nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 54, no. 10, pp. 2812–2822, Oct. 2019.

[41] L. Zhang, B. Ciftcioglu, M. Huang, and H. Wu, "Injection-Locked Clocking: A New GHz Clock Distribution Scheme," in IEEE Custom Integrated Circuits Conference 2006, Sept. 2006, pp. 785–788.

[42] M. Hossain and A. C. Carusone, "CMOS Oscillators for Clock Distribution and Injection-Locked Deskew," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2138–2153, Aug. 2009.
[43] M. Hossain and A. C. Carusone, "A 6.8mW 7.4Gb/s clock-forwarded receiver with up to 300MHz jitter tracking in 65nm CMOS," in ISSCC, Dig. Tech. Papers, Feb. 2010, pp. 158–159.
[44] S. Shekha et al., "Strong Injection Locking in Low-Q LC Oscillators: Modeling and Application in a Forwarded-Clock I/O Receiver," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 8, pp. 1818–1829, Aug. 2009.
[45] Y.-J. Kim, S.-H. Chung, and L.-S. Kim, "A Quarter-Rate Forwarded Clock Receiver Based on ILO With Low Jitter Tracking Bandwidth Variation Using Phase Shifting Phenomenon in 65 nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 8, pp. 2482–2490, Aug. 2014.
[46] Y.-J. Kim, S.-H. Chung, K.-S. Ha, S.-J. Bae, and L.-S. Kim, "A 9.6 Gb/s 0.96 mW/Gb/s Forwarded Clock Receiver With High Jitter Tolerance Using Mixing Cell Integrated Injection-Locked Oscillator," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 10, pp. 2495–2503, Oct. 2015.
[47] M. Raj, S. Saeedi, and A. Emami, "A Wideband Injection Locked Quadrature Clock Generation and Distribution Technique for an Energy-Proportional 16–32 Gb/s Optical Receiver in 28 nm FDSOI CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 10, pp. 2446–2462, Oct. 2016.
[48] D. Kim et al., "A 1.1-V 10-nm Class 6.4-Gb/s/Pin 16-Gb DDR5 SDRAM With a Phase Rotator-ILO DLL, High-Speed SerDes, and DFE/FFE Equalization Scheme for Rx/Tx," *IEEE J. Solid-State Circuits*, vol. 55, no. 1, pp. 167–177, Jan. 2020.
[49] H. R. Rategh, H. Samavati, and T. H. Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5-GHz wireless LAN receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 5, pp. 780–787, May 2000.
[50] C.-Y. Wu and C.-Y. Yu, "Design and Analysis of a Millimeter-Wave Direct Injection-Locked Frequency Divider With Large Frequency Locking Range," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 8, pp. 1649–1658, Aug. 2007.
[51] J.-C. Chien and L.-H. Lu, "Analysis and Design of Wideband Injection-Locked Ring Oscillators With Multiple-Input Injection," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1906–1915, Sept. 2007.
[52] T.-N. Luo, S.-Y. Bai, and Y.-J. E. Chen, "A 60-GHz 0.13-µm CMOS Divide-by-Three Frequency Divider," *IEEE Trans. Microw. TheoryTech.*, vol. 56, no. 11, pp. 2409–2415, Nov. 2008.
[53] M.-W. Li, P.-C. Wang, T.-H. Huang, and H.-R. Chuang, "Low-Voltage, Wide-Locking-Range, Millimeter-Wave Divide-by-5 Injection-Locked Frequency Dividers," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3,pp. 679–685, Mar. 2012.
[54] Wolfram Research Inc., Mathematica 8.0, 2010. [Online]. Available: http://www.wolfram.com
[55] P. Virtanen et al., "SciPy 1.0: Fundamental Algorithms for Scientific Computing in Python," *Nature Methods*, vol. 17, pp. 261–272, 2020.
[56] D. Fischette, "First Time, Every Time – Practical Tips for Phase-Locked Loop Design," URL: http://www.delroy.com/PLL_dir/tutorial/PLL_tutorial_slides.pdf
[57] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
[58] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 790–804, June 1999.
[59] F. M. Gardner, "Charge-Pump Phase-Lock Loops," *IEEE Transactions on Communications*, vol. 28, no. 11, pp. 1849–1858, Nov. 1980.
[60] W. Bae and D.-K. Jeong, Analysis and Design of CMOS Clocking Circuits for Low Phase Noise. London, U.K.: Institution of Engineering and Technology, 2020.

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