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Ultradense 2-to-4 decoder in quantum-dot cellular automata technology based on MV32 gate

Akram Abbasizadeh[1] | **Mohammad Mosleh**[2]

[1]Department of Computer Engineering, Karoon Institute of Higher Education, Ahvaz, Iran

[2]Department of Computer Engineering, Dezful Branch, Islamic Azad University, Dezful, Iran

Correspondence
Mohammad Mosleh, Department of Computer Engineering, Dezful Branch, Islamic Azad University, Dezful, Iran.
Email: Mosleh@iaud.ac.ir

Quantum-dot cellular automata (QCA) is an alternative complementary metal-oxide-semiconductor (CMOS) technology that is used to implement high-speed logical circuits at the atomic or molecular scale. In this study, an optimal 2-to-4 decoder in QCA is presented. The proposed QCA decoder is designed using a new formulation based on the MV32 gate. Notably, the MV32 gate has three inputs and two outputs, which is equivalent two 3-input majority gates, and operates based on cellular interactions. A multilayer design is suggested for the proposed decoder. Subsequently, a new and efficient 3-to-8 QCA decoder architecture is presented using the proposed 2-to-4 QCA decoder. The simulation results of the QCADesigner 2.0.3 software show that the proposed decoders perform well. Comparisons show that the proposed 2-to-4 QCA decoder is superior to the previously proposed ones in terms of cell count, occupied area, and delay.

KEYWORDS
decoder circuit, majority gate, MV32 gate, nanotechnology, quantum-dot cellular automata

1 | INTRODUCTION

CMOS technology has been considered a standard for implementing very large-scale integration circuits over the past decades. However, because of limitations such as low switching speed, high complexity, and high power consumption, an appropriate alternative to this technology is required [1,2].

Quantum-dot cellular automata (QCA) is an alternative CMOS technology. Because of its considerably small size at the atomic or molecular scale, significantly low power consumption, and high switching speed, it can be used as an appropriate option [3–5].

Thus far, several integrated and sequential circuits, such as adders [6–8], multiplier [9,10], decoder [11], memory [12], and flip flops [13,14], have been implemented with QCA technology.

In digital electronics, the decoder is a hybrid circuit that converts binary information from n inputs to 2^n outputs. In addition, decoders have an Enable input, which can enable or disable the decoder. Notably, decoder circuits can be used in many applications, such as data demultiplexing, seven segment display, memory addresses decoding, microprocessor commands decoding, and microprocessor inputs-outputs selection [11,15].

Thus far, many research works have addressed the design and implementation of decoder circuits in QCA technology. Some of the most important among them are reviewed here.

In 2006, a configurable logic block (CLB) block was designed by Lantz and Peskin for a field-programmable gate array (FPGA) architecture by using a 2-to-4 decoder, which included eight 3-input majority gates [16]. The simulation results revealed that the decoder had 318 cells in an area of 0.50 μm^2, and a delay of seven clock phases.

In 2011, Kianpour and Sabbaghi-Nadoshan designed and implemented another 2-to-4 decoder, in which five 5-input majority gates were used [17]. It had 270 cells in an area of 0.38 μm^2 and a delay of seven clock phases; it was used as a module for designing an n-to-2^n decoder.

In another study, Xilinx CLB and FPGA elements were designed and simulated by Kianpour and Sabbaghi-Nadoshan in 2014, and all the CLB components were investigated to reduce the complexity in terms of the number of cells; they proposed a novel 2-to-4 decoder that included eight 3-input majority gates in one layer [18]. The simulation results of the QCADesigner indicated that the proposed decoder had 268 cells in an area of 0.30 μm^2 and a delay of seven clock phases.

In 2015, Jeon presented a 2-to-4 decoder that comprised four 5-input majority gates to ensure structural regularity to be easily extensible to 3-to-8 or 4-to-16 decoders and readily connected with other circuits [19]. The decoder had 219 cells and a delay of four clock phases.

In 2016, De and others presented an effective programmable logic array design using a new XOR gate, in which a 2-to-4 decoder was introduced without Enable input; the decoder was designed using four 3-input majority gates [13], which comprised 93 cells and had a delay of four clock phases.

In 2017, Kumar and Sasamal presented a 2-to-4 decoder in which six 3-input majority gates were used in one layer [20]. The simulation results showed that the proposed decoder had 212 cells in an area of 0.25 μm^2 and a delay of six clock phases.

In 2018, Sharizadeh and Navimipour proposed a modular decoder design using the QCA technology. The proposed design was a modular approach for devising higher-order decoders using lower-order cascade decoders. The proposed 2-to-4 decoder had four 5-input majority gates [15]. The results showed that the proposed design had 193 cells in an area of 0.22 μm^2 and a delay of three clock phases.

Finally, in 2018, Navimipour and Seyyedi designed and implemented a new 2-to-4 decoder with a small area and complexity. The proposed scheme was designed using four 5-input majority gates in three layers [11]. The simulation results of the QCADesigner tool showed that the proposed QCA-based decoder had 88 cells in an area of 0.06 μm^2 and a delay of two clock phases.

In this study, a new 2-to-4 decoder in QCA is presented with a different formulation based on the MV32 gate. Notably, the MV32 gate is a circuit with three inputs and two outputs, with each output providing a 3-input majority gate. In the proposed decoder architecture, two MV32 gates and four 3-input majority gates have been used. The proposed design is simulated using the QCADesigner 2.0.3 software. The comparison results show that, compared with other decoders, the proposed decoder is more optimal in terms of the number of consumed cells, covered area, and delay.

In the second section, we outline the QCA principles and fundamentals; in addition, we introduce the MV32 gate and the architecture of a 2-to-4 decoder. In the third section, the design of the proposed 2-to-4 decoder is presented using the new formulation based on the MV32 gate. In the fourth section, using the QCADesigner software, the proposed method is simulated, and the results are presented. Finally, this paper ends with the conclusion section.

2 | BASICS OF RESEARCH

In this section, the QCA principles and basics are presented first. Then, the MV32 gate is addressed, and finally, the structure of the 2-to-4 decoder with Enable input is introduced.

2.1 | Basics and principles of QCA

The QCA technology is a new technology for designing and implementing nanoscale logic circuits. A quantum cell, which is the basic computing element in QCA, comprises four quantum dots in the four corners of a square along with two electrons that can be placed at the quantum dots and transfers between the dots via tunneling. On the basis of Coulomb law and electron repulsion, the two electrons are diagonally placed in the square and two polarities of –1 and+ 1 are created, which are equivalent to zero and one logic, respectively (Figure 1) [21].

In the QCA technology, a cells' sequence that transmits the input signal to the output is called the QCA wire. There are the following two commonly used base structures in QCA circuits: the inverter gate (NOT) and 3-input majority gate (MV3). The circuit and cellular schematic of the inverter gate and 3-input majority gate with A, B, and C inputs are shown in Figure 2.

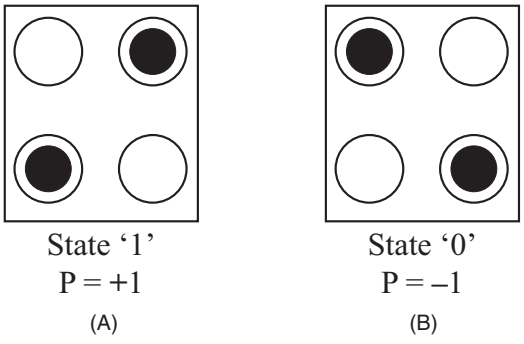

FIGURE 1 QCA cell: (A) P = +1 polarity and (B) P = –1 polarity

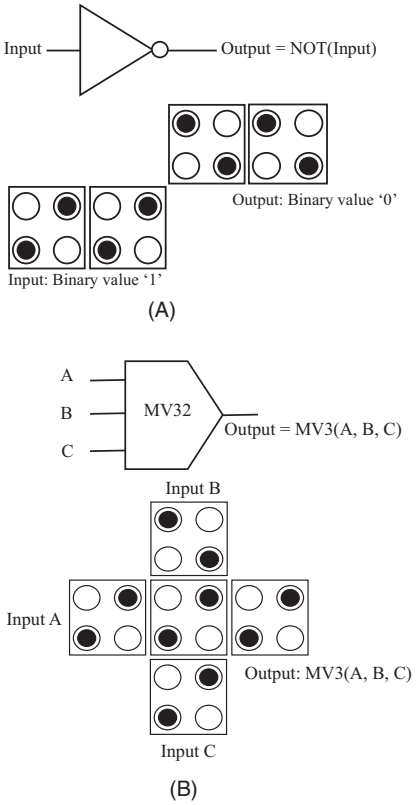

FIGURE 2 Circuit and cell display: (A) Inverter gate and (B) 3-input majority gate

If one of the inputs of the 3-input majority gate becomes zero or one, the AND and OR gates are logically generated, respectively.

The QCA circuits require clock pulse for supplying energy for circuit components and controlling data transfer in the cells. The clock pulse facilitates the movement of electrons inside the cells. The design of a clocking, as shown in Figure 3, consists of the following four phases [22,23].

Switch: In this phase, the barrier forces against the movement of electrons within each cell begin to increase, and the movement of electrons slowly decreases.

Hold: In this phase, the barrier forces against the movement of electrons inside the cell reach their maximum limit, and the location of the electrons remains constant.

Release: In this phase, the barrier force decreases, and the electrons are slowly released.

Relax: In this phase, the cell has no polarization, and the electrons move freely inside the cell.

2.2 | Introduction to the MV32 gate

The MV32 gate is designed using a combination of two QCA designs shown in Figure 4. Each of these designs

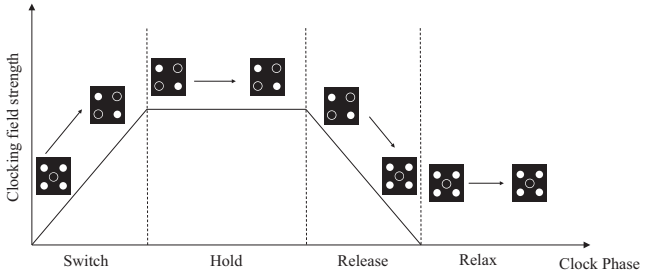

FIGURE 3 Four clock phases in QCA

comprises nine cells and generates output at two clock phases [24]. Their functions are described in detail as follows.

In Figure 4A, at the first clock zone (clock zone 0), the cells that are marked with 1, 2, 4, 5, 6, and 7 go to the Switch state. Subsequently, the *A* input polarity is copied to cell 5, *B* input polarity to cell 2, and *C* input polarity to cell 7.

At clock zone 1, cells 2, 5, and 7 go to the Hold state and sustain their polarities, and they can also influence their neighbor cells that are placed at clock zone 1.

Cell 3, the target cell, and cell $O1$ are at clock zone 1, and they go to the Switch state and obtain their polarities via the sum up of the electrostatic energies that come from the neighbor cells. Cell 3, the target cell, and cell $O1$ form a simple inverter gate.

The polarity of cell 3 can be calculated using a 3-input majority gate $\mathrm{MV3}(A.B.C)$, which applies the inverse of its polarity $\overline{\mathrm{MV3}(A.B.C)}$ to the target cell.

Therefore, the target cell is influenced by 3 forces from cells 3, 2, and 5, respectively, which are its neighbors. These forces are represented by $f1 = A, f2 = B$, and $f3 = \overline{\mathrm{MV3}(A.B.C)}$. The outcome of these forces determines the polarity of output $O1$.

Moreover, the function of the target cell is evaluated on the basis of physical relations. Notably, the size of each QCA cell has been considered $18 \times 18\ \mathrm{nm}^2$ so that the distance between neighbor cells is 2 nm. Generally, the energy between two electron charges is calculated as follows:

$$U = \frac{kq_1q_2}{r} \tag{1}$$

where k denotes Coulomb constant, q_1 and q_2 the electric charges, and r the distance between both the electric charges.

Substituting the values of k, q_1, and q_2 in the numerator of (1), we obtain

$$\begin{aligned} kq_1q_2 &= 9\ \ 10^9\ \ (1.6)^{-2}\ \ 10^{38} \\ &= 23.04\ \ 10^{29}. \end{aligned} \tag{2}$$

U_T, which is the summation of the kink energies, is calculated as follows:

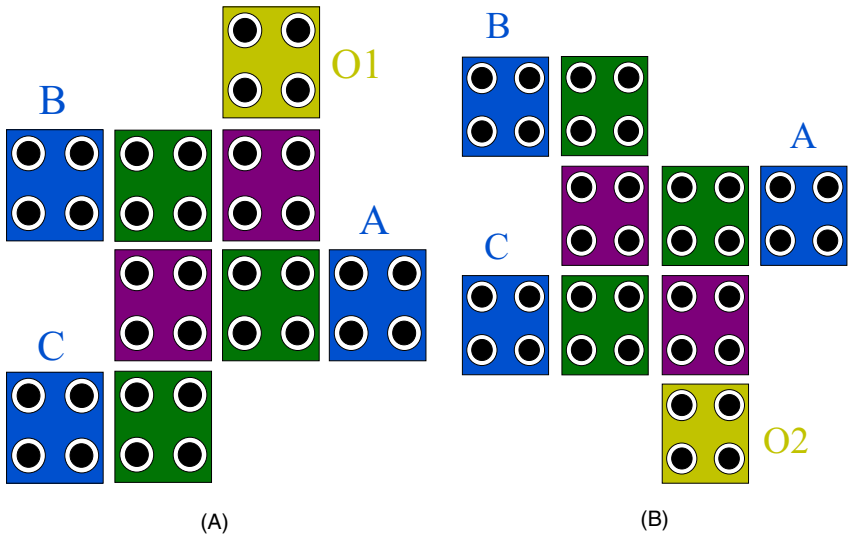

FIGURE 4 (A) First QCA scheme and (B) second QCA scheme

$$U_T = \sum_{i=1}^{2} U_i. \tag{3}$$

In the following, using the introduced physical relations, we obtain the total energy of cells, 2, 3, and 5 on the target cell, for example, for arbitrary inputs $A = 1$, $B = 1$, and $C = 0$, two different polarities are considered for the target cell as follows:

With comparison of the achieved results in Tables 1 and 2, the electrons in the target cell are positioned in the state Figure 5A which is more stable and has lower kink

TABLE 1 Total energy of three cells in Figure 5A

Electron *y*	Electron *x*
$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{18.11\times10^{-9}} \approx 1.27\times10^{-20}\ (J)$	$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.52\times10^{-20}\ (J)$
$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.152\times10^{-20}\ (J)$	$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{42.04\times10^{-9}} \approx 0.548\times10^{-20}\ (J)$
$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{42.01\times10^{-9}} \approx 0.548\times10^{-20}\ (J)$	$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.152\times10^{-20}\ (J)$
$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{20\times10^{-9}} \approx 1.152\times10^{-20}\ (J)$	$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{18.11\times10^{-9}} \approx 1.272\times10^{-20}\ (J)$
$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{38.05\times10^{-9}} \approx 0.605\times10^{-20}\ (J)$	$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{28.28\times10^{-9}} \approx 0.814\times10^{-20}\ (J)$
$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{28.28\times10^{-9}} \approx 0.814\times10^{-20}\ (J)$	$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{38.05\times10^{-9}} \approx 0.605\times10^{-20}\ (J)$
$U_{T_y} = \sum_{i=1}^{6} U_i = 5.543\times10^{-20}\ (J)$	$U_{T_x} = \sum_{i=1}^{6} U_i = 5.543\times10^{-20}\ (J)$
$U_{Ta} = \sum_{i=x,y} U_{T_i} = 11.08\times10^{-20}\ (J)$	

TABLE 2 Total energy of the three cells in Figure 5B

Electron *y*	Electron *x*
$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{2\times10^{-9}} \approx 1.27\times10^{-20}\ (J)$	$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{26.90\times10^{-9}} \approx 0.856\times10^{-20}\ (J)$
$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{26.90\times10^{-9}} \approx 0.856\times10^{-20}\ (J)$	$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{38\times10^{-9}} \approx 0.606\times10^{-20}\ (J)$
$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{26.90\times10^{-9}} \approx 0.856\times10^{-20}\ (J)$	$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{38\times10^{-9}} \approx 0.856\times10^{-20}\ (J)$
$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{2\times10^{-9}} \approx 11.52\times10^{-20}\ (J)$	$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{26.90\times10^{-9}} \approx 0.856\times10^{-20}\ (J)$
$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{20.09\times10^{-9}} \approx 1.142\times10^{-20}\ (J)$	$U_5 = \frac{A}{r_5} = \frac{23.04\times10^{-29}}{42.59\times10^{-9}} \approx 0.540\times10^{-20}\ (J)$
$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{20.09\times10^{-9}} \approx 1.142\times10^{-20}\ (J)$	$U_6 = \frac{A}{r_6} = \frac{23.04\times10^{-29}}{42.59\times10^{-9}} \approx 0.540\times10^{-20}\ (J)$
$U_{T_y} = \sum_{i=1}^{6} U_i = 16.786\times10^{-20}\ (J)$	$U_{T_x} = \sum_{i=1}^{6} U_i = 4.182\times10^{-20}\ (J)$
$U_{Tb} = \sum_{i=x,y} U_{T_i} = 20.968\times10^{-20}\ (J)$	

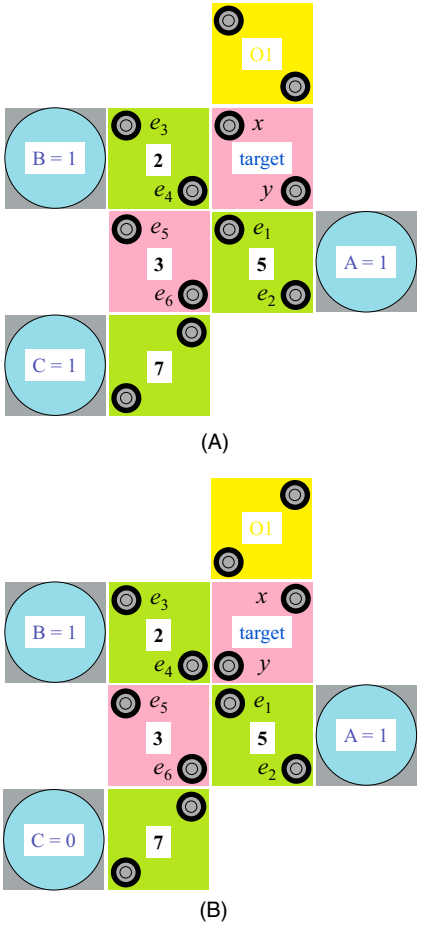

FIGURE 5 (A) One value in target cell, and (B) zero value in target cell

energy. For other input values, calculations are performed similarly.

Therefore, the polarity of the target cell is obtained according to Table 3.

$$\begin{aligned}&\text{target output polarization} = O1\\&= \text{MV3}(\overline{\text{MV3}\,(A.B.C)}A, B = B\overline{C} + AB + A\overline{C}.\end{aligned} \tag{4}$$

TABLE 3 Truth table of the structure in Figure 4A

A	*B*	*C*	*O1*
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

TABLE 4 Truth table of the structure in Figure 4B

A	*B*	*C*	*O2*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

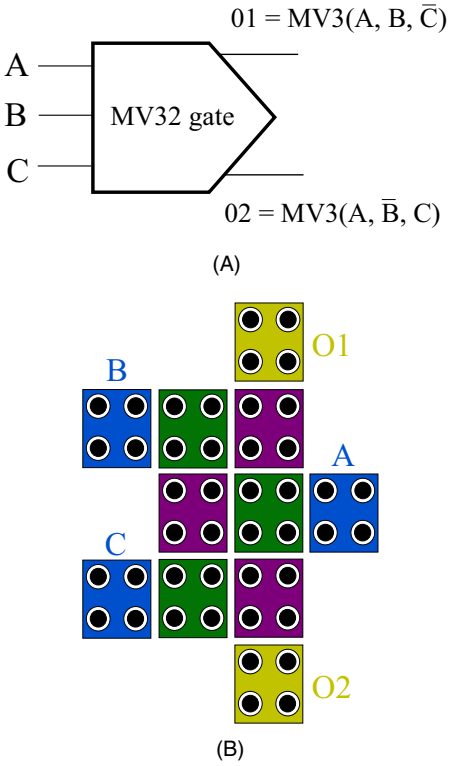

FIGURE 6 MV32 gate: (A) circuit display and (B) QCA layout

The second structure, which is depicted in Figure 4B, works in the same manner. The polarity of cell 3 is calculated as MV3 (*A*, *B*, *C*), and the polarities of the target cell and *O*2 can be calculated according to Table 4.

$$\begin{aligned}&\text{target output polarization} = O2 =\\&\text{MV3}(\overline{\text{MV3}\,(A.B.C)}A, C = A\overline{B} + AC + \overline{B}C.\end{aligned} \tag{5}$$

By combining both the designs, an MV32 gate with three inputs and two outputs is created, as depicted in Figure 6, and it has 11 cells and generates output in two clock phases.

TABLE 5 Truth table of the 2-to-4 decoder with Enable input

Enable	*X*	*Y*	*D*1	*D*2	*D*3	*D*4
0	0	0	0	0	0	0
0	0	1	0	0	0	0
0	1	0	0	0	0	0
0	1	1	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1

2.3 | 2-to-4 decoder architecture

One of the most widely used hybrid logic circuits is a decoder, which is used in various applications, such as data demultiplexing, seven segment displays, and memory-address decoding. Notably, decoders convert the binary information from n inputs to 2^n outputs. A 2-to-4 decoder with Enable input has two *X* and *Y* inputs and four outputs *D*1, *D*2, *D*3, and *D*4. When Enable pin is disabled (ie, Enable = 0), all the outputs are inactive, and if it is enabled (ie, Enable = 1), the outputs are based on the truth table presented in Table 5.

Therefore, the output equations are obtained as follows:

$$D1(\text{Enable}, X, Y) = \text{Enable}\,\overline{XY}, \tag{6}$$

$$D2(\text{Enable}, X, Y) = \text{Enable}\,\overline{X}Y, \tag{7}$$

$$D3(\text{Enable}, X, Y) = \text{Enable}\,X\overline{Y}, \tag{8}$$

$$D4(\text{Enable}, X, Y) = \text{Enable}\,XY. \tag{9}$$

3 | PROPOSE DECODERS IN QCA

In this section, a novel and efficient architecture is first proposed for a 2-to-4 QCA decoder, and then a new and efficient architecture is provided for a 3-to-8 decoder architecture by using the proposed 2-to-4 QCA decoder.

3.1 | Proposed 2-to-4 QCA Decoder

Thus far, various designs of a 2-to-4 decoder have been proposed in QCA, each of which has attempted to reduce the number of cells and area, as well as the clock phases, and a few of them have been reviewed at the start of this study. In this section, we present a new 2-to-4 decoder design that is based on a new formulation of the MV32 gate.

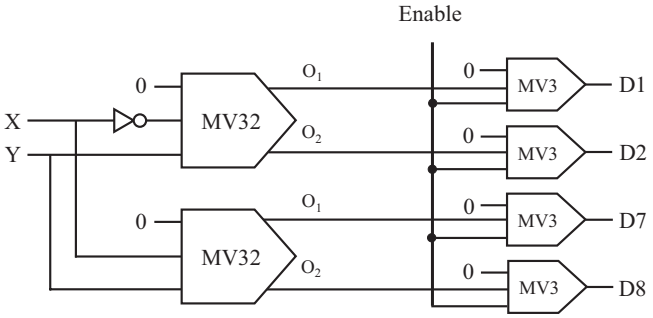

FIGURE 7 Circuit display of proposed 2-to-4 decoder

Given the outputs of MV32 in (10) and (11), when $A = 0$, $B = \overline{X}$, and $C = Y$, we have the following:

$$\text{MV32}\left(0, \overline{X}, Y\right) = \begin{cases} O1 = \text{MV3}\left(0, \overline{X}, \overline{Y}\right), \\ O2 = \text{MV3}\,(0, X, Y). \end{cases} \tag{10}$$

and when $A = 0$, $B = X$, and $C = Y$, we have the following:

$$\text{MV32}\,(0, X, Y) = \begin{cases} O1 = \text{MV3}\left(0, X, \overline{Y}\right), \\ O2 = \text{MV3}\left(0, \overline{X}, Y\right). \end{cases} \tag{11}$$

Therefore, the outputs of the decoder are derived as follows:

$$D1 = \text{MV3}\left(0, \text{MV3}\left(0, \overline{X}, \overline{Y}\right), \text{Enable}\right) = \text{Enable}\,\overline{XY}, \tag{12}$$

$$D2 = \text{MV3}\left(0, \text{MV3}\left(0, X, \overline{Y}\right), \text{Enable}\right) = \text{Enable}\,\overline{X}Y, \tag{13}$$

$$D3 = \text{MV3}\left(0, \text{MV3}\left(0, \overline{X}, Y\right), \text{Enable}\right) = \text{Enable}\,X\overline{Y}, \tag{14}$$

$$D4 = \text{MV3}\,(0, \text{MV3}\,(0, X, Y), \text{Enable}) = \text{Enable}\,XY. \tag{15}$$

The circuit schematic of the proposed design is presented in Figure 7.

The implementation of the proposed design in QCA is depicted in Figure 8. As can be seen, the design has been implemented in three layers that have 62 cells, and the delay of three clock phases and area of 0.03 μm^2.

3.2 | Proposed 3-to-8 QCA Decoder

The output functions of the 3-to-8 decoder can be expressed as follows:

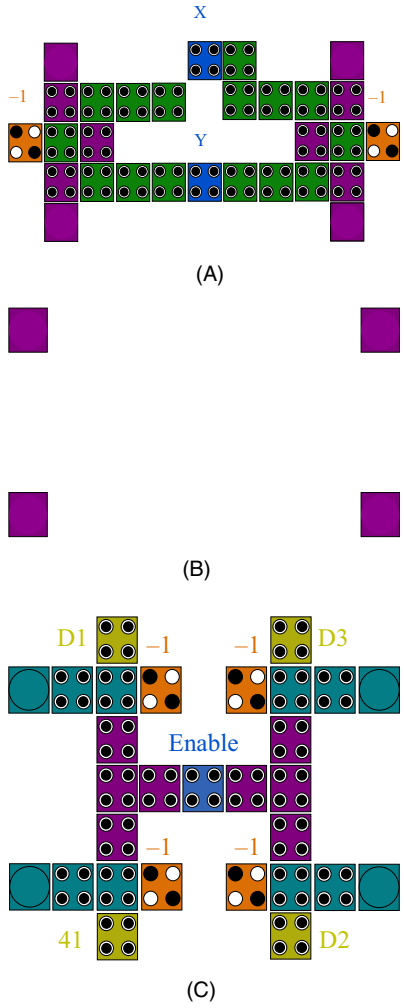

FIGURE 8 Three layers of proposed 2-to-4 QCA decoder (A) layer 1 (main layer), (B) layer 2 (via layer), and (C) layer 3

$$D1 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, \overline{X}, \overline{Y}\right), \overline{Z}\right) = \overline{XYZ}, \quad (16)$$

$$D2 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, \overline{X}, \overline{Y}\right), Z\right) = \overline{XY}Z, \quad (17)$$

$$D3 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, \overline{X}, Y\right), \overline{Z}\right) = \overline{X}Y\overline{Z}, \quad (18)$$

$$D4 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, \overline{X}, Y\right), Z\right) = \overline{X}YZ, \quad (19)$$

$$D5 = \mathrm{MV3}\left(0, MV3\left(0, X, \overline{Y}\right), \overline{Z}\right) = X\overline{YZ}, \quad (20)$$

$$D6 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, X, \overline{Y}\right), Z\right) = X\overline{Y}Z, \quad (21)$$

$$D7 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, X, Y\right), \overline{Z}\right) = XY\overline{Z}, \quad (22)$$

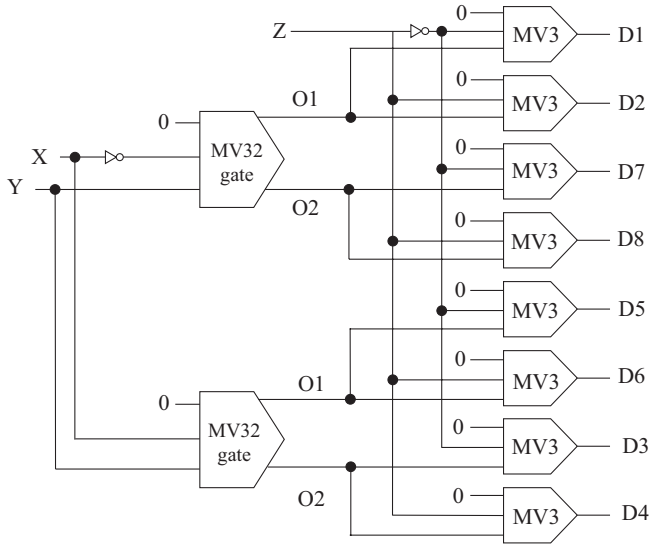

FIGURE 9 Circuit display of proposed 3-to-8 decoder

$$D8 = \mathrm{MV3}\left(0, \mathrm{MV3}\left(0, X, Y\right), Z\right) = XYZ. \quad (23)$$

The circuit diagram of the proposed 3-to-8 QCA decoder is depicted in Figure 9.

The implementation of the proposed 3-to-8 QCA decoder is illustrated in Figure 10. As can be observed, the design has been implemented in three layers that have 140 cells, and the delay of four clock phases and area of 0.09 μm^2.

4 | SIMULATION RESULTS

The proposed 2-to- 4 decoder was simulated using the QCADesigner 2.0.3 software. All the simulation conditions and parameters have default values in the QCADesigner, as shown in Table 6.

As shown in Table 6, the size of each quantum cell is 18 nm × 18 nm. In addition, there is a distance of 2 nm between the neighboring cells. Therefore, the occupied area of a QCA layout can be calculated as follows:

$$\begin{aligned}\text{Area} = &(\text{maximum longitudinal cell number}) \\ &\times(\text{maximum transversal cell number}) \times 400\,\text{nm}^2.\end{aligned} \quad (24)$$

The simulation results of the proposed 2-to-4 decoder are shown for all X, Y, and Enable input modes in Figure 11. As can be seen, the proposed decoder works satisfactorily, and the outputs are achieved with a delay of three clock phases. In addition, it has 62 cells in the area of 0.03 μm^2.

A generalized cost function for QCA circuits was first introduced by Liu and others as follows [25]:

$$\mathrm{QCA}_{\mathrm{cost}} = \left(M^k + I + C^l\right) \times T^p. \quad k.l.p \geq 1. \quad (25)$$

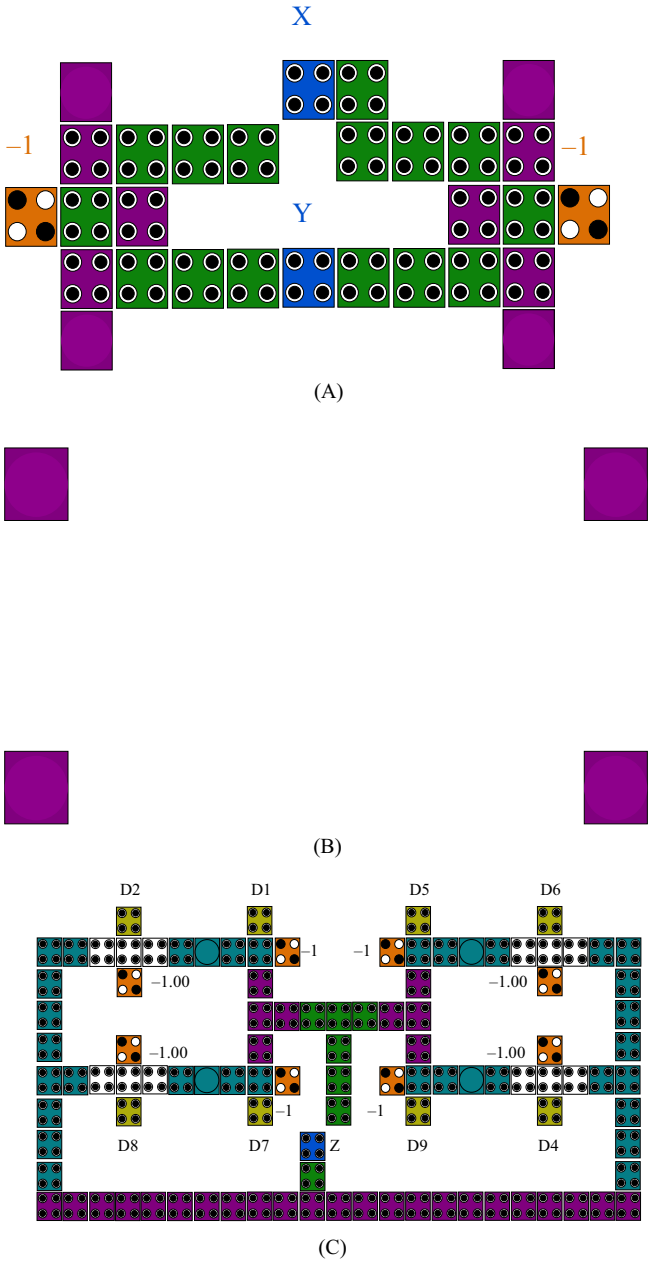

FIGURE 10 Three layers of proposed 3-to-8 QCA decoder (A) layer 1 (main layer), (B) layer 2 (via layer), and (C) layer 3

where M denotes the number of majority gates, I the number of inverters, C the number of crossovers, and T the delay of the circuit. Moreover, k, l, and p denote the exponential weightings for majority gate count, crossover count, and delay, respectively.

Because the number of the majority gates is related to complexity and energy dissipation, a double weight is considered for the M parameter, that is, $k = 2$. In addition, this issue is also true for the C parameter, as the number of crossovers is related to the complexity and fabrication difficulty. Therefore, in the general case, the QCA cost function can be expressed as follows:

$$\mathrm{QCA}_{\mathrm{cost}} = \left(M^2 + I + C^2\right) T. \tag{26}$$

TABLE 6 Utilized parameters for "bistable approximation" engine in our simulation

Parameters	Values
Number of samples	12 800
Convergence tolerance	0.001000
Radius of effect (nm)	65.000000
Relative permittivity	12.900000
Clock high	9.800000e–022
Clock low	3.800000e–023
Clock shift	0.00000e + 000
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iteration per sample	100
Cell width	18.0 nm
Cell height	18.0 nm
Dot diameter	5.0000

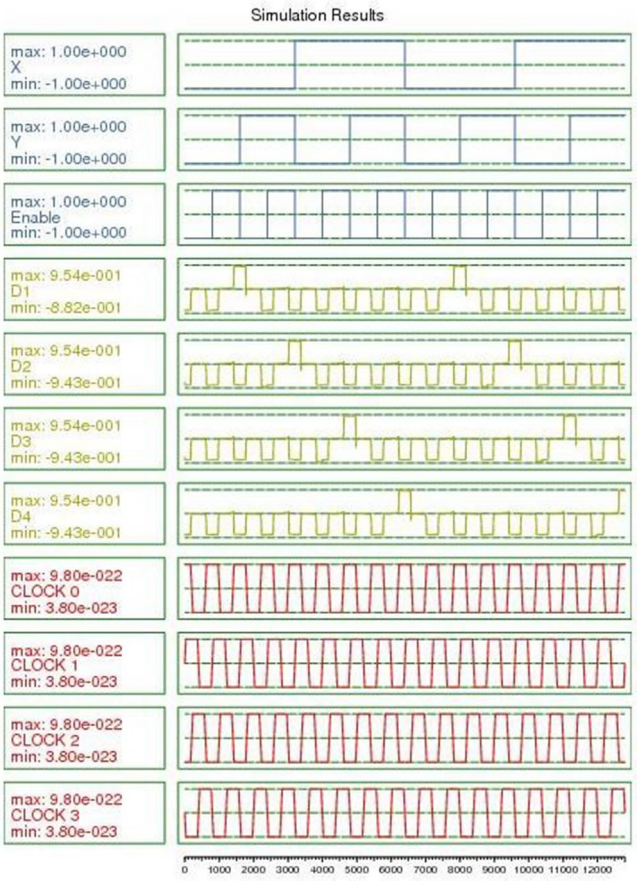

FIGURE 11 Simulation results of proposed 2-to-4 decoder in QCA

Notably, the value of the C parameter between multilayer crossovers, C_{ml}, and coplanar crossbar C_{cp} are different from each other, such that $C_{\mathrm{ml}} = 3 \times C_{\mathrm{cp}}$.

TABLE 7 Comparison table for QCA decoders

Design	#Cells	Area (μm^2)	Clock zones	#Layer(s)	Cost function
[16]	318	0.50	7	1	231
[19]	219	N/A	4	1	84
[20]	212	0.25	6	1	310.5
[15]	193	0.22	3	1	313.5
[13]	93	0.09	4	1	20 (without the Enable input)
[11]	88	0.06	2	3	1809
Proposed	62	0.03	3	3	217.5*

*The MV32 gate is regarded as two majority gates

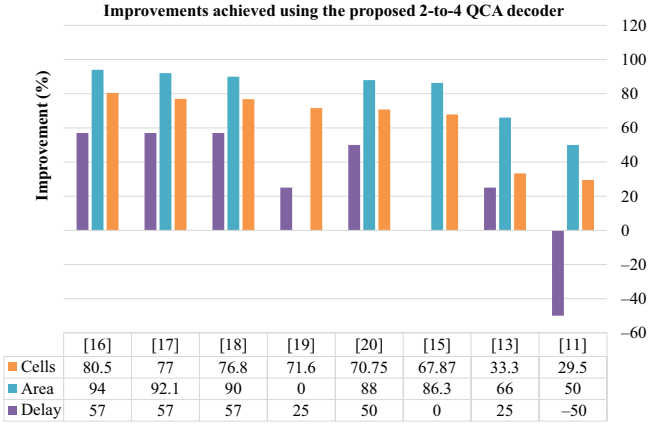

FIGURE 12 Improvements obtained using the proposed 2-to-4 decoder in QCA compared with the previously conducted works

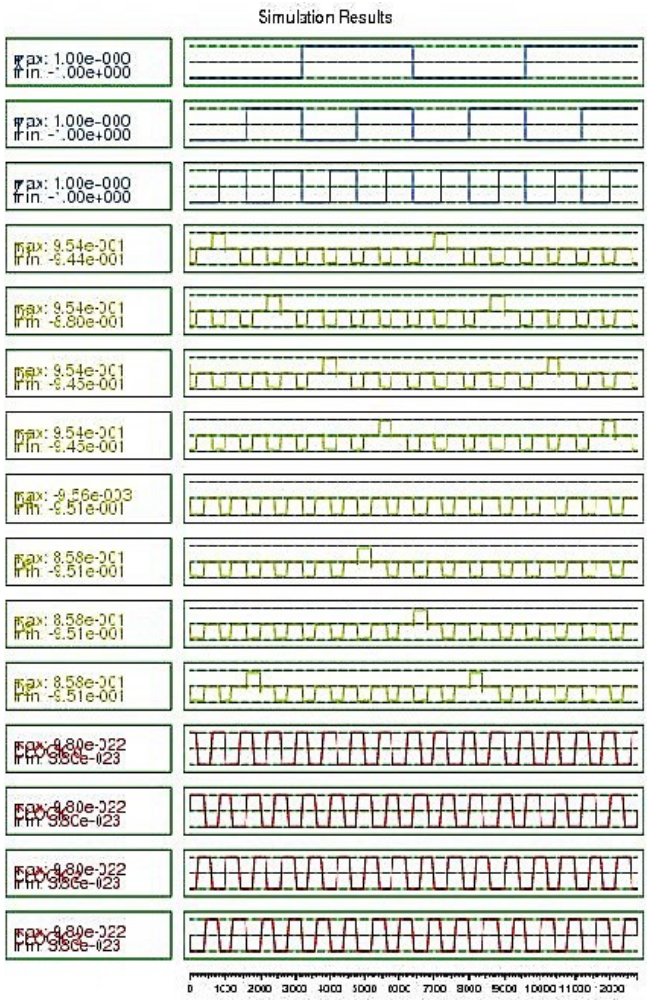

FIGURE 13 Simulation results of proposed 3-to-8 decoder in QCA

In Table 7, the proposed decoder is compared with the previously proposed ones in terms of the number of cells, occupied area, number of clock phases, number of layers, and cost function. In addition, in Figure 12, the percentage improvement in the proposed scheme is compared with those of previously proposed designs in terms of the number of cells, occupied area, and delay.

As shown in Figure 12, the proposed scheme is superior to all the previously proposed designs in terms of the number of cells and occupied area, with 29.5% and 50% improvements, respectively, compared with the best previous designs in [11]. Considering the delay, the proposed design is superior to all previously proposed designs, except for that in [11]. Finally, in terms of the cost function, although the cost of the proposed design is higher than those of the schemes in [13] and [19], the proposed design is considerably better in terms of complexity, occupied area, and delay criteria. Notably, the design presented in [13] lacks the Enable input.

Moreover, the simulation results of the proposed 3-to-8 decoder are given for all *X*, *Y*, and *Z* input modes in Figure 13. As can be seen, the proposed decoder works satisfactorily, and the outputs are achieved with a delay of four clock phases. In addition, it has 140 cells in the area of 0.09 μm^2.

5 | CONCLUSION

Decoders are one of the most important hybrid integrated circuits that are critical to designing logic circuits. In this study, we presented an optimum 2-to-4 decoder using a new formulation that is based on the MV32 gate in three layers. The proposed decoder is implemented and simulated using QCADesigner 2.0.3. Our proposed structure has 62 cells, area of 0.03 μm^2, and delay of three clock phases. The simulation results show that the proposed scheme works correctly and represents 29.5% and 50% improvement in terms of the number of cells and occupied area in comparison with the best previous designs, respectively. Moreover, a 3-to-8 QCA decoder architecture was designed and implemented using the proposed 2-to-4 QCA decoder. It has 140 cells, area of 0.09 μm^2, and delay of four clock phases.

ORCID

Mohammad Mosleh https://orcid.org/0000-0002-0991-1623

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AUTHOR BIOGRAPHIES

Akram Abbasizadeh received the BS degree in Electronic Engineering from Islamic Azad University, Shushtar Branch, Shushtar, Iran, in 2008, She received the MS degree in Architecture of Computer Systems from Karoon Institute of Higher Education, Ahvaz, Iran, in 2019. Her main research activities include quan tum-dot cellular automata and nano electronic circuits

Mohammad Mosleh received the BS degree in Computer Hardware Engineering from Islamic Azad University, Dezful Branch, Dezful, Iran, in 2003, the MS degree in Architecture of Computer Systems from Islamic Azad University, Science and Research Branch, Tehran, Iran, in 2006, and PhD in Computer Engineering from the Islamic Azad University, Science and Research Branch, Tehran, Iran, in 2010. He is an assistant professor with the Department of Computer Engineering, Dezful Branch, Islamic Azad University, Dezful, Iran. His research interests include audio security (watermarking and steganography), and nano computing including quantum-dot cellular automata and reversible circuits.