ORIGINAL ARTICLE

ETRI Journal WILEY

Low energy and area efficient quaternary multiplier with carbon nanotube field effect transistors

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In this study, new multiplier and adder method designs with multiplexers are proposed. The designs are based on quaternary logic and a carbon nanotube field-effect transistor (CNTFET). The design utilizes 4 × 4 multiplier blocks. Applying specific rotational functions and unary operators to the quaternary logic reduced the power delay produced (PDP) circuit by 54% and 17.5% in the CNTFETs used in the adder block and by 98.4% and 43.62% in the transistors in the multiplier block, respectively. The proposed 4 × 4 multiplier also reduced the occupied area by 66.05% and increased the speed circuit by 55.59%. The proposed designs are simulated using HSPICE software and 32 nm technology in the Stanford Compact SPICE model for CNTFETs. The simulated results display a significant improvement in the fabrication, average power consumption, speed, and PDP compared to the current best-performing techniques in the literature. The proposed operators and circuits are evaluated under various operating conditions, and the results demonstrate the stability of the proposed circuits.

KEYWORDS
Carbon nano tube, minimum power consumption, multiplier, quaternary logic

1 | INTRODUCTION

Regarding advances in science and technology, the human need for information, processing speed, and storage has increased considerably over time. The fabrication of compact integrated circuits has reduced energy consumption and increased system speeds. With the advent of complementary metal-oxide-semiconductor (CMOS) technology, CMOS transistors encountered challenges such as short channel effects, leakage currents, increased power consumption, and high sensitivity to orbital parameters that encouraged scientists to take advantage of new technologies at the nanoscale [1,2]. The similarities between carbon nanotube field-effect transistors (CNTFETs) and metal-oxide-semiconductor field-effect transistors have been studied by researchers. CNTFETs have a high carrier mobility, low power consumption, lower latency, and small intrinsic capacitors that result in high-performance speeds. Due to the similar electron and hole mobilities, the P- and N-types of these transistors have similar channel lengths. One unique feature of CNTFETs is the variation in the threshold voltage by hanging the channel length [3]. Using these transistors and multi-value logic (MVL) greatly reduces the integrated circuit volume. MVL circuits do not exhibit common problems of binary circuits including a high number of connections and power consumption [4], which reduces the circuit complexity and chip surface. This allows rational and mathematical functions to be implemented at a faster rate and the number of computation

[5]. The multi-valued logic is divided into ternary, quaternary, and pentanary groups. Most of this research is performed in the ternary field. The quaternary logic between the highest and the lowest levels in the MVL circuits can be considered a suitable option when designing microprocessors. Different circuits have been designed using CNTFETs and MVL logic. Ternary and quaternary circuits work directly with ternary and quaternary logic [6,7]. The circuits work by Ternary and Quaternary converters to binary and vice versa [8,9] or work by multiplexers (MUXs) [10,11]. Because most computational operations are performed by adding an operator, in this study, different adder and multiplier blocks were designed using MUXs and circuits with quaternary logic. New insights into MUXs and circuits dramatically reduced the number of transistors, average power consumption, delay in propagation, and PDP compared with previous results [7,12–16]. The remainder of the paper is organized as follows. The second section describes the basic principal. The third section includes the proposed circuit design, and the fourth section presents the simulated results and comparison. The conclusions are presented in the final section.

2 | BASIC PRINCIPLE

This section is an overview of the general CNTFET and Quaternary logic transistor principles.

2.1 | CNTFET

Nanotubes are graphite plates with a tubular form and hexagonal structure. The nanotube plates can be conductive or semi-conductive depending on their rotational axis. Carbon nanotubes are composed of tubular graphite plates that are based on the chirality vector $C = ma_1 + na_2$ where a_1 and a_2 are the unit vectors of the graphite plate, and the chirality (m, n) determines how the CNTs twist. Single-walled carbon Nanotubes can be conductors or semiconductors. If m and n are equal $(m = n)$ or their product is a multiple of 3 $(m{\cdot}n = 3i)$, then the nanotube will exhibit metal conductivity. Otherwise, the produced nanotube will exhibit a semi-conductive property [17]. Figure 1 shows the structure CNTFET structure. The appropriate threshold voltage for CNTFETs can be obtained by using an appropriate CNT diameter. The CNTFET threshold voltage is inversely related to the nanotube diameter and is expressed as follows [12].

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3} \frac{a.V_\pi}{e.DCNT} \approx \frac{0.43}{DCNT(nm)}, \quad (1a)$$

$$DCNT = \frac{a.\sqrt{m^2 + n^2 + m.n}}{\pi} = 0.078\sqrt{m^2 + n^2 + m.n}, \quad (1b)$$
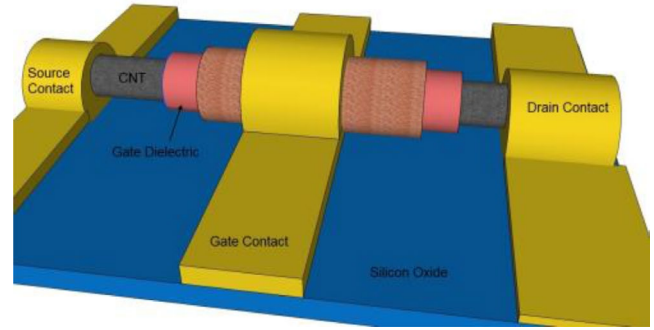
FIGURE 1 CNTFET structure [18]. Reprinted from Popproject3, CC BY-SA 3.0, https://creativecommons.org/licenses/by-sa/3.0.

where a is the distance between two adjacent carbon atoms $(a \cong 0.248)$, V_π is the bond energy between the two carbon atoms $(V_\pi = 0.033)$, e is the unit electron charge, and DCNT is the diameter of the carbon nanotube. Therefore, by using a CNTFET transistor with appropriate nanotube diameters, different threshold voltages, which are the basis for evaluating various logical levels, can be created. The relationships between chirality, CNT diameter, and threshold voltage are shown in Table 1.

2.2 | Quaternary logic

Quaternary logic consists of four voltage levels, as shown in Table 2. Logical functions were also introduced based on

TABLE 1 Relationships between chirality, CNT Diameter, and Threshold voltage

(n, m)	Diameter (CNTs)	Threshold voltage (N-CNTFET)	Threshold voltage (P-CNTFET)
(19, 0)	1.487 nm	0.289 V	–0.289 V
(17, 0)	1.330 nm	0.328 V	–0.328 V
(16, 0)	1.253 nm	0.348 V	–0.348 V
(14, 0)	1.100 nm	0.398 V	–0.398 V
(13, 0)	1.018 nm	0.428 V	–0.428 V
(11, 0)	0.861 nm	0.506 V	–0.506 V
(10, 0)	0.783 nm	0.559 V	–0.559 V

TABLE 2 Corresponding voltages and logic values

Scale	Logic	Voltage (V)
GND	0	0
$V_{dd}/3$	1	0.3
$2V_{dd}/3$	2	0.6
V_{dd}	3	0.9

TABLE 3 Quaternary inversion truth table

IN	NQI	PQI	IQI	SQI
0	3	3	3	3
1	0	3	3	2
2	0	3	0	1
3	0	0	0	0

TABLE 4 QNAND and QNOR truth table

A	QNAND				A	QNOR			
B	0	1	2	3	B	0	1	2	3
0	3	3	3	3	0	3	2	1	0
1	3	2	2	2	1	2	2	1	0
2	3	2	1	1	2	1	1	1	0
3	3	2	1	0	3	0	0	0	0

quaternary logic such as QNAND, QNOR, QNOT, and other special functions [12,14].

Multi-value functions include various functions based on the particular attitude type assigned to them, for example, the inverter has several functions such as the Intermediate Quaternary Inversion (IQI), Negative Quaternary Inversion (NQI), Positive Quaternary Inversion (PQI), and Standard Quaternary Inversion (SQI) [5,18].

$$QNOT(a) = 3 - a, \quad (2a)$$

$$QNAND(a,b) = \overline{MIN(a,b)} = \begin{cases} 3-a & \text{if } a \le b \\ 3-b & \text{otherwise} \end{cases}, \quad (2b)$$

$$QNOR(a,b) = \overline{MAX(a,b)} = \begin{cases} 3-a & \text{if } a \ge b \\ 3-b & \text{otherwise} \end{cases}. \quad (2c)$$

The accuracy of the inverter functions is shown in Table 3.

TABLE 5 Unary operator truth table

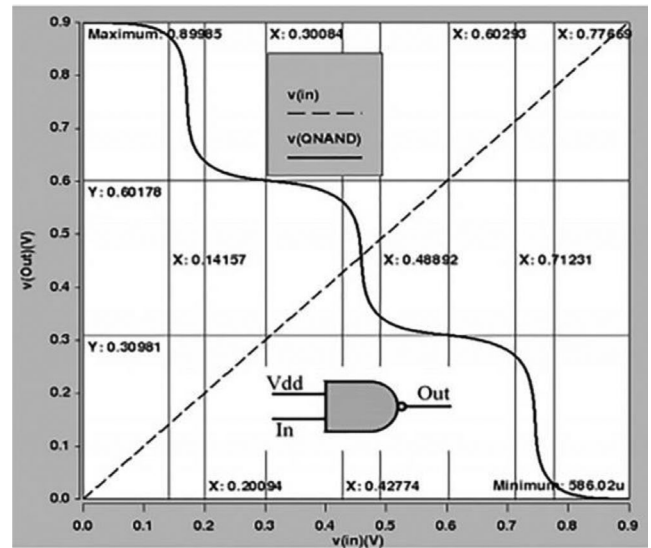| A	A_P	A_N	A_I	A^1	A^2	A^3	1. $\overline{A_P}$	1. $\overline{A_N}$	1. $\overline{A_I}$	S_1	S_2
0	3	3	3	1	2	3	0	0	0	0	0
1	3	0	3	2	3	0	0	1	0	3	0
2	3	0	0	3	0	1	0	1	1	0	3
3	0	0	0	0	1	2	1	1	1	0	0

FIGURE 2 QNAND voltage-to-time converter diagram [13]

Equation (2a) is equal to the SQI function, and the performance of (2b) and (2c) are shown in Table 4 and Figure 2.

3 | PROPOSED CIRCUITS

In this section, one 4 × 4 multiplier design is proposed. It is necessary to have a 1 × 1 multiplier block and various adder blocks in the MUX design approach.

3.1 | Proposed quaternary MUX and unary functions

Specific design functions such as circuits are defined in Table 5. A_P is equivalent to the PQI function, A_N is equivalent to the NQI function, and A_I is equivalent to the IQI function. The circuit operators are defined according to their design requirements in this work. Table 5 displays the operators used in this study. A^1, A^2, and A^3 are the rotational quaternary logic operators that, according to their indices, represent the beginning of the function with that level. For example, A^1 indicates that the operator starts

TABLE 6 Quaternary multiplier truth table [13]

A	Product				A	Carry			
B	0	1	2	3	B	0	1	2	3
0	0	0	0	0	0	0	0	0	0
1	0	1	2	3	1	0	0	0	0
2	0	2	0	2	2	0	0	1	1
3	0	3	2	1	3	0	0	1	2
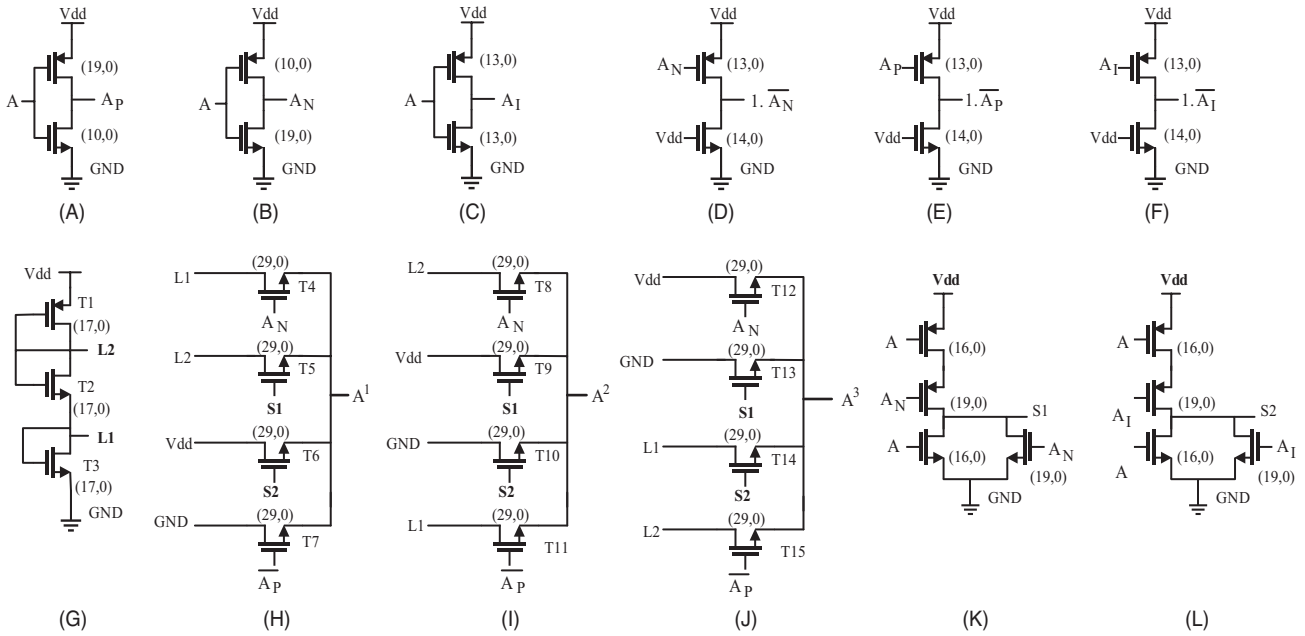
FIGURE 3 CNTFET unary operator circuits: (A) A_P, (B) A_N, (C) A_I, (D) $1.\overline{A_N}$, (E) $1.\overline{A_P}$, (F) $1.\overline{A_I}$, (G) voltage divider, (H) A^1, (I) A^2, (J) A^3, (K) S_1, and (L) S_2

at level 1, and the A^2 operator begins at level 2. These operators were constructed by varying the voltage levels of the chirality vector according to the status of A and its dependent operators. Figure 3 illustrates this claim. A 4×1 MUX was used to construct the A^1, A^2, and A^3 operators, and the voltage levels L_1 (0.3 V) and L_2 (0.6 V) were generated by the voltage divider. In Figure 3H, the S_1 and S_2 operators are used to control the MUX outputs. For example, in the A^1 operator, when A switches on its corresponding levels (0, 1, 2, and 3), the voltage levels (A) of transistors T_4, T_5, T_6, and T_7 are switched on, respectively. This is also the case for the A^2 and A^3 operators, which produce different output levels proportional to the input A [14]. Three types of 4×1, 8×4, and 12×4 MUX structures were also used in the

multiplier and adder block circuit designs, and their structures are shown in Figure 4.

3.2 | Proposed multiplier

The multiplier operator is one of the most important and commonly used operators in the arithmetic logic unit. The accuracy of the quaternary multiplier is presented in Table 4 [13].

According to Table 4, the product and carry values were obtained from (3), where A_0, A_1, A_2, and A_3 are equivalent to the A = 0, 1, 2, and 3 levels, respectively. This also applies to B and its various levels.
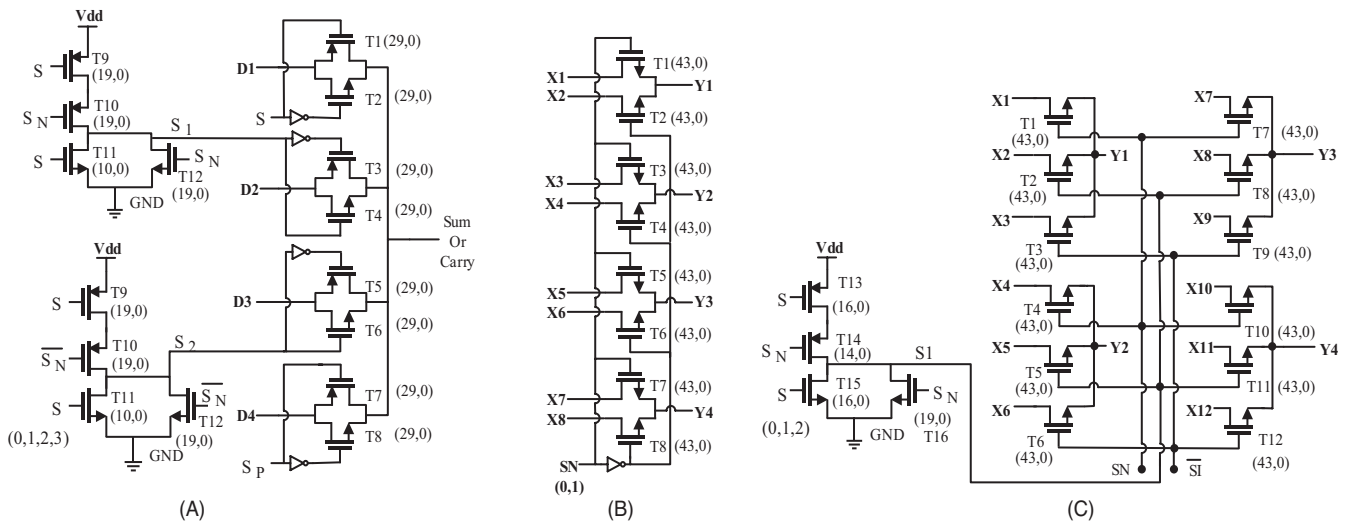
FIGURE 4 Quaternary multiplexers used in the proposed design: (A) 4×1 multiplexer, (B) 8×4 multiplexer, and (C) 12×4 multiplexer
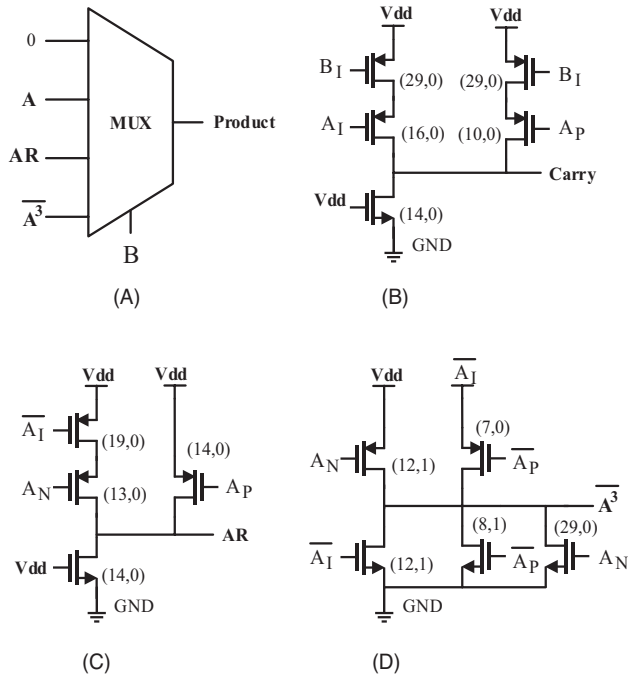
FIGURE 5 Quaternary multiplier structure: (A) multiplier product, (B) carry multiplier, (C) unary operator AR, and (D) unary operator $\overline{A_3}$

$$\text{product} = B_1 \left(A_0 + A_1 + A_2 + A_3\right) + B_2 \left(A_0 + A_2 + A_0 + A_2\right)$$
$$+ B_3 \left(A_0 + A_3 + A_2 + A_1\right), \tag{3}$$
$$\text{Carry} = B_2 \left((1.A_2) + (1.A_3)\right) + B_3 \left((1.A_2) + (2.A_3)\right).$$

TABLE 7 Quaternary half adder truth table

A	Sum					A	Carry				
B	**0**	**1**	**2**	**3**		**B**	**0**	**1**	**2**	**3**	
0	0	1	2	3	A	0	0	0	0	0	0
1	1	2	3	0	A^1	1	0	0	0	1	$1.\overline{A_P}$
2	2	3	0	1	A^2	2	0	0	1	1	$1.\overline{A_I}$
3	3	0	1	2	A^3	3	0	1	1	1	$1.\overline{A_N}$

TABLE 8 Truth table of proposed quaternary full adder with unary

C_{in}	B	A	Sum	C_{out}
0	0	A	A	0
0	1	A	A^1	$1.\overline{A_P}$
0	2	A	A^2	$1.\overline{A_I}$
0	3	A	A^3	$1.\overline{A_N}$
1	0	A	A^1	$1.\overline{A_P}$
1	1	A	A^2	$1.\overline{A_I}$
1	2	A	A^3	$1.\overline{A_N}$
1	3	A	A	1

The product and carry equations can be rewritten as relations (4).

$$\text{product} = B_1 (A) + B_2 (AR) + B_3 \left(\overline{A_3}\right),$$
$$\text{Carry} = B_2 (C1) + B_3 (C2). \tag{4}$$

According to (4), the MUX 4 × 1 structure can be used to design the multiplier unit. Figure 5A shows the proposed multiplier block structure inputs of the MUX 4 × 1 according to (4), and Table 6 is set for product section. Another MUX can also be used to construct the carry operators. A reduced number of proposed transistor circuits are shown in Figure 5B. Figure 5C and 5D display the unary function circuits used in the multiplication operation. In the above multiplier circuit, 53 CNTFET transistors were used to create the product and carry operators, and one power supply was used for the MUX units and control circuits. whereas the space applied decreased by 43.62% compared to [13] and by 61.59% compared to the first design [16]. The operators also decreased the power consumption by 98.46% compared to [13] and 98.26% compared to [16].

3.3 | Proposed half adder

The half adder structure significantly impacted the general design of the adder blocks. Table 6 illustrates the correctness of the A + B addition function [15,17]. In this study, previously proposed plans are further developed [8,14,18], and the sum levels and circuit diversities used were reduced to the number of transistors in the proposed design. According to Table 7, the value of the sum and carry are obtained by (5).

$$\text{Sum} = B_0 \left(A_0 + A_1 + A_2 + A_3\right) + B_1 \left(A_1 + A_2 + A_3 + A_0\right)$$
$$+ B_2 \left(A_2 + A_3 + A_0 + A_1\right) + B_3 \left(A_3 + A_2 + A_1 + A_0\right),$$
$$\text{Carry} = B_0 (0) + B_1 (1.A_3) + B_2 \left((1.A_2) + (1.A_3)\right)$$
$$+ B_3 \left((1.A_1) + (1.A_2) + (1.A_3)\right). \tag{5}$$

In these relations A_0, A_1, A_2, and A_3 are equal to levels $A = 0$, 1, 2, and 3, respectively. This also applies to B and its various levels. The sum and carry are rewritten as relationships in (6).

$$\text{Sum} = B_0 (A) + B_1 \left(A^1\right) + B_2 \left(A^2\right) + B_3 \left(A^3\right),$$
$$\text{Carry} = B_0 (0) + B_1 \left(1.\overline{A_P}\right) + B_2 \left(1.\overline{A_I}\right) + B_3 \left(1.\overline{A_N}\right). \tag{6}$$

With respect to (6), we were able to design the sum and carry using two MUX 4 × 1 multipliers, which can be seen in Figure 6. In this case, B acts as a selector in the MUX units, and by selecting one of the B levels as the sum operator, one of the A, A^1, A^2, and A^3 inputs is considered to
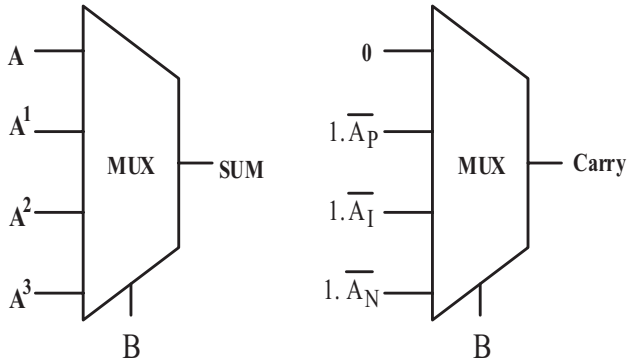
FIGURE 6 Proposed quaternary half adder design

FIGURE 7 Proposed QFA1 structure

be the output, and for the carry operator, B is selected as one of the operators (1. $\overline{A_P}$, 1. $\overline{A_I}$, 1. $\overline{A_N}$) or 0 is the output.

Figure 4A shows the MUX structure used in this research. In the half adder circuit, a total of 71 CNTFET transistors were used to create the sum and carry operators. MUX units and control circuits were used with one power supply, and applied space decreased by 33% compared to [7], 21% compared to the first design [12], and 19% compared to the second design [12].

3.4 | Proposed first full adder

Each Full adder block consists of three inputs (IN$_1$, IN$_2$, and C_{in}) and two outputs (Sum and C_{out}). According to Table 7, we can observe that the highest value of the carry operator is 0 or 1; therefore, the input carry (C_{in}) can be a maximum of 1. The collector accuracy can be found in Table 8.

According to Table 8, the value of the sum and carry operators are as follows:

$$
\begin{aligned}
\text{Sum} &= C_0 \left(B_0 (A) + B_1 \left(A^1 \right) + B_2 \left(A^2 \right) + B_3 \left(A^3 \right) \right) \\
&\quad + C_1 \left(B_0 \left(A^1 \right) + B_1 \left(A^2 \right) + B_2 \left(A^3 \right) + B_3 (A) \right), \\
\text{Carry} &= C_0 \left(B_0 (0) + B_1 \left(1.\overline{A_P} \right) + B_2 \left(1.\overline{A_I} \right) + B_3 \left(1.\overline{A_N} \right) \right) \\
&\quad + C_1 \left(B_0 \left(1.\overline{A_P} \right) + B_1 \left(1.\overline{A_I} \right) + B_2 \left(1.\overline{A_N} \right) + B_3 (1) \right).
\end{aligned}
$$
(7)

In these equations, A, B, and C are the inputs; A and B are equal to 0, 1, 2, or 3 and is C_{in} equal to 0 or 1.

Based on Table 8 and (7), the proposed full adder structure design is displayed in Figure 7. A MUX 8 × 4 that saves two MUXs compared with that of the full adder base is used in this structure [17]. In Figure 4B, the MUX 8 × 4 structures are shown, where if $C = 0$, transistors T_1, T_3, T_5, and T_7 switch on, and if $C = 1$, transistors T_2, T_4, T_6, and T_8 switch on and the input operator transfers to that of the output. In total, 93 CNTFET transistors were used in the full adder, and the space required decreased by 52% compared to that of [12], 32% compared to that of the first design of [14] and 41%
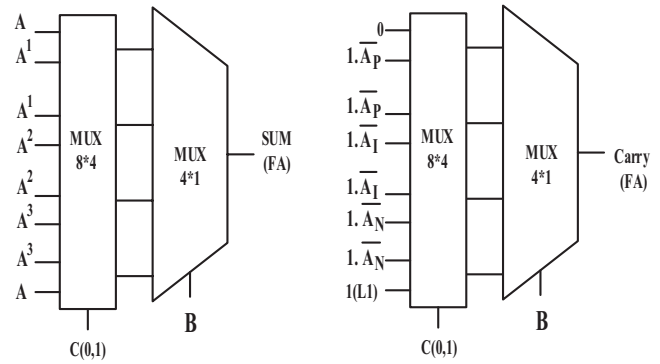
compared to that of the second design of [14], 43% compared to that of [13], and 40% compared to that of [7].

3.5 | Proposed second full adder

As mentioned in the previous section, typically the highest carry that can be moved to the next block in an additional action is 1. In the worst-case scenario, the count of a multiplier block can be 2. In this case, the maximum C_{in} of the full adder can be 2, and Table 9 represents the second full adder.

For the full adder design with the specifications in Table 9, one MUX 12 × 4 and one MUX 4 × 1 were used to create the output sum and carry operators in Figure 8. In this case, four fewer MUXs were utilized compared to that of the full adder base [17]. Table 10 and Figure 9 display the accuracy table and structure of the CE operator, respectively. The MUX used in the proposed design is shown in Figure 4C. In this circuit, if $C = 0$, T_1, T_4, T_7, and T_{10} switch on and communicate the connection between the incoming and outgoing

TABLE 9 QFA2 truth table

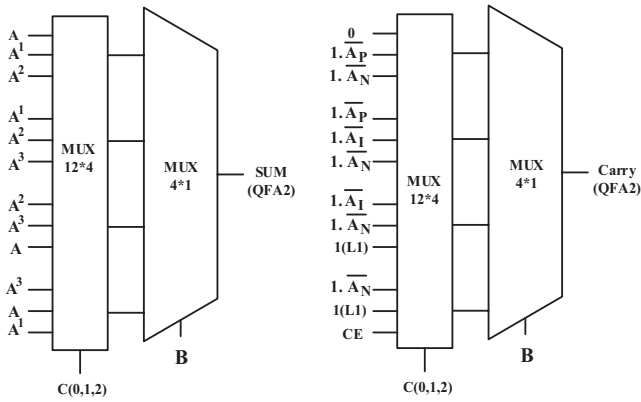| C_{in}	B	A	Sum	C_{out}
0	0	A	A	0
0	1	A	A^1	$1.\overline{A_P}$
0	2	A	A^2	$1.\overline{A_I}$
0	3	A	A^3	$1.\overline{A_N}$
1	0	A	A^1	$1.\overline{A_P}$
1	1	A	A^2	$1.\overline{A_I}$
1	2	A	A^3	$1.\overline{A_N}$
1	3	A	A	1
2	0	A	A^2	$1.\overline{A_I}$
2	1	A	A^3	$1.\overline{A_N}$
2	2	A	A	1
2	3	A	A^1	CE

FIGURE 8 Proposed QFA2 structure/

signals. Additionally, if $C = 1$, T_2, T_5, T_8, and T_{11} switch on, and if $C = 2$, T_3, T_6, T_9, and T_{12} switch on and transmit the input signal to the next floor. A total of 114 CNTFETs were used to construct the proposed QFA2, and the space applied decreased by 42% compared to that of [12], 18% compared to that of the first design of [14], 28% compared to that of the second design of [14], 31% compared to that of [7], and 27% compared to that of [12].

3.6 | Proposed 4 × 4 quaternary multiplier

The proposed multiplier is based on the classical Wallace and array Multiplier [19]. The structure of a four-trit

TABLE 10 CE operator truth table

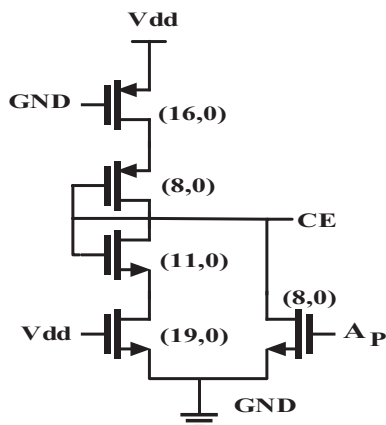| C_{in}	B	A	Sum	C_{out}
2	3	0	1	1
2	3	1	2	1
2	3	2	3	1
2	3	3	0	2

FIGURE 9 Unary operator CE structure

multiplier is depicted in Figure 10. In this structure, the M blocks only contain multiplier units; MA blocks in addition to a multiplication unit, contain one semiconductor
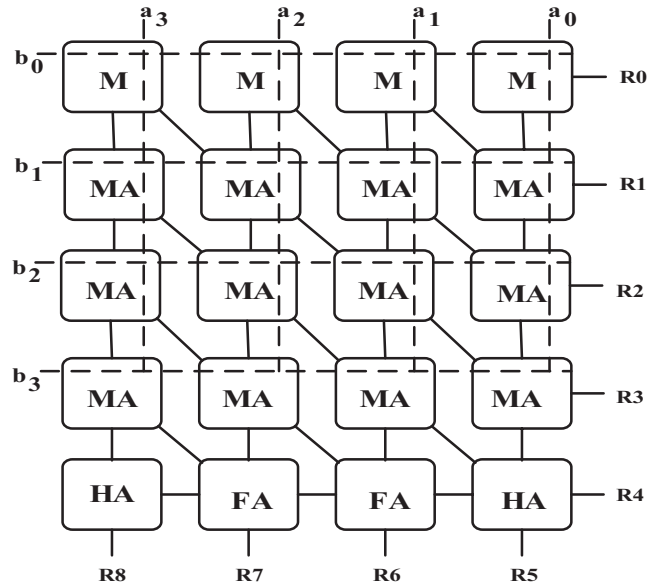

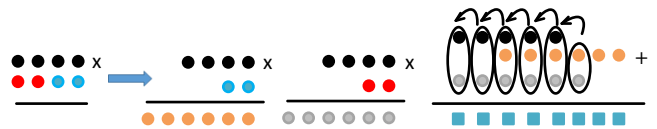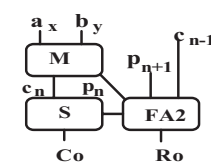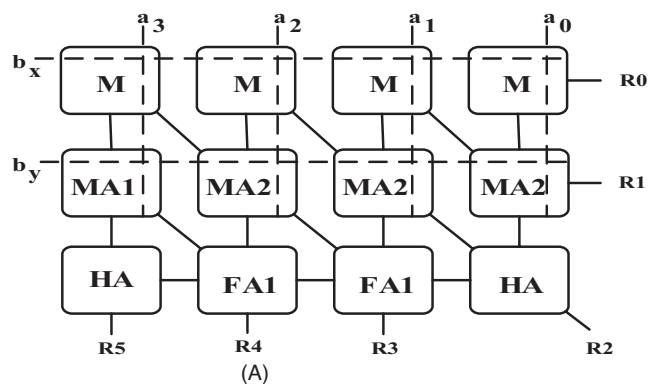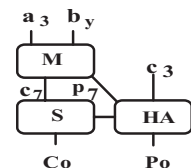**FIGURE 10** Structure of 4 × 4 quaternary array multiplier

FIGURE 11 Conversion of 4 × 4 multiplier to 2 × 4 multiplier

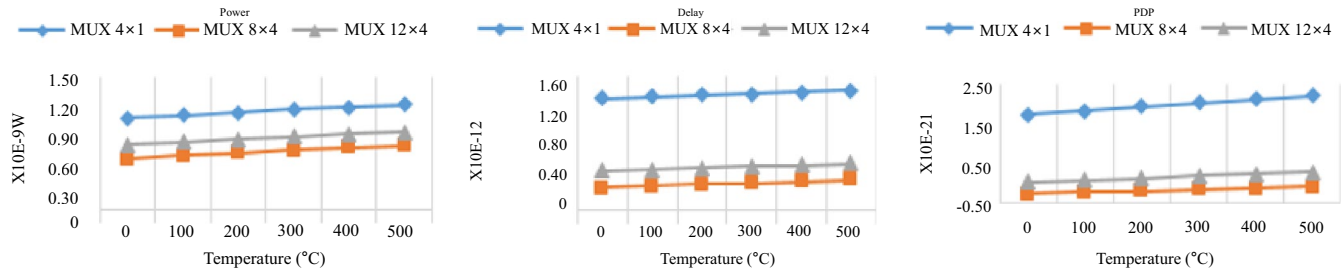**FIGURE 12** Structure of 2 × 4 multiplier

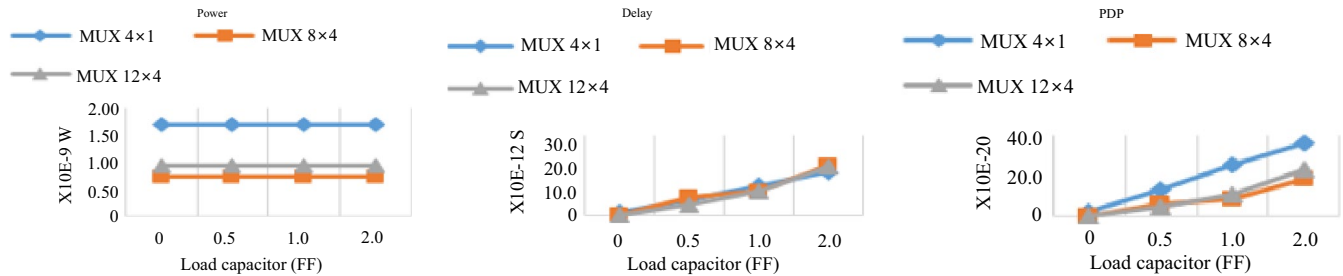**FIGURE 13** Evaluation of the proposed MUX for different temperatures

FIGURE 14 Evaluation of the proposed MUX for different load capacitor's

and one integrator that in total require 16 multipliers, 14 half adders, and 14 full adders to perform a 4 × 4 multiplication operation. For complete multiplication, the block delays must be considered.

In this study, a new multiplication approach is introduced, and two 2 × 4 multiplication blocks are used to accelerate multiplication operations, As illustrated in Figure 11.

Figure 12A shows the proposed multiplication structure. In this structure, block M only contains multipliers, and block MA2 contains one multiplier, one full adder, and one sum unit because the sum of Pn and Cn is a maximum of 3 only from the half adder block. The sum is utilized in Figure 12B. Additionally, block MA1 contains a multiplier, half adder, and a sum unit (Figure 12C). Each 2 × 4 multiplier contains eight multipliers, three FA2s, two FA1s, two HAs, and four sum units. Two 2 × 4 multiplier blocks require three HAs and threes FA1s as illustrated in Figure 11. The proposed multiplication blocks utilize a total of 2548 CNTFETs transistors including 93 for FA1, 113 for FA2, 71 for HA, 39 for the sum, and 53 for the multipliers. The proposed plan occupies 66.05% less space than that of [20]. In the proposed scheme, for a 4 × 4 multiplication operation, we should consider the delay of the eight multiplication blocks, six full adders, five half adders, and one sum increasing the multiplication rate to 55.59% compared to that of the usual method as shown in Figure 10.

4 | SIMULATION AND RESULTS

A simulation was performed using HSPICE software, 32 nm technology, and a standard model at Stanford University [21,22]. When designing the circuits exhibited in Figures 5–7, and Figure 9, between four and eight nanotubes were considered to design the MUX circuits to exhibit the optimal flow drive and a sufficient fanning out with eight tubes and a control circuit with four tubes. The accuracy and performance of the circuits designed at different temperatures and under different loads are shown in Figures 13 and 14. The circuits were simulated with a 0.9 V power supply, and Figure 15 displays the transient mode output multiplier. The evaluation criteria performances, including those of delay propagation, average power consumption, PDP, number of transistors used, and number of power supplies used are shown in Tables 11, 12, and 13. In the evaluation, the worst-case propagation delay includes the longest signal path and maximum delay time.

Table 11 shows the simulation results of the multiplier blocks with no load mode compared to those with a capacitive load of 2fF. The proposed PDP shows a 98.5% reduction compared to that of [13] and a 99.53% reduction compared to that of [16] and a power consumption reduction of 98.46% compared to that of [13] and a reduction of 98.26% compared to that of [16]. The velocity of the orbits increases by 5.5% compared to that of [13] and 73.27% compared to that of [16]. Additionally, the number of transistors used in the proposed
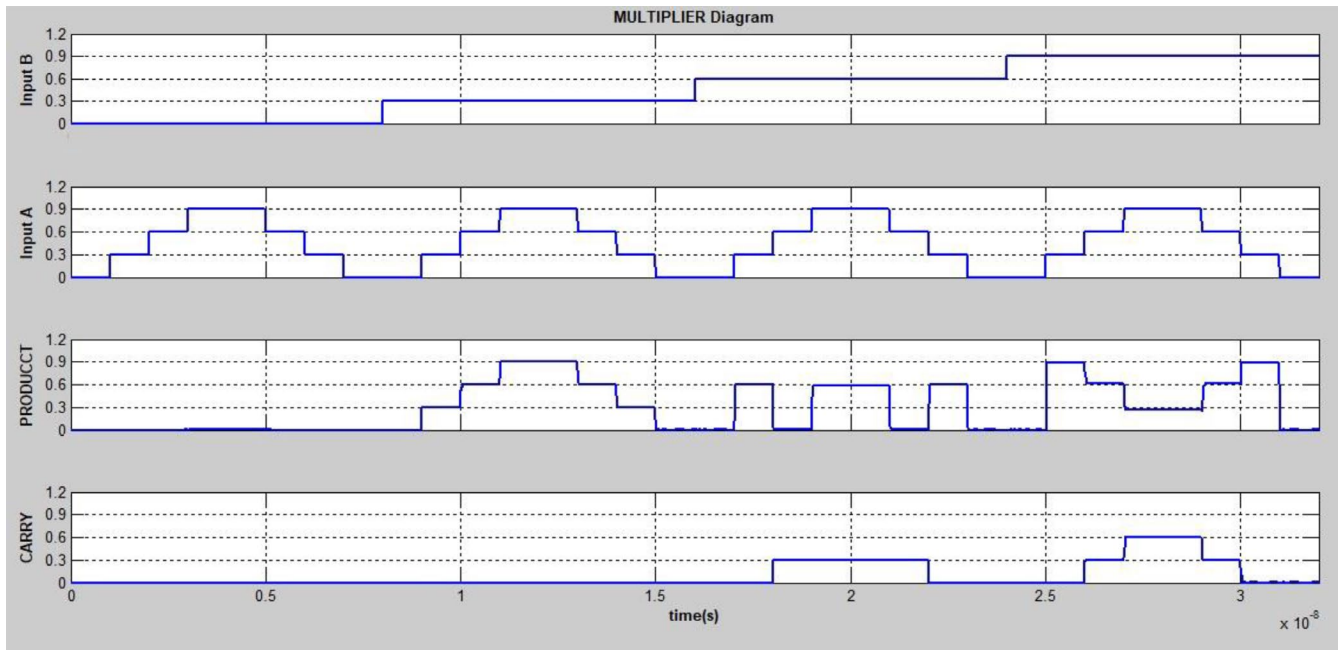
FIGURE 15   Transient response of the proposed quaternary multiplier

TABLE 11   Performance comparison of the quaternary multiplier

	Power (uw)	Delay (ps)	PDP (e-16J)	Transistor count	Power supply count
C-Load = 0e-15fF					
Proposed multiplier	0.0828	20.717	0.01715	53	1
[13]	5.379	21.928	1.1795	94	3
[16]	4.768	77.51	3.657	138	3
C-Load = 2e-15fF					
Proposed multiplier	0.112	49.5	0.0554	53	1

TABLE 12   Performance comparison of the quaternary half adders

	Power (uw)	Delay (ps)	PDP (e-16J)	Transistor count	Power supply count
C-Load = 0e-15fF					
Proposed (HA)	0.5858	31.8	0.1862	71	1
Design 1 [14]	0.116	10.92	0.012	50	3
Design 2 [14]	0.499	38.08	0.190	70	1
Design 1 [12]	1.755	49.89	0.876	89	1
Design 1 [12]	1.456	18.97	0.276	87	1
[13]	5.882	20.57	1.210	106	3
C-Load = 2e-15fF					
Proposed (HA)	0.7514	68.2	0.5123	71	1
Design 1 [14]	0.333	277.6	0.924	50	3
Design 2 [14]	0.729	99.54	0.752	70	1
Design 1 [12]	1.908	251.3	4.795	89	1
Design 1 [12]	1.619	74.94	1.213	87	1
[13]	5.961	42.45	2.531	106	3

design compared to design of [13] decreased by 43.62% and compared to that of [16] decreased by 61.59%.

Table 12 shows the simulation results. The proposed half adder with and without a 2fF capacitor decreased the PDP compared to the first design of [14] by 44.5%, second design of [14] by 32%, first design of [12] by 89.3%, second design of [12] by 58%, and design of [13] by 80% and decreased the number of transistors compared to the design of [14] by 33% and designs of [12] by 18% to 20%.

Table 13 shows the comparison results of all the proposed full adders with and without the presence of a 2fF capacitor load. There was a significant decrease in the number of transistors used, PDP, average power consumption, and propagation delay. As demonstrated by the first proposed full adder, the number of transistors used compared to the first design of [14] decreased by 32%, second design of [14] decreased by 41%, design of [12] decreased by 52%, design of [7] decreased

by 43%, first design of [15] decreased by 88%, and second design of [15] decreased by 40%, taking up less space on the chip. The PDP of the proposed design as compared to the first design of [14] decreased by 50%, second design of [14] decreased by 88%, design of [12] decreased by 68%, and design of [7] decreased by 100%. For the second proposed full adder, the PDP decreased compared to the first design of [14]

TABLE 13 Quaternary full adder performance comparison

	Power (uw)	Delay (ps)	PDP (e-16J)	Transistor count	Power supply count
C-Load = 0e-15fF					
Proposed 1 (FA)	0.7064	48.33	0.3414	93	1
Proposed 2 (FA)	0.7115	53.6	0.3713	113	1
Design 1 [14]	0.212	46.71	0.099	137	3
Design 2 [14]	0.884	43.88	0.387	157	1
[12]	2.467	71.72	1.178	195	1
[6]	75.34	112.7	84.95	163	1
Design 1 [15]	137.5	114.7	157.5	788	3
Design 2 [15]	57.73	71.54	41.25	154	1
C-Load = 2e-15fF					
Proposed 1 (FA)	0.9745	95.5	0.9306	93	1
Proposed 2 (FA)	1.216	109.67	1.33	113	1
Design 1 [14]	0.453	407.2	1.844	137	3
Design 2 [14]	1.161	665.0	7.721	157	1
[12]	2.657	107.9	2.871	195	1
[7]	102.4	122.3	125.3	163	1

by 28%, second design of [14] by 83%, design of [12] by 54%, and design of [7] by 99%.

5 | CONCLUSION

Applying the MVL logic to the CNTFET transistors speeds up the computational circuits and decreases the chip size. In this study, the multiplier, half adder, and full adder quaternary logic are designed using MUXs and pass transistor logic. Additionally, a 4 × 4 multiplier block was proposed, and previous designs were compared to the proposed ones. The proposed multiplier exhibits a minimum of 98.26% less energy consumption, a minimum PDP of 98.5%, and the number of transistors ranges from 43.62% to 61.59%. It also increases the circuit speed by 5.5% to 73.27%. In this research, the proposed 4 × 4 multiplier increased the circuit speed by 55.59% and reduced the space by 66.05%. That can benefit nanotechnology development. The design of multi-trit multipliers is recommended when considering the need to use different adders and multipliers in future circuits.

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