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생체 이식형 장치를 위해 구현된 403.5MHz CMOS 링 발진기의 성능 분석*

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Performance Analysis of 403.5MHz CMOS Ring Oscillator Implemented for Biomedical Implantable Device

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〈Abstract〉

With the increasing advancement of VLSI technology, health care system is also developing to serve the humanity with better care. Therefore, biomedical implantable devices are one of the amazing important invention of scientist to collect data from the body cell for the diagnosis of diseases without any pain. This Biomedical implantable transceiver circuit has several important issues. Oscillator is one of them. For the design flexibility and complete transistor-based architecture ring oscillator is favorite to the oscillator circuit designer. This paper represents the design and analysis of the a 9-stage CMOS ring oscillator using cadence virtuoso tool in 180㎚ technology. It is also designed to generate the carrier signal of 403.5MHz frequency. Ring oscillator comprises of odd number of stages with a feedback circuit forming a closed loop. This circuit was designed with 9-stages of delay inverter and simulated for various parameters such as delay, phase noise or jitter and power consumption. The average power consumption for this oscillator is 9.32㎼ and average phase noise is only －86 dBc/Hz with the source voltage of 0.8827V.

Key Words : MICS Band, Phase Noise, Ring Oscillator, Jitter, Biomedical Implantable Device

Ⅰ. Introduction

Biomedical implant devices are in embedding of many devices. From simple body temperature to complex invasive neural data are collected by the technology of implant devices. So, for the demand of present era this technology is upgrading day by day, for the low power consumption and size of the chip area. In these implant devices, data transceiver is one of the most important blocks, where oscillator is the essential part of the circuit. Figure 1 shows the block diagram of a transceiver system of implant device. MICS band of 402-405㎒ standardized by the IEEE work group which is used for implant devices, usually implemented just under the skin [1]. For low

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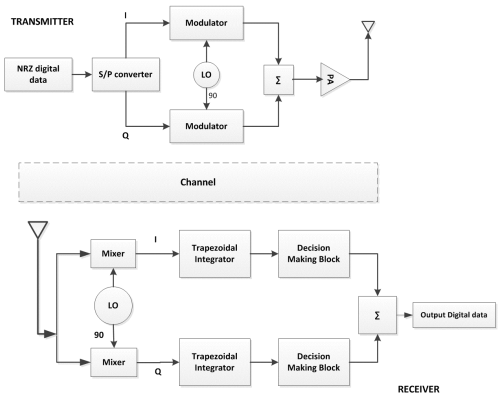
radiation and low transmission power, this band is used for transmitting data from inside to outside the body [2]. That is why in this work, the oscillator circuit needs to produce the carrier signal within the narrow-band.



<Figure 1> Data transceiver system for Implantable device

It is a well-recognized statistic that the application of oscillators is numerous, and it makes an obvious vital block in many mixed signal and RF circuits. As the frequency of an oscillator varies from few Hz to several MHz or GHz range according to its targeted field of application will also vary. The importance of ring oscillators in the industry is unquestionable. With the immense and fast development in the field of VLSI, their importance has too increased. With the advent of ADCs, PLLs and VCOs which have tremendous usages of ring oscillators. However, oscillators with high frequency are used in applications such as low power phase locked loops (PLL), voltage control oscillator (VCO) and oscillators with low frequency are used in specially designed radio communication like implanted biomedical transceivers [3]. The integrated passive LC oscillator shows good frequency stability and high spectral purity due to the frequency-selective feedback network. However, the large size of passives for use in low frequency LC oscillator is not economical. Although the crystal oscillators can provide clock signals with excellent stability with respect to supply voltage, temperature and process variations, its incompatibility with IC technology makes it unsuitable for a low-cost system. The inverter-based ring oscillator is simple, easy to be integrated and consumes lower power when compared with other types of oscillators such as RC oscillator, crystal oscillator and relaxation oscillator.

Numerous implementation of ring oscillators has been done in past decades. In [4], it is designed ring oscillator using 45nm technology with the phase noise of 179.1 dBc/Hz with the maximum voltage of 1.1V generating frequency range 6.62GHz. In [5], very low frequency of 1Hz range ring oscillator was designed using 90nm technology. With the power consumption of 14.44mW, a ring oscillator in 90nm technology for the voltage control oscillator is designed[6]. In [7], a simple but improved ring oscillator in 350nm technology which performed 300% better with positive feedback is designed.

Basically, a conventional Ring oscillator produces oscillations of several MHz frequency range and the frequency of the oscillations can be varied by adding the number of stages to it.

II. Ring Oscillator

Oscillatory behavior is omnipresent in all physical systems, particularly in electronic and optical system. Oscillators are used for frequency

translation of information signals and channel selection in radio frequency and light wave communication systems. A perfect time reference, i.e., a periodic signal, would have been provided by an ideal oscillator. However, all physical oscillators are besmirched by undesired perturbation/noise. Hence, signals generated by practical oscillators are not perfectly periodic, since the oscillator is a noisy physical system, and it makes them unique in their response to perturbation/noise. Though a variety of oscillators are implemented in different sectors of technology but the principle of operation, the frequency band of oscillation and the performance in noisy environment are different from one type of oscillators to the other. Nowadays, for transceiver designs of wireless communication system in biomedical implant devices demands oscillators with low power and low cost, such as ring oscillator. This ring oscillators have formed great attention because of their numerous useful and amazing features. These attractive features are:

- It is easy to design with the state-of-art integrated circuit technology, i.e. CMOS
- Oscillations can be achieved at low voltage
- High frequency of oscillations with dissipating low power can be achieved.
- It is easy to tune the oscillator electrically and wide tuning range can be provided.

However, due to the flexibility and easier implementation to the integrated circuit technology in comparison with others, such as RC or LC oscillators and relaxation oscillators, ring oscillator is always chosen for biomedical implant devices wireless transceivers blocks. Specially, the main tendency is to design with full transistor oscillators to avail the easy integration with the absenteeism of passive elements, which reduces the die area and average power consumption. So, these properties have made the ring oscillator prevalent for many communication systems. Generally, the performance of ring oscillator has always been better than relaxation oscillator but not like, as much as good as sinusoidal oscillators. But the continuous efforts of the researchers have yielded in the performance of ring oscillators to achieve a better level of approval which can now be used successfully in the communication systems, and it has been achieved in both factors, i.e. in speed or delay and noise performances.

Generally, oscillators needs to mollify Barkhausen criterion of stability, i.e. if A_1, A_2..., A_N are the gain of the amplifying elements of stage *1, 2,⋯,N* respectively, and $j\omega$ is the transfer functions of the feedback path, then the circuit will sustain the steady state oscillations only at frequencies for which the loop gain is unity and can be expressed as,

$$A_1(j\omega), A_2(j\omega), \dots, A_N(j\omega) = 1 \quad (1)$$

Usually, a ring oscillator is made of some delay stages. However, for Single-Input Single-Output (SISO) delay stages of inverter of odd numbers can make an oscillator wonderfully. So, some odd numbers of stages of this inverter can make an oscillator. Depending on Barkhausen criteria, every stage should add 180°/N phase to the signal (or reduce) and the other 180° provided by the sign of inverters, while N is a odd number of stages.

For calculating the frequencies of oscillation, all the stages of inverters are assumed to be the same.

So, based on Barkhausen criteria following equations can be expressed,

$$A_1(j\omega) = A_2(j\omega) \ldots\ldots = A_N(j\omega) = \frac{g_m R}{1+j\omega RC} \quad (2)$$

Also, about the phase oscillator we have

$$\angle A_1(j\omega) = \theta = tan^{-1}(\omega RC) = \frac{2K\pi}{RC} \quad (3)$$

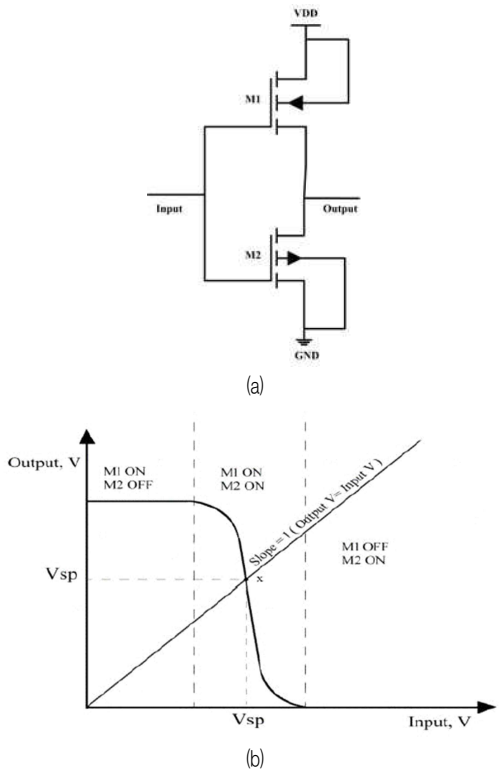
The frequency of oscillation can be calculated from the equation (4). But this frequency is actually the starting of the frequency of oscillation [8]. However, it is better to use large signal analysis, so that any stage of oscillator has specific delay time, where stage is an inverter with delay time t_d. As the stages are assumed to be similar to each other, so the frequency of oscillation can be calculated by the following equation,

$$f_0 = \frac{1}{2Nt_d} \quad (4)$$

It is observed from (4) that, with the number of stages N and, in a given number of times, the signal is passed through each stage twice. Actually, starting frequency is determined by the Barkhausen criteria and stable frequency of oscillation is determined by the delays of inverters [9]. As the oscillation frequency depends only on the delay time and the number of delay stages in a fixed structure, is constant, so the calculation and verifying the delay time is important.

2.1 CMOS Inverter

Generally, a single stage inverter involves a PMOS and a NMOS connected through the gate to obtain the single input as shown in figure 2.



<Figure 2> (a) Inverter configuration
(b) Transfer function [9]

The switching point of an inverter can be obtained by DC analysis and is as depicted in figure 2(b). From figure 2(b), it can be observed that when input voltage is equal to output voltage, it intersects at point x. This point x is called as inverter switching point and the corresponding voltage is called inverter switching voltage, V_{SP}. At point x both the MOSFETs M1 and M2 will be in saturation region. V_{SP} is given by (5) [9].

$$V_{SP} = \frac{\left(\sqrt{\frac{\beta_n}{\beta_p}}V_{THN}+V_{DD}-V_{THP}\right)}{\left(1+\sqrt{\frac{\beta_n}{\beta_p}}\right)} \quad (5)$$

β_n and β_p are the aspect ratios of NMOS and PMOS respectively, V_{THN} and V_{THP} are the threshold

voltage of NMOS and PMOS respectively.

One of the most important parameters of an inverter is V_{th} which characterizes its steady state characteristics [10]. It is also important to design W/L ratio of PMOS and NMOS devices for the gate to drive the current in both the directions. Thus, the following is derived:

$$\sqrt{\frac{1}{K_r}} = \frac{V_{th}-V_{ton}}{V_{dd}+V_{top}-V_{th}} \quad (6)$$

To achieve the required V_{th}, the equation of K_r is to be solved as follows:

$$K_r = \frac{K_n}{K_p} = \frac{(V_{dd}+V_{top}-V_{th})^2}{(V_{th}-V_{ton})^2} \quad (7)$$

For an ideal inverter, the relation can be given as below:

$$V_{th\_ideal} = \frac{1}{2V_{dd}} \quad (8)$$

So, to solve the equations, we use

$$\left(\frac{K_n}{K_p}\right)_{ideal} = \frac{(0.5V_{dd}+V_{top})^2}{(0.5V_{dd}-V_{on})^2} \quad (9)$$

The operation of PMOS and NMOS devices are complement in CMOS inverter. Hence,

$$\left(\frac{K_n}{K_p}\right)_{ideal} = 1 \quad (10)$$

Therefore, K_r is defined as

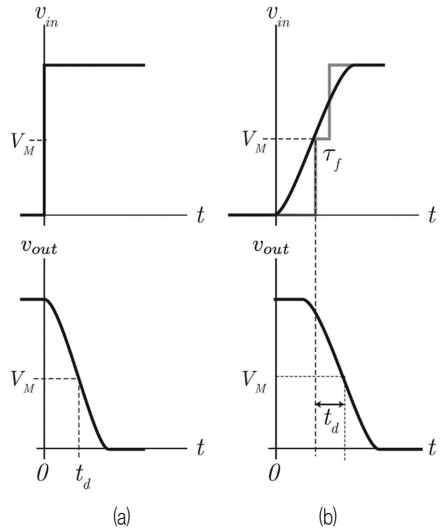
$$\frac{K_n}{K_p} = \frac{\mu_n C_{ox}\left(\frac{W}{L}\right)_n}{\mu_n C_{ox}\left(\frac{W}{L}\right)_p} \quad (11)$$

Assuming oxide thickness of gate equal for both NMOS and PMOS, and hence

$$\left(\frac{W}{L}\right)_p = 0.25\left(\frac{W}{L}\right)_n \quad (12)$$

2.2 Delay in Ring Oscillator

A CMOS inverter circuit has an important aspect, known as gate delay or propagation delay t_d. It can be defined as the time, when the input crosses the switching threshold or clasp point (V_M) of the inverter, to when its output crosses the clasp point of the next inverter in a manacle. The estimated delay time for the output voltage of an NMOS and CMOS inverter drives the capacitance of the next stage to cross the trip point in response to an input step in figure. 3.



<Figure 3> Delay graphs for toggling in the circuit

However, the input waveforms in a practical logic manacle are not ideal steps but have a finite slop, which in the case of a manacle of identical stages is the same at the input and output of each inverter

with opposite sign. This has directed to a distinguished calculation based on step response delay, which takes into account of the finite slope of the input ramp, as shown in figure 3(b) [11].

In [12], an astonishingly complicated, but complete analytical expression for delay is presented; given that the circuit in question contains only a NFET, a PFET, and a capacitor. The intricacy of these analyses forces designers to continue designing simple estimation based on RC delay for hand calculation, which are refined on timing simulations[13]. In [12], it is shown that delay can be estimated within 10% by approximating a ramp with a delayed two-level step input. The delay in the first step is the time it takes the ramp to reach the inverter toggle point, and the delay in the second step depends on the load capacitance and the ramp rate at the input.

Conventional CMOS Ring Oscillator is formed by cascading odd number of CMOS inverter stages forming a closed loop [9][14][15]. The 9-stage CMOS ring oscillator is shown in figure 4, M1-M18 constitutes the CMOS ring oscillator. As the frequency of oscillation is specified by the inverter delay time, accurate calculation of the delay in terms of model parameters is an important aspect in the design procedure.

Thus, for $t_0 < t < t_1$ *nmos* → *saturation*

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{th})^2 = -I_{CL} = -C_L\frac{dV_{out}}{dt} \quad (13)$$

For $V_{DD} - V_{th} < V_{out} < V_{DD}$

$$V_{DD} - V_{th} = \alpha V_{DD} \rightarrow 0 < \alpha < 1 \quad (14)$$

$$\int_{t_0}^{t_1} dt = -C_L\int_{V_{DD}}^{\alpha V_{DD}}\frac{1}{I_{Dn}}dV_{out} \quad (15)$$

$$\int_{t_0}^{t_1} dt = -\frac{2C_L}{\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{th})^2}\int_{V_{DD}}^{\alpha V_{DD}} dV_{out} \quad (16)$$

$$t_1 - t_0 = \frac{2C_L(1-\alpha)V_{DD}}{\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{th})^2} \quad (17)$$

For $t_1 < t < t_2$ *nmos* → *linear*

$$I_{Dn} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{th})V_{out} - \frac{1}{2}V_{out}^2 \quad (18)$$

$$\mu_n C_{ox}\frac{W}{L}(V_{in} - V_{th})V_{out} - \frac{1}{2}V_{out}^2 = -C_L\frac{dV_{out}}{dt} \quad (19)$$

For $V_{out} < V_{DD} - V_{th}$

$$\int_{t_1}^{t_2} dt = -C_L\int_{\alpha V_{DD}}^{\beta V_{DD}}\frac{1}{I_{Dn}}dV_{out} \quad (20)$$

$$\int_{t_1}^{t_2} dt = \frac{-2C_L}{\mu_n C_{ox}\frac{W}{L}}\int_{\alpha V_{DD}}^{\beta V_{DD}}\frac{1}{(V_{in}-V_{th})V_{out} - \frac{1}{2}V_{out}^2}dV_{out} \quad (21)$$

$$t_2 - t_1 = \frac{C_L}{\mu_n C_{ox}\frac{W}{L}(V_{DD} - V_{th})}\ln\left(\frac{2\alpha-\beta}{\beta}\right), \alpha > \beta \quad (22)$$

(17) and (22) yield the delay time t_{delay} as follows:

$$t_{delay} \approx t_2 - t_0 = (t_2 - t_1) + (t_1 - t_0) \quad (23)$$

$$t_{delay} \approx \frac{2C_L(1-\alpha)V_{DD}}{\mu_n C_{ox}\frac{W}{L}(V_{in}-V_{th})^2} + \frac{C_L}{\mu_n C_{ox}\frac{W}{L}(V_{DD}-V_{th})}\ln\left(\frac{2\alpha-\beta}{\beta}\right) \quad (24)$$

2.3 Jitter and Phase Noise in Ring Oscillator

A noise analysis in a ring oscillator differs from that of other oscillators, such as sinusoidal and relaxation oscillators. A harmonic oscillator, which is characterized by a correspondence between two energy storage elements and operates under

resonance, is used to provide a periodic output signal. The real resonant component might be an LC tank or a quartz crystal. Again, a relaxation (multi-vibrator) oscillator is also characterized by a correspondence with one energy storage element and relies on additional circuitry to sense the component state and control its excitation to provide a periodic output signal. In contrast, ring oscillators do not need to have any type of resonator and have a large tuning range. However, their frequency and phase characteristics are somewhat poorer than those of high Q-resonator based oscillators. Unlike a multi-vibrator, a ring oscillator is fully integrable in nature, although the fundamental difference between them is the number of energy storage components present in the oscillator circuit. The number of energy storage components is not unambiguous in a ring oscillator; in fact, there are many energy storage components available because the ring is unruffled of consists of multiple stages. However, a relaxation oscillator is integrated by nature, whereas a ring oscillator is not well-suited for the model of a relaxation oscillator.

In [16], it is described the consequence of thermal noise on the timing jitter in a CMOS differential delay cell-based ring oscillator. Their study produced factors in which the timing jitter is inversely proportional to the total capacitive load at the output of each delay stage and inversely proportional to the gate-source bias voltage above the threshold for a balanced state. Because the timing jitter and power consumption of a ring oscillator have an inverse relationship for a fixed output period, the total jitter variance for one cycle of oscillation is proportional to m and for m-stage ring oscillator, although the noise sources are uncorrelated. The rms of timing jitter of a ring-oscillator based PLL is greater than the intrinsic jitter in an inverter manacle.

It is reported in [17] the phase noise and timing jitter of a CMOS differential ring oscillator. Their results are as follows: The nonlinearity of the delay stage and the unwanted fluctuation of the tail current owing to supply and substrate noise increase the phase noise of the oscillator output. The jitter increases almost linearly with the increase in frequency of the supply and substrate voltage noise. An increase in the transistor gate width of a CMOS inverter and the number of inverters in the ring structure increase the jitter of the oscillator output. Again, the phase noise and jitter decrease with an increase in the power consumption of the oscillator for a fixed period of oscillation.

However, it is also indicated in [18] that timing jitter occurs owing to the circuit parameters and circuit level noise sources, i.e. thermal and shot noise in a ring oscillator composed of bipolar differential pair delay stages. Jitter caused by the collector resistance of the delay stage is proportional to the square-root of the thermal energy divided by the power dissipation in the collector resistance. Therefore, power dissipation in the collector load decreases the oscillator jitter. However, thermal noise of the base resistance of the delay stage increases the oscillator jitter. Again, the fluctuation of the tail current caused by the thermal and shot noise increases the oscillator jitter, but an increase in the tail current means the delay stage dissipates more power, leading to an improvement in the jitter performance. Jitter does not depend on the number of stages of the ring

oscillator. To comprehend this assumption, which was verified through a hardware experiment conducted by the present authors, one must consider the jitter accumulation process around the ring where there is only one delay stage, which, during the process of transition, affects jitter accumulation at a given instant and all other stages in the ring are inactive and do not contribute to jitter. And it proves, for the jitter accumulation, the main measurement is the number of stage transitions, not the number of oscillator periods.

Researchers reported in [19] on the phase noise and timing jitter of single-ended CMOS ring oscillators and differential ring oscillators, and showed that the phase noise is inversely proportional to the power consumption of a single ended ring oscillator (SERO) and differential-pair ring oscillator (DRO) and increases quadratically with the oscillation frequency. In addition, the timing jitter is inversely proportional to the square-root of the power dissipation by the SERO and DRO. The phase noise and timing jitter depend on the number of stages of the DRO, but have no such dependency on the number of stages of the SERO. The DRO has lower sensitivity to the substrate and supply noise in comparison with the SERO. The DRO injects relatively low noise into the other circuit components on the same chip in comparison with the SERO.

In [20], scientist analyzed the phase noise in a CMOS differential ring oscillator. Based on their analysis, it can be stated that the phase noise is proportional to for a linear operation and when the output voltage swing is clipped by the power supplies of the oscillator. In addition, is the peak-to-peak voltage swing of the oscillator output. The thermal and flicker noises of the biasing circuit of the differential delay stages increase the phase noise at the oscillator output.

However, it is reported in [21] that the timing jitter and phase noise in a CMOS ring oscillator occur owing to white and flicker noises. White noise in the differential pairs dominates the jitter and phase noise, whereas the phase noise occurring from flicker noise mainly increases from the tail current control circuit. The analysis indicates that jitter and phase noise are independent of the number of stages, owing to the presence of white noise. However, the phase noise is proportional to and for white noise and flicker noise, respectively. The behaviors of the phase noise and timing jitter, based on probability theory, stochastic theory, and numerical methods, were also discussed by [17].

Such reviews have confirmed that noise is a major problem in oscillators because introducing even a small amount of noise into an oscillator causes histrionic changes in the frequency spectrum. This occurrence is unusual to oscillators and is known as phase noise or timing jitter. A perfect oscillator would have confined tones at discrete frequencies; however, any corrupting noise spreads these perfect tones, and ensues at high power levels within neighboring frequencies. This effect is the major donor of undesired phenomena, such as inter-channel interference, leading to an increased bit-error-rate (BER) in RF communication systems. Another appearance of the same phenomenon is jitter, which is important in clocked and sampled-data systems, resulting in uncertainties in switching instants caused by noise, thereby leading to synchronization problems. Characterizing how

noise affects an oscillator is therefore crucial for practical applications. The problem remains challenging because oscillators constitute a special class among noisy physical systems, i.e. their autonomous nature makes them unique in their response to perturbations.

Jitter is a noteworthy and usually undesired factor in communication systems, and in clock recovery circuits, is called timing jitter. It may be caused from electromagnetic interference (EMI) and crosstalk with other signals. Jitter affects the performance of a device and can cause an undesired effect in audio signals and a loss in the data transmitted between devices [21]. Jitter can be divided into period jitter and cycle-to-cycle jitter.

2.3.1 Period Jitter

The difference between any one clock period and an ideal clock period is called period jitter. This tends to be important in synchronous circuits such as digital state machines where an error-free operation is limited by the shortest possible clock period, and the average clock period limits the performance of the circuitry.

2.3.2 Cycle to Cycle Jitter

The difference between the duration of two adjacent clock periods is called the cycle-to-cycle jitter. This can be important for clock generation circuits used in RAM interfaces and microprocessors. Phase noise is the representation of random fluctuations in the frequency domain, which is caused by jitter. The total phase noise of ring oscillator (RO) can be determined in (25):

$$\mathcal{L}\{\Delta f\} = \frac{8kTV_{DD}f_{osc}^2}{3\eta P_{avg}V_{char}\Delta f^2} \quad (25)$$

where $$V_{char} = \frac{\Delta V}{\gamma}$$

In here, Δf is the offset frequency from the carrier at which the phase noise is measured, γ is a coefficient of 2/3 for long channel devices during saturation, ΔV is the gate over-drive voltage, k is a Boltzmann constant, and T is absolute temperature.

2.4 Average Power Consumption

The present era is demanding low-power consuming devices to be fabricated for implant devices and sensor networks. The power consumption in any circuit is a factor of significant interest because the power consumed in a circuit depends on the supply voltage. A higher supply voltage can cause more power consumption. Indeed, the use of a capacitor at every stage of the oscillator increases the delay and power consumption, but it becomes important to reduce the phase noise and jitter. In this study, the input supply voltage was maintained at 0.8827 V. Power in an N stage RO is given in (26):

$$P_{avg} = \eta V_{DD} I_{avg} = \eta N V_{DD} q_{max} f_{osc} \quad (26)$$

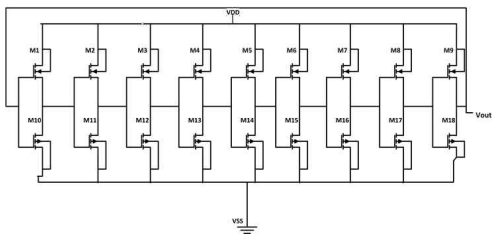
where $q_{max} = C_{tot}V_{DD} \quad I_{avg} = NC_{tot}V_{DD}f_{osc}$ (27)

A steady state is an equilibrium condition for a circuit, owing to the effects of a sudden change of state. A periodic steady-state response is an important factor because many design specifications in electronic circuits are given in terms of a steady

state, and it is therefore a prerequisite for dynamic small-signal modelling.

Ⅲ. Experimental Results

In this paper, a nine-stage ring oscillator is designed using 180㎚ technology. The width of both the NMOS and PMOS is maintained at 480㎛ and the length is 180㎚. After designing the transistor level, as shown in figure 4, the circuit is simulated using Cadence Virtuoso. The source voltage VDD is applied. A transient analysis is then conducted using 120㎱ for checking the frequency, phase noise, and average power. A DC analysis also applied to check the internal transistor parameters.



<Figure 4> 9-stage ring oscillator transistor level design

Figure 5 shows the oscillation of a circuit. It can also be observed that, owing to the internal properties of the inverter at the start point, there is a delay of approximately 22㎱. This delay is extremely less in comparison with other technologies because no initial biasing voltage is applied to start the oscillation.

It was observed that, according to VDD = 0.8827 V, a fixed oscillation frequency of 403.5 MHz is achieved, as shown in figure 6. Thus, by varying the VDD carefully, the desired bandwidth can also be achieved.

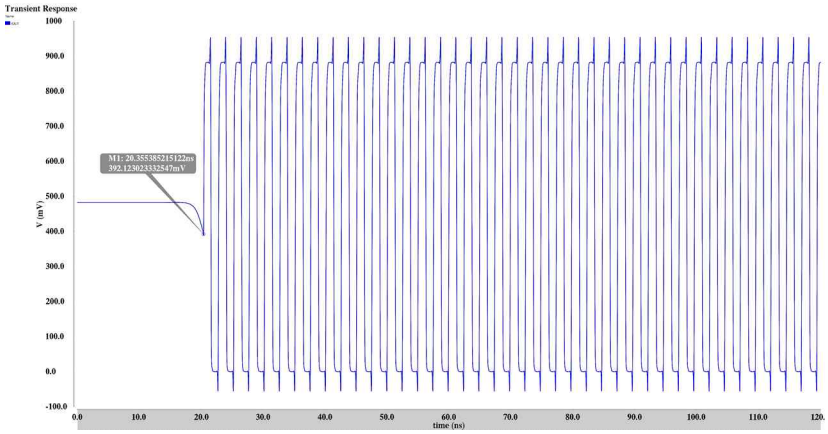
Figure 7 shows a waveform for the total power consumption in a circuit. The average power for the circuit is 8.88㎼. Again, the output characteristic noise curve, shown in figure 8, for the circuit is just like the input curve because of the odd number of stages and because the output is connected to the input as feedback.

Figure 9 shows the nature of phase noise in a circuit versus the frequency. The average noise level is −61 dBc/Hz. The percentage of Total harmonic distortion is shown in figure 10, and is continuous over the different harmonics of frequency, and is constant at approximately 37%. Another parameter, frequency jitter response is observed in transient respond. Frequency jitter is -277㎑ after 25㎱, and it is constant, observed in figure 11.

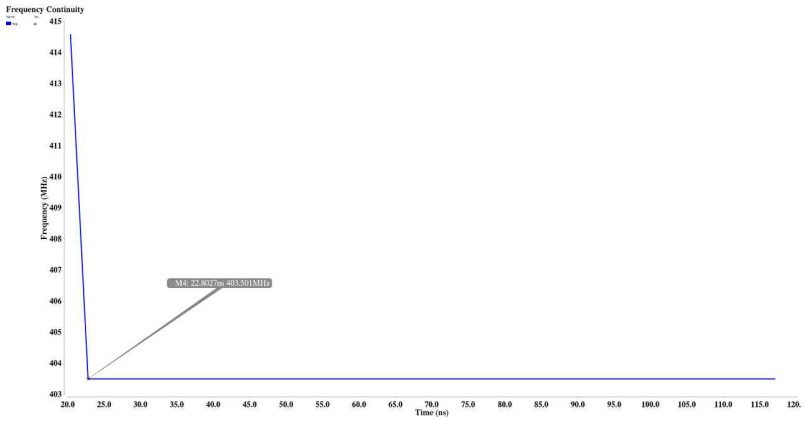
It can also be observed in figure 10 that a fixed stable frequency is achieved from approximately 22 ㎱, i.e. 403.5㎒. Table 1 shows a summary of the results and comparison with other works. Here, the average power is only 9.07㎼, and phase noise is only −61 dBc/Hz.

<표 Table 1> Comparison with previous studies

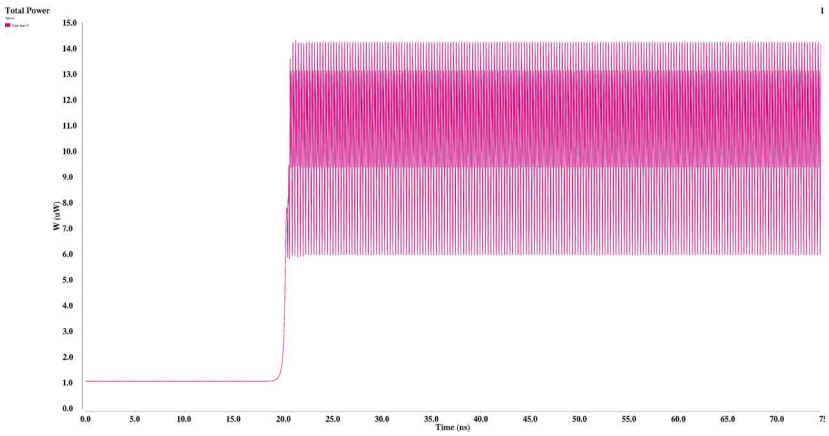
	This work	[7]	[5]	[4]	[6]
Technology	180㎚	-	90㎚	90㎚	350㎚
Supply Voltage(V)	0.8827	0.6~1	2.5~5	1.5	2~5
Generated Frequency	403.5 ㎒	3~6.62㎓	3.1~3.9 ㎒	1.2~3.2 ㎓	18.7~33.5 ㎒
Average Power	9.07 ㎼	1.23 ㎊	-	14.44 ㎽	-
Average Phase Noise	-61 dBc/㎐	179.1 dBc/㎐	-	90.1 dBc/㎐	-
Frequency Jitter	-277 %	-	-	-	-
Delay	22 ㎱	0.21 ㎰	-	-	55 ㎲



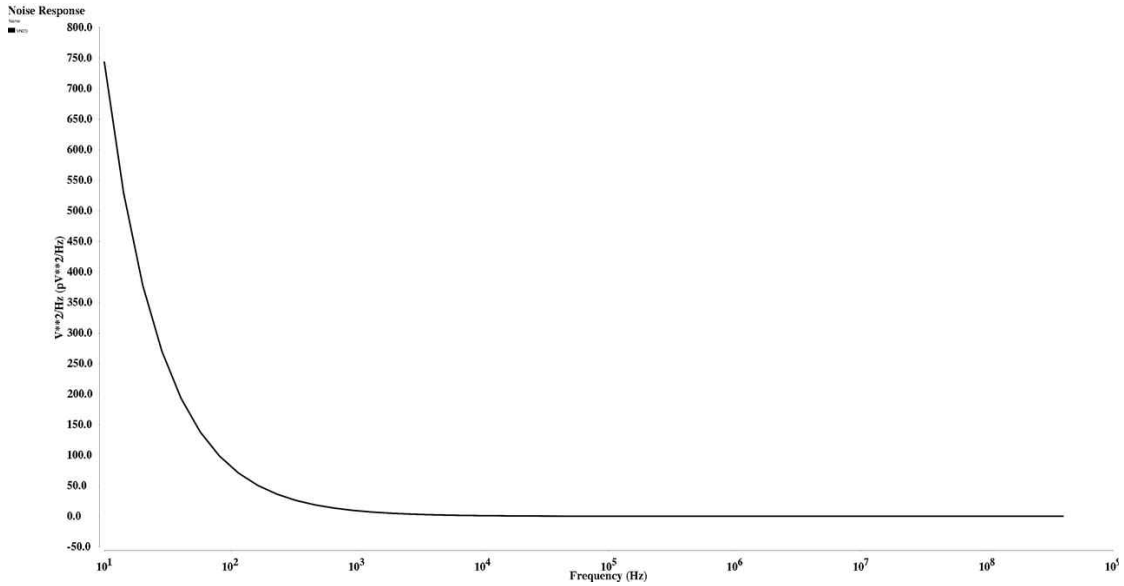
<Figure 5> Delay time before starting the oscillation



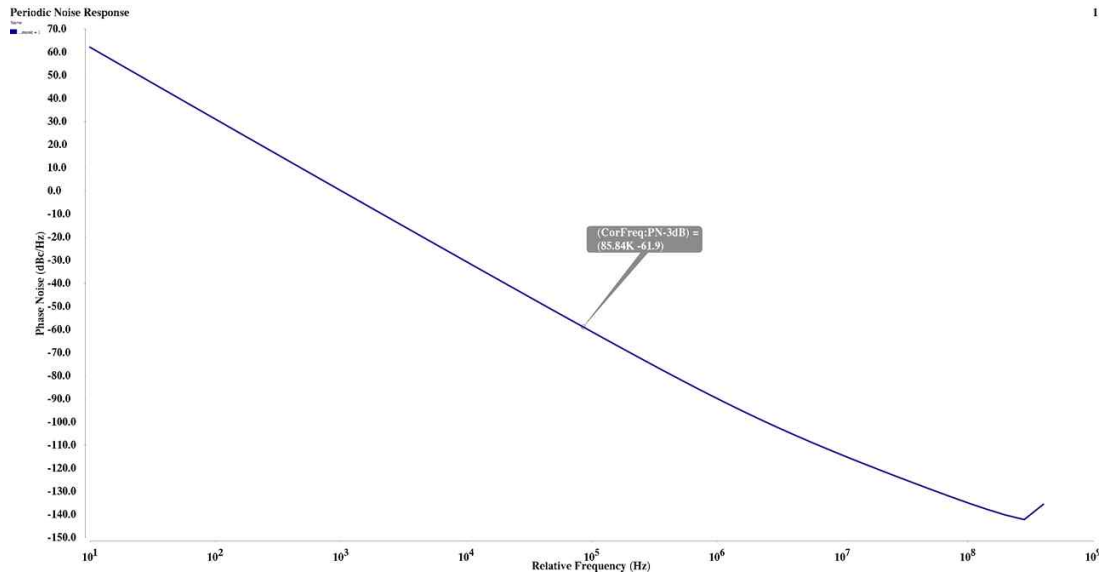
<Figure 6> Transient analysis: generating continuous frequency



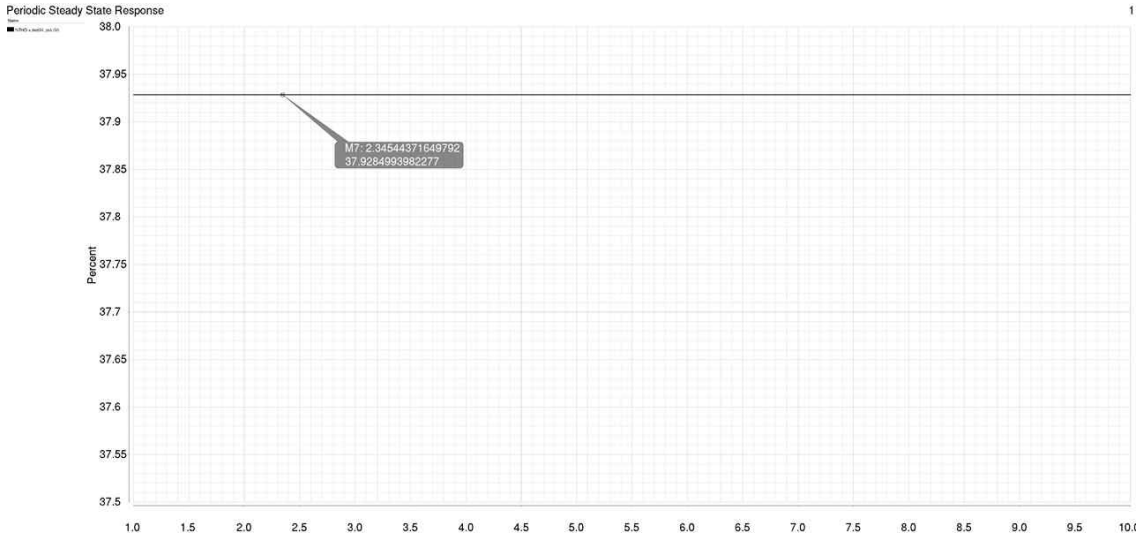
<Figure 7> Waveform for total power



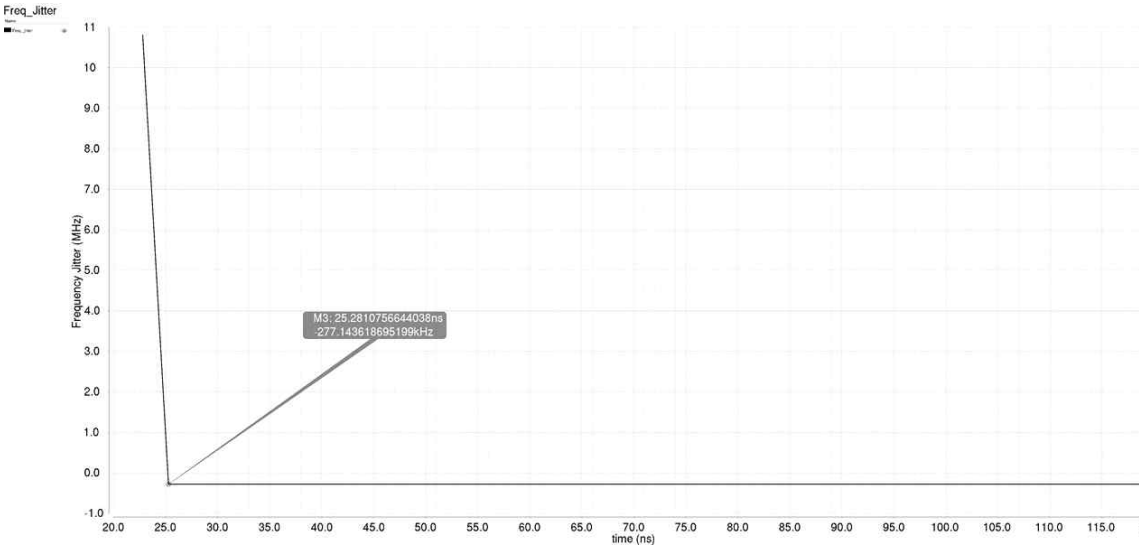
<Figure 8> Waveform for output noise



<Figure 9> Phase noise vs. frequency



<Figure 10> Total Harmonic Distortion (THD) for different harmonics of frequency



<Figure 11> Constant and Low Frequency Jitter after approximately 25㎲

Ⅳ. Conclusion

In this paper, a nine-stage ring oscillator was designed using 180-nm technology for biomedical implantable devices, which show better performance in comparison with a conventional power and space hungry RC or LC oscillator. The developed oscillator can be integrated with a VCO or PLL in the future. To reduce the phase noise and increase the accuracy, passive oscillator parameters can be

added to the circuit. However, this will increase the power consumption, and thus the main trade-off is power. Despite this, the accuracy of he frequency generation without extra biasing achieved using this simple method is highly significant.

References

[1] Spectrum Management and Telecommunications Radio Standards Specification, Medical Devices Operating in the 401-406㎒ Frequency Band, Spectrum Management and Telecommunications Industry Canada, RSS-243, Issue 3, February 2010.

[2] Federal Communications Commission (FCC), Amendment of parts 2 and 95 to the Communication's Rules to Establish a Medical Implant Communication Service at 401-402 and 405-406MHz, Federal Communications Commission, March 2009.

[3] Ajay Kumar Mahato, "Ultra Low Frequency CMOS Ring Oscillator Design," IEEE Proceedings of 2014 Recent Advances in Engineering and Computational Sciences, March 2014.

[4] Shruti Suman, Monika Bhardwaj, and B.P. Singh, "An Improved Performance Ring Oscillator Design," IEEE Proceedings of 2012 Second International Conference on Advanced Computing & Communication Technologies, Jan 2012.

[5] S. Balaji Ramakrishna, Shivananda Yalpi, L Nithin Kumar, H.B Ravindra, and Chaina Ram, "Design and performance analysis of low frequency CMOS ring oscillator using 90nm technology," Proceedings of 2016 IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology, May 2016.

[6] Akansha Shrivastava, Saurabh Khandelwal, and Shyam Akashe, "Performance evaluation of five stage VCO ring oscillator with reverse substrate bias and SAL technique using nanoscale CMOS technology," IEEE Proceedings of 2013 Third International Conference on Advanced Computing & Communication Technologies, June 2013.

[7] J.K. Panigrahi and D.P. Acharya, "Performance analysis and design of wide-band CMOS voltage-controlled ring oscillator," IEEE Proceedings of 2010 5th International Conference on Industrial and Information Systems, July 2010.

[8] R.J. Baker, CMOS Circuit Desig, Layout, and Simulation, IEEE Press Series on Microelectronic System 2nd edition, 2007

[9] J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits, Upper Saddle River, NJ: Pearson/Prentice-Hall, 2003

[10] Pankaj Gautam, Devesh Kaushik and Rahul Sharma, "Design of CMOS Inverter Using Different Aspect Ratios," EATHD-2015 Conference Proceeding, March 2015.

[11] N. Hedenstierna and K. Jeppson, "CMOS circuit speed and buffer optimization," IEEE Transaction Computer Aided Design: Integrated Circuits Systems, Vol. 6, No. 2, 1987, pp. 270–281

[12] L. Bisdounis, S. Nikolaidis and O. Loufopavlou,

"Propagation delay and short circuit power dissipation modelling of the CMOS inverter," IEEE Transaction of Circuits System International, Fundamental Vol. 45, No. 3, 1998, pp. 259–270.

[13] B Razavi, Design of Analog CMOS Integrated Circuits, Mc-Graw-HILL Edition, 2002.

[14] N. Weste and D. Harris, CMOS VLSI Design, Boston, MA: Pearson/Addison-Wesley, 2005.

[15] ZQ Lu, JG Ma and FC Lai, "A low-phase-noise 900-MHz CMOS ring oscillator with quadrature output," Analog Integrated circuits and Signal processing, Vol. 49, No. 1, 2006, pp. 27-30.

[16] F. Herzel and B. Razavi, "A study of oscillator jitter due to supply and substrate noise," IEEE Transactions on Circuits and SystemsII: Analog and Digital Signal Processing, Vol. 46, No. 1, 1999, pp. 56-62.

[17] J.A. McNeill, "Jitter in ring oscillators," IEEE Journal of Solid-State Circuits, Vol. 32, No. 6, 1997, pp. 870-879.

[18] A. Hajimiri, and T.H. Lee, The Design of Low Noise Oscillators, Kluwer Academic Press, Boston, 1999.

[19] L. Dai and R. Harjani, "Design of Low Phase Noise CMOS Ring Oscillators," IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. Vol. 49, No. 5, 2002, pp. 328-338.

[20] A.A. Abidi, "Phase Noise and Jitter in CMOS Ring Oscillator," IEEE Journal of Solid-State Circuits, Vol. 41, No. 8, 2006, pp. 1803-1816.

[21] Xiang Gao, Eric A. M. Klumperink, Paul F. J. Geraedts and Bram Nauta, "Jitter Analysis and a Benchmarking Fig.-of-Merit for Phase-Locked Loops," IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 56, No. 2, 2009, pp. 117-121.

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