On-Chip Spiral Inductors for RF Applications: An Overview

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Abstract—**Passive components are indispensable in the design and development of microchips for high-frequency applications. Inductors in particular are used frequently in radio frequency (RF) IC's such as low-noise amplifiers and oscillators. This paper gives a broad overview on the on-chip spiral inductors. The design concept and modeling approach of the typical square-shaped spiral inductor are first addressed. This is followed by the discussions of advanced structures for the enhancement of inductor performance. Research works reported in the literature are summarized to aid the understanding of the recent development of such devices.**

I. INTRODUCTION

In contrast with digital circuits which use mainly active devices, on-chip passive components are necessary and imperative adjuncts to most RF electronics [1-2]. These components, which include inductors, capacitors, varactors, and resistors, have been known as performance as well as cost limiting elements of radio frequency (RF) integrated circuits. While all of these components can be realized using MOS technology, their specific designs necessitate special consideration due to the requirement of high quality factor Q at relatively high frequencies. Inductors in particular are critical components in oscillators and other tuned circuits. For low-frequency applications, passive devices can be connected externally, but as the frequency increases, the characteristics of the passive devices would be overwhelmed by parasitic effect [3]. For instance, a voltage-controlled oscillator (VCO) of 10 MHz needs a tank inductance on the order of several μH, whereas at 10 GHz the inductance is around 1 nH. It's impossible to access such a small inductance externally, since the inductance associated with the package pin and bond wire can exceed 1 nH. As a result, on-chip passive components are commonly used in RF applications.

This paper will focus on the on-chip inductors. Basically there are three types of on-chip inductors. The most widely used type is the planar spiral inductor, and a square shaped spiral inductor is shown in Fig. 1 [4]. Although a circular shaped inductor may be more efficient and yield better performance, the shape of inductor is often limited to the availability of fabrication processes. Most processes restrict all spiral angles to be 90°, and a rectangular/square pattern (hereafter called square pattern) is a nature choice, but a polygon spiral inductor can serve as a compromise between the square and circular shaped inductors. Structural parameters such as the outer dimension, number of turns, the distance between the centers of lines (or pitch), and substrate property are all important factors in determining the performance of on-chip inductors.

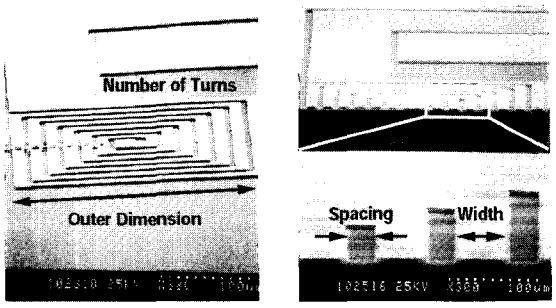

Fig. 1. Topology and cross section of a typical on-chip square shaped spiral inductor (after [4]).

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Besides the spiral inductor, two other kinds of on-chip inductors have been used. Gyrator, or active inductor, utilizes active components (i.e., transistors) to transform the impedance of a capacitor to inductance [5]. Fig. 2 shows the basic gyrator circuit. The active device and capacitor required in the gyrator can be easily fabricated and occupy minimal space, but they consume relatively large power and introduce additional noise. The third on-chip inductor type is constructed with the bond wire [6], as shown in Fig. 3. It can offer a very high quality factor (30~60, typically), but such an approach is likely to cause unwanted coupling to other devices and may not be sufficiently robust for some RF applications. Only spiral inductors are covered in this paper.

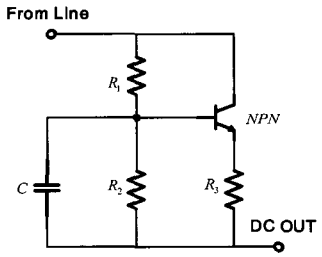


Fig. 2. Equivalent circuit of a basic gyrator.

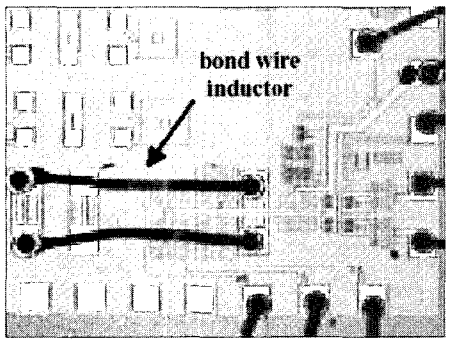


Fig. 3. Schematic of a bond wire inductor (after [6]).

The organization of the paper is as follows. In Section II, square shaped spiral inductors will be considered to address the concept and modeling of on-chip inductors. Advanced features to improve the inductor's performance will be then be presented in Section III. Finally, conclusions are given in Section IV.

II. Concept And Modeling Of Spiral Inductors

Traditionally, spiral inductors are made in square shape due to its ease of design and support from drawing tools [7]. From the performance point of view, however, the most optimum pattern is a circular spiral because it suffers less resistive and capacitive losses. But the circular inductor is not widely used because only a few commercial layout tools support such a pattern. Hexagonal and octagonal structures are good alternatives, as they resemble closely to the circular structure and are easier to construct and supported by most computer-aided design tools. It has been reported that the series resistance of the octagonal and circular shaped inductors is 10% smaller than that of a square shaped spiral inductor with the same inductance value [8].

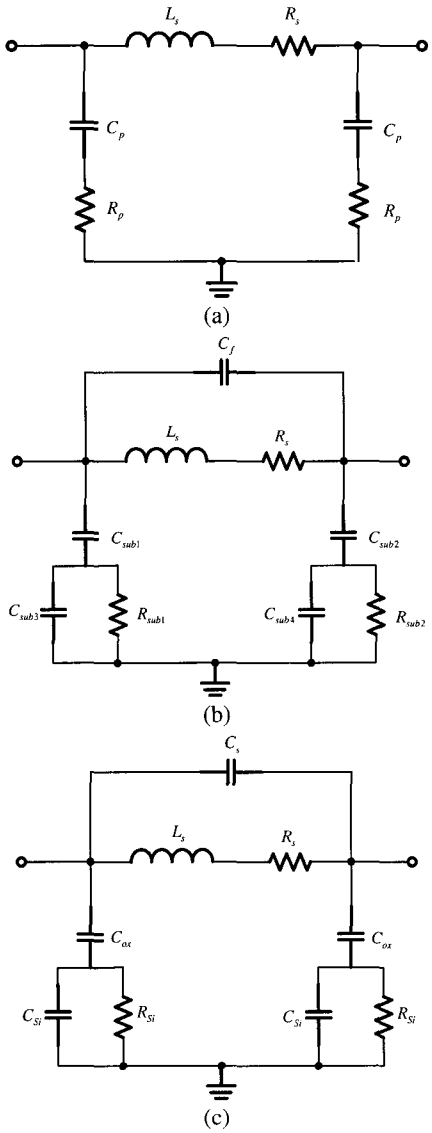


Fig. 4. Lumped π models for spiral inductors developed by (a) Nguyen and Meyer [9]; (b) Ashby et al. [10]; and (c) Yue and Wong [11].

In 1990, Nguyen and Meyer [9] first developed a planar inductor on silicon using the interconnect technology, and they proposed a simple π model to describe the inductor's behavior (see Fig. 4(a)), which can be considered as a section of the ladder model for interconnects. An improved model, shown in Fig. 4(b), was later developed by Ashby et al. [10]. This model accounts for more physical mechanisms taking place in the inductor. However, the model parameters need to be extracted from empirical curve fitting rather than physical means. More recently, Yue and Wong [11] reported an inductor model similar to that in Fig. 4(b), as shown in Fig. 4(c), but with models parameters more relevant to inductor geometry and processing.

In the following subsections, we will consider the square shaped spiral inductor and use the model in Fig. 4(c) as a benchmark to discuss the important issues associated with such a device, including the series inductance (L_S), resistances (R_S and R_{Si}), capacitances (C_S, C_{Si}, and C_{OX}), and quality factor and substrate loss. Note that these issues strongly correlate with the components in the equivalent circuit given in Fig. 4(c) for modeling the on-chip inductor.

1. Series Inductance

It is quite obvious that the knowledge of series inductance is critical to engineers who develop and utilize on-chip inductors for RF IC's. The inductance represents the magnetic energy stored in the device, although parasitic components may store energy as well. Numerical simulators computing the electromagnetic field distribution can be used to calculate the inductance, but our focus here is to determine such a parameter through analytical means, as the latter is less complicated and provides more physical insights.

In 1946, Grover derived formulas for the inductance of various inductor structures [12]. Greenhouse later applied the formulas to calculate the inductance of a square shaped inductor [13]. He divided the inductor into straight-line segments, and calculated the inductance by summing the self inductance of the individual segment and mutual inductance between any two parallel segments. The model has the form of

$$L_S = L_0 + M_+ - M_- \tag{1}$$

where L_S is the total series inductance, L_0 is the sum of the self inductance of all the straight segments, M_+ is the sum of the positive mutual inductances and M_- is the sum of the negative mutual inductances. Self inductance L'_0 of a particular segment can be expressed as

$$L'_0 = 2l\left(\ln\frac{2l}{w+t} + 0.5 + \frac{w+t}{3l}\right) \tag{2}$$

L'_0 is the inductance in nH, l is the length of a segment in cm, w is the width of a segment in cm, and t is the metal thickness in cm. The mutual inductance between any two parallel wires can be calculated using

$$M = 2lQ' \tag{3}$$

where M is the mutual inductance in nH and Q' is the mutual inductance parameter

$$Q' = \ln\left[\frac{l}{GMD} + \sqrt{1+\left(\frac{l}{GMD}\right)^2}\right] - \sqrt{1+\left(\frac{l}{GMD}\right)^2} + \frac{l}{GMD} \tag{4}$$

GMD denotes the geometrical mean distance between the two wires. When two parallel wires are of the same width, GMD is reduced to

$$\ln GMD = \ln d - \frac{w^2}{12d^2} - \frac{w^4}{60d^4} - \frac{w^6}{168d^6} - \frac{w^8}{360d^8} - \frac{w^{10}}{660d^{10}} - \cdots \tag{5}$$

d is the pitch of the two wires. Note that the mutual inductance between two segments that are perpendicular to each other is neglected. As the number of segments increases, the calculation complexity is increased notably because it is proportional to (number of segments)^2. Another drawback of the model is its limitation to only square shaped inductors.

The above model could be simplified using an averaged distance for all segments rather than considering the segments individually [14]. Based on this approach, the self and mutual inductances are calculated directly as

$$L_0 = \frac{\mu_0}{4\pi} l\left(\ln\frac{l_T}{n(w+l)} - 0.2\right) \tag{6}$$

$$M_{-} = \frac{\mu_0}{4\pi} l_T \frac{n}{214} \tag{7}$$

$$M_{+} = \frac{\mu_0}{4\pi} l_T (n-1)\left[\ln\left(\sqrt{1+\left(\frac{l_T}{4nd}\right)^2}+\frac{l_T}{4nd}\right)-\sqrt{1+\left(\frac{4nd}{l_T}\right)^2}+\frac{4nd}{l_T}\right] \tag{8}$$

where μ_0 is the permeability of vacuum, l_T is the total inductor length, n is the number of turns, and d' is the averaged distance of all segments:

$$d' = (w+s)\left(\sum_{i=1}^{(n-i)>0} i(n-i) \Big/ \sum_{i=1}^{(n-i)>0} (n-i)\right) \tag{9}$$

Mohan developed another method which further simplifies the calculations based on the current sheet concept [15]. His method serves as an adequate approximation for geometries where the conductor thickness is dwarfed by the length and width, and has the advantage of easily extendable to other geometries (i.e., octagonal and circular).

The methods mentioned above offer various solutions to estimate the inductance of a square shaped inductor. Some empirical techniques based on curve fitting have also been reported in [16]-[18], however models derived in this way cannot be scaled to reflect changes in the inductor's layout or fabrication technology.

2. Resistances

Series resistance R_S (see Fig. 4(c)) arises from the metal resistivity in the inductor and is closely related to the quality factor. As such, the series resistance is a key issue for inductor modeling. When the inductor operates at high frequencies, the metal line suffers from the skin and proximity effects, and R_S becomes a function of frequency [19]. As a first-order approximation, the current density decays exponentially away from the metal-SiO_2 interface, and R_S can be expressed as [11]:

$$R_S = \frac{\rho \cdot l_T}{w \cdot t_{eff}} \tag{10}$$

Where ρ is the resistivity of the wire, and t_{eff} is given by

$$t_{eff} = \delta \cdot \left(1 - e^{-t/\delta}\right) \tag{11}$$

t is the physical thickness of the wire, and δ is the skin depth which is a function of the frequency:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{12}$$

where μ is the permeability in H/m and f is the frequency in Hz.

The most severe drawback of a frequency-dependent component, such as R_S, in a model is that it cannot be directly implemented in a time domain simulator, such as Cadence Spectre. Researchers have proposed to use frequency-independent components to model frequency-dependent resistance [19]-[25]. Ooi et al. [21] replaced R_S with a network of 2 R's and 1 L, where R and L are frequency-independent components, in the inductor equivalent circuit, as shown in the dashed line box in Fig. 5(a). The total equivalent resistance R_{total} of the box is

$$R_{total} = R_0\left[1 + \frac{\omega^2\left(0.035 w^4 t^2 \sigma^2 \mu_0^2\right)}{P^2} \sum_{n=1}^{N}\left(\frac{n-M}{N-M}\right)^2\right] \tag{13}$$

where R_0 is the steady-state series resistance, ω is the radian frequency, P is the turn pitch, t is the inductor thickness, w is the inductor width, σ is the conductivity, N is the total number of turns, and M is the turn number where the field falls to zero. This expression coincides with the approach based on the square-law relationship proposed in [22]. Fig. 5(b) compares the measured and simulated series resistances of two different inductors. Another approach [23] used an R-L ladder to model the frequency-dependant resistor, which gives better flexibility and accuracy. Figs. 6(a) and (b) show the equivalent circuit of R-L ladder model and the series resistance results, respectively. Melendy et al. [24] used a series of R-L loops to represent the effect of series resistance, see Figs. 7(a) and (b). Another method is to average the different parameter values associated with R over the frequency [25].

Coupling resistance R_{Si} associated with the Si substrate (see Fig. 4(c)) also degrades the inductor performance. A simple model to describe the substrate

resistance is given by [11]

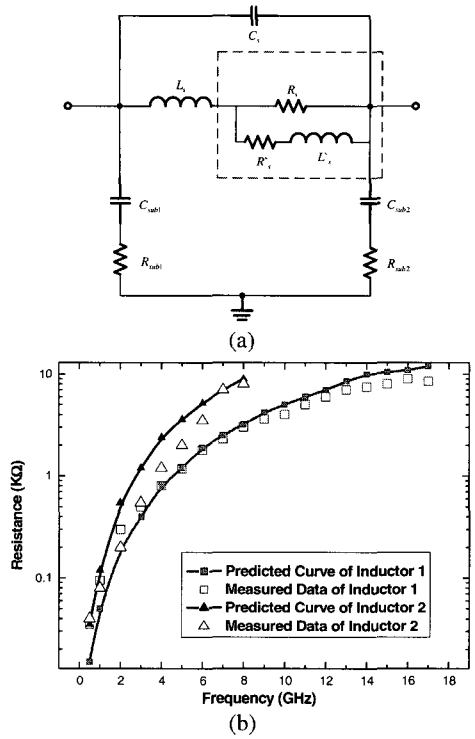


Fig. 5. (a) Model with improved series resistance (dashed line box) developed by Ooi et al. and (b) resistances measured and simulated for two different inductors (after [21]).

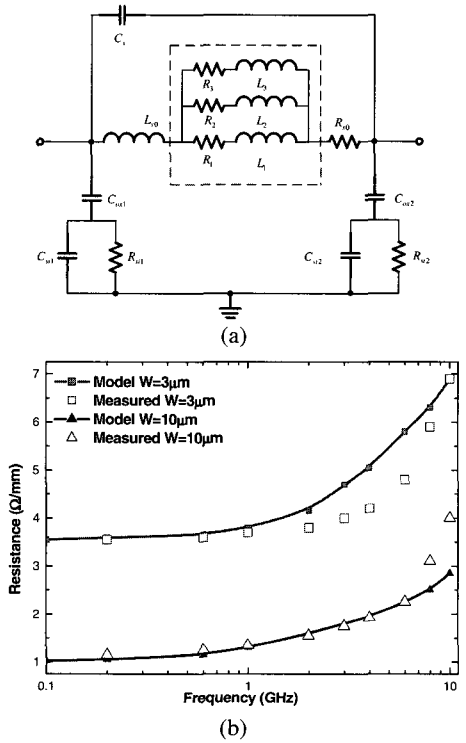


Fig. 6. (a) Model with improved series resistance (dashed line box) developed by Rotella et al. and (b) resistances measured and simulated for two different inductors (after [23]).

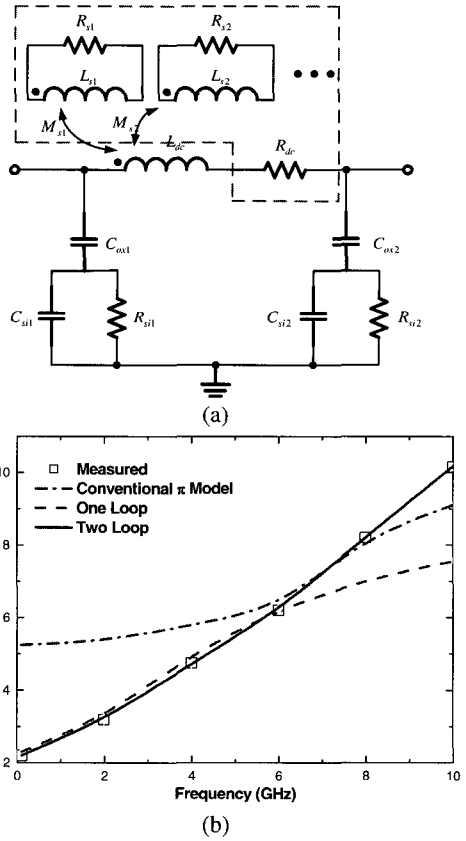


Fig. 7. (a) Model with improved series resistance (dashed line box) developed by Melendy et al. and (b) resistances measured and simulated from the conventional model and improved model with one and two R/L loops in the dashed line box (after [24]).

$$R_{Si} = \frac{2}{l \cdot \mathrm{w} \cdot G_{sub}} \tag{14}$$

where l is total length of all line segments, G_{sub} is the conductance per unit area of the substrate.

3. Capacitances

There are basically three types of capacitances in an on-chip inductor: the series capacitance C_S between metal lines, the oxide capacitance C_{OX} associated with the oxide layer, and the coupling capacitance C_{Si} associated with the Si substrate. Traditionally, they are modeled using the parallel-plate capacitance concept [11]:

$$C_s = n \cdot \mathrm{w}^2 \cdot \frac{\varepsilon_{ox}}{t_{oxM1-M2}} \tag{15}$$

$$C_{ox} = \frac{1}{2} \cdot l_T \cdot \mathrm{w} \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{16}$$

$$C_{Si} = \frac{1}{2} \cdot l_T \cdot \mathrm{w} \cdot C_{sub} \tag{17}$$

where n is the number of overlaps, w is the spiral line width, C_{sub} is the capacitance of the substrate, t_{ox} is the oxide thickness underneath the metal, and $t_{oxM1\text{-}M2}$ is the oxide thickness between the spiral. An improved method [26], which evaluates the voltage and energy stored in each turn, leads to the equivalent capacitances of C_p and C_{sub}, as shown in Fig. 8. Compared to the model in Fig. 4(c), C_p and C_{sub} in this model are equivalent to C_S and the combination of C_{ox} and C_{Si}, respectively,

$$C_p = \sum_{k=1}^{n-1} \frac{1}{4} C_{mm} l_k [d(k+1) - d(k-1)]^2 \tag{18}$$

$$C_{sub} = \sum_{k=1}^{n} \frac{1}{4} C_{ms} A_k [2 - d(k-1) - d(k)]^2 \tag{19}$$

$$d(k) \equiv h_1 + h_2 + \Lambda\ h_{k-1} + h_k \tag{20}$$

$$h_k = (l_k / l_T) \tag{21}$$

$$Q = 2\pi \cdot \left(\frac{\textit{Peak Magnetic Energy - Peak Electric Energy}}{\textit{Energy Loss in One Oscillation Cycle}} \right) \tag{22}$$

where C_{ms} represents the capacitance per unit area between the m^{th} metal layer and the substrate, C_{mm} represents the capacitance per unit length between adjacent metal tracks, A_k is the track area of k^{th} turn and l_k is the length of k^{th} turn. The model also implies that C_S is a function of the index difference of each adjacent segment pair. This means that the larger the index difference between the two adjacent lines, the higher the capacitance [27]. This concept can be used to improve the inductor structure to be discussed in Section III.

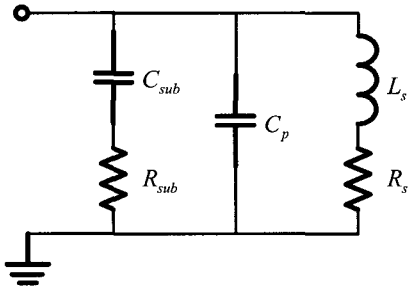


Fig. 8. Equivalent circuit of spiral inductor developed by Wu et al. [26].

4. Q Factor and Substrate Loss

The quality factor Q is an extremely important figure of merit for the inductor at high frequencies. For an inductor, only the energy stored in the magnetic field is of interest, and the quality factor is defined as [28]

Basically, it describes how good an inductor can work as an energy-storage element. In the ideal case, inductance is pure energy-storage element (Q approaches infinity), while in reality parasitic resistance and capacitance reduce Q. This is because the parasitic resistance consumes stored energy, and the parasitic capacitance reduces inductivity (the inductor can even become capacitive at high frequencies). Self-resonant frequency f_{SR} marks the point where the inductor turns to capacitive and, obviously, the larger the parasitic capacitance, the lower the f_{SR}.

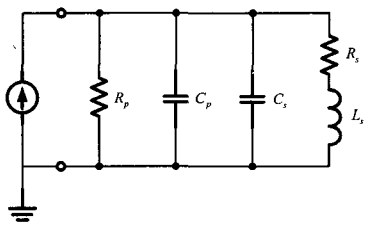


Fig. 9. Equivalent circuit of one terminal grounded inductor for modeling the Q factor.

If the inductor has one terminal grounded, as in typical applications, then the equivalent circuit of the inductor can be reduced to that shown in Fig. 9. From such a model, the quality factor Q of the inductor can be derived as [28]:

$$Q = \frac{\omega L_s}{R_s} \cdot \frac{R_p}{R_p + \left[(\omega L_s / R_s)^2 + 1\right] R_s} \cdot \left[1 - \frac{R_s^2 (C_s + C_p)}{L_s} - \omega^2 L_s (C_s + C_p) \right]$$
$$= \frac{\omega L_s}{R_s} \cdot \textit{Substrate Loss Factor} \cdot \textit{Self Resonance Factor} \tag{23}$$

where ω is the radian frequency, L_S is the series inductance, R_S is the series resistance, R_P is the coupling resistance, and C_P is the coupling capacitance. R_P and C_P in Fig. 9 are related to R_{Si}, C_{Si}, and C_{OX} in the model in Fig. 4(c) as

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{Si}} + \frac{R_{Si} (C_{ox} + C_p)^2}{C_{ox}^2} \tag{24}$$

$$C_p = C_{ox} \cdot \frac{1+\omega^2(C_{ox}+C_{Si})C_{Si}R_{Si}^2}{1+\omega^2(C_{ox}+C_{Si})^2 R_{Si}^2} \qquad (25)$$

Note that Q increases with increasing L_S and with decreasing R_S. Moreover, it appears from (23) that Q should increase monotonically with the frequency. This is not the case, however, as the substrate loss becomes a dominant factor for Q at high frequencies. The last two terms on the right-hand side of (23) denote the substrate loss factor and self-resonant factor. On-chip inductors are normally built on a conductive Si substrate, and the substrate loss is due mainly to the capacitive and inductive coupling [7]. The capacitive coupling (represented by C_P in the model in Fig. 9) from the metal layer to the substrate changes the substrate potential and induces the displacement current. The inductive coupling is formed due to time-varying magnetic fields penetrating the substrate, and such a coupling induces the eddy current flow in the substrate. Both the displacement and eddy currents give rise to the substrate loss and thereby degrade the inductor performance. Fig. 10 illustrates schematically the eddy and displacement currents in the substrate induced magnetically and electrically, respectively, by the current flow in the inductor spiral.

An important conclusion can be drawn from (23), that is when R_P approaches infinity, the substrate loss factor approaches unity. Since R_P approaches infinity when R_{Si} goes to zero or infinity, Q can be improved by making the silicon substrate either a short or an open [28].

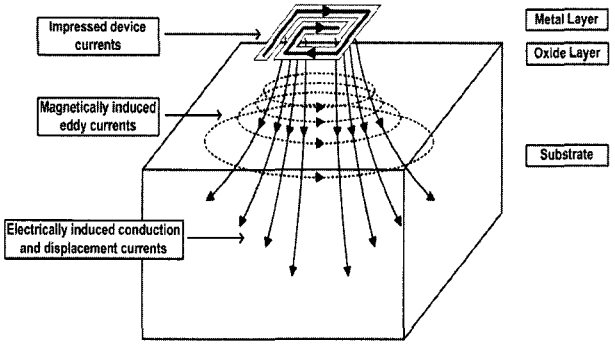
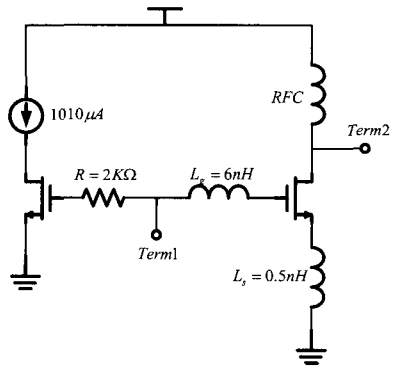
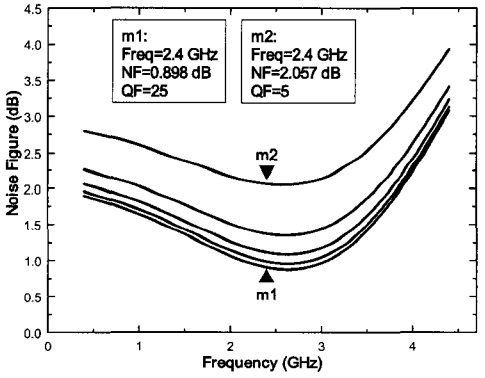


Fig. 10. Eddy and displacement currents in the substrate induced by the current flow in inductor spiral.

We use an example below to explain the importance of Q factor. Figs. 11(a) shows a typical low-noise amplifier (LNA) with two active inductors and an ideal inductor with infinite inductance serving as RF choke (RFC). Figs. 11(b) and (c) show the simulated noise figure and current gain, respectively, for the LNA when the Q factors of the two inductors are assumed equal and changed from 5 to 25. Clearly, the RF performances of the LNA are degraded when the inductors' Q factor is reduced.



(a)



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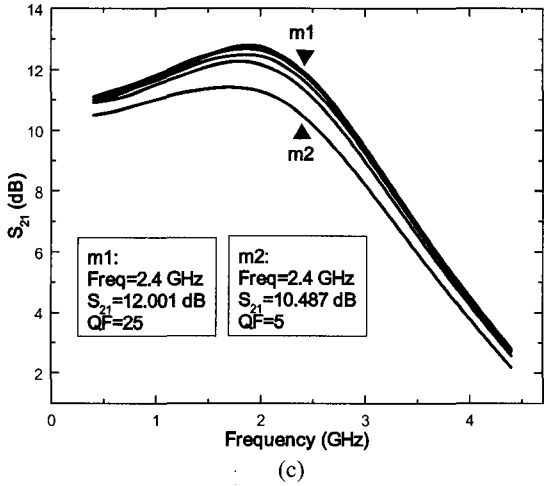
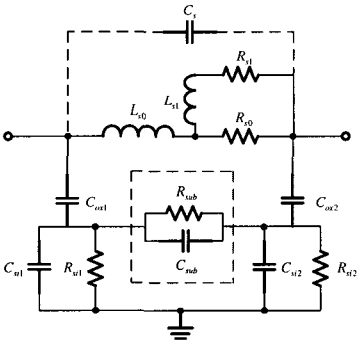


(c)

Fig. 11. (a) A typical low-noise amplifier, (b) simulated noise figures, and (c) simulated small-signal current gains. In the simulations, the two active inductors were assumed having the same Q factors and the Q factors were increased from 5 to 25.

5. Modified π Models

Some studies have been conducted to improve the accuracy of the simple lumped models shown in Fig. 4. Gil and Shin [29] modified the simple π model by adding the horizontally coupled substrate resistor and capacitor, and the equivalent circuit and results of Q factor are given in Figs. 12(a) and (b). Cao et al. [19] proposed a double π model to account for the frequency-dependant resistance and inductance, in which the frequency-independent resistance components follow the square-law relationship suggested in [21]-[22] and the frequency-independent inductance components are derived based on mutual inductances and calculated from empirical equations. The equivalent circuit and model results are given in Figs. 13(a) and (b). Lakdawala et al. [30], on the other hand, used an RLC laddered network to describe the frequency-dependent resistance and inductance, as shown in Fig. 14(a). The measured and calculated Q factors of a conventional and micromachined inductors are given in Fig. 14(b). The models in Figs. 6(a) and Fig. 7(a) could also yield good predictions for Q, and the results are shown in Figs. 15(a) and (b), respectively.



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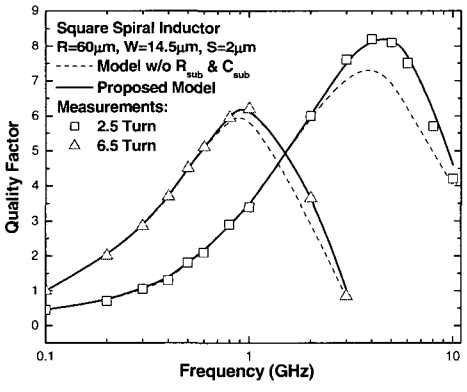
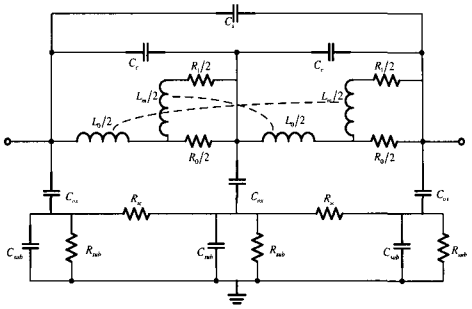
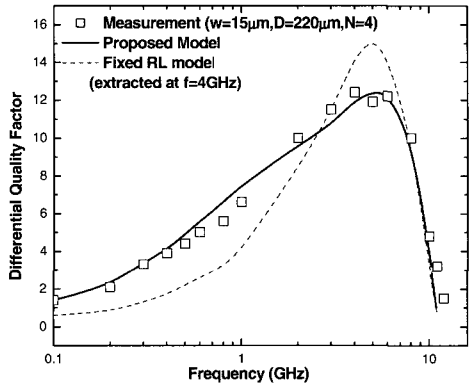


(b)

Fig. 12 . (a) Improved inductor model with horizontally coupled resistance and capacitance (R_{sub} and C_{sub}) and (b) Q factors measured and simulated with and without R_{sub} and C_{sub} (after [29]).

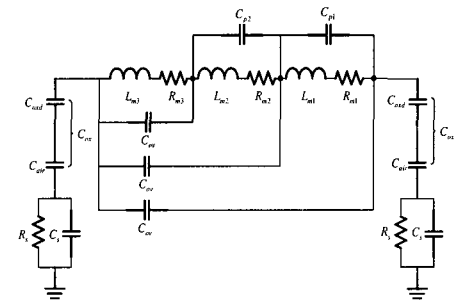


(a)

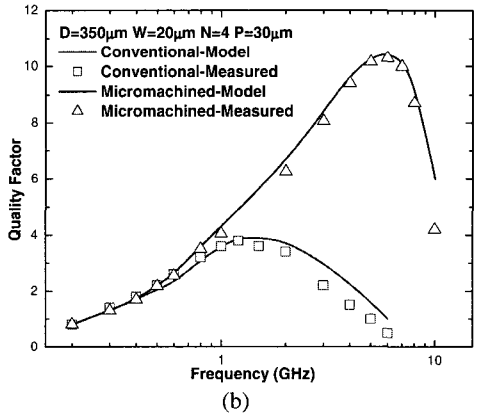


(b)

Fig. 13. (a) Improved double π model to more accurately account for the frequency-dependent series resistance and inductance and (b) Q factors measured and simulated from the conventional and improved models (after [19]).



(a)



(b)

Fig. 14. (a) Modified π model with RLC laddered network and (b) Q factors measured and calculated from the modified model (after [30]).

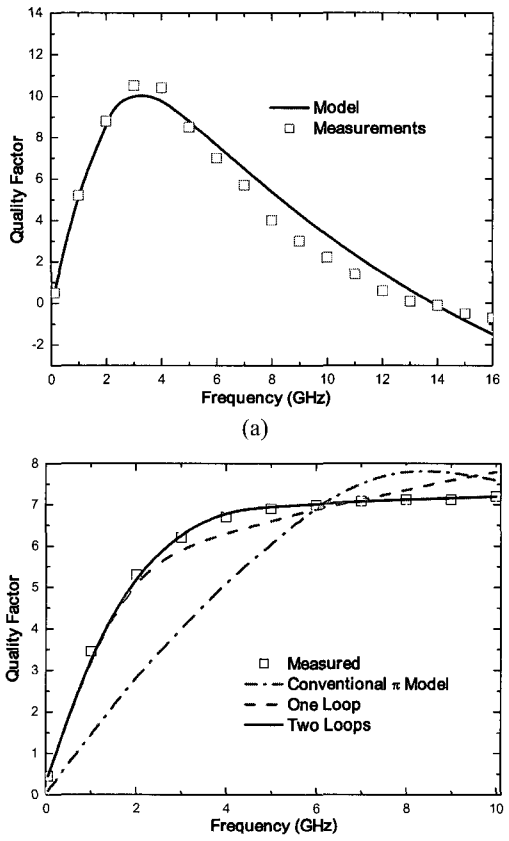


Fig. 15. (a) Quality factors measured and calculated from model in Fig. 7(a); (b) Inductances and quality factors measured and calculated from model in Fig. 8(a).

III. ADVANCED STRUCTURES

The preceding section has addressed the design concept and modeling of a typical square shaped spiral inductor. The performance of such an inductor can be improved with the following advanced structures.

1. Structures to Reduce Substrate Loss

1.1 Ground Shield

As mentioned earlier, the substrate loss can be reduced with decreasing the substrate resistance R_{Si}. To achieve this, one can insert a metal or ploy-Si layer between the inductor and substrate, and connect this layer to the ground. This approach, called the ground shielding, reduces the effective distance between the spiral metal and ground and thereby reduces the substrate coupling resistance. Another purpose of the shield is that it can truncate the electric field in the substrate and thus reduce the noise. For a solid ground shield (SGS), however, the varying electromagnetic field in the inductor could induce the eddy current with the presence of ground plane, and the reflected image in the ground plane serves as a counteractive inductor [31]. Hence, it's necessary to pattern the shield to cut the eddy current loop [28],[32]. It has been found that poly-Si is a good material for the patterned ground shield (PGS). Chen et al. [33] reported the use of an n^+-diffusion Si patterned ground shield to improve the quality factor. Since the substrate current mainly concentrates at the Si-SiO_2 surface due to the proximity effect, the n^+-diffusion Si PGS can effectively break the current loop and thus eliminate the eddy current effect [34]. Figs. 16(a) and (b) show a typical PGS and the results of quality factor Q with SGS and PGS. Clearly, the presence of PGS improves Q considerably.

The most significant drawback of ground shielding is the fact that it reduces the distance between inductor and ground and thereby introduces additional capacitance. This effect may sometimes adversely decrease the quality factor of ground-shielding inductors [35].

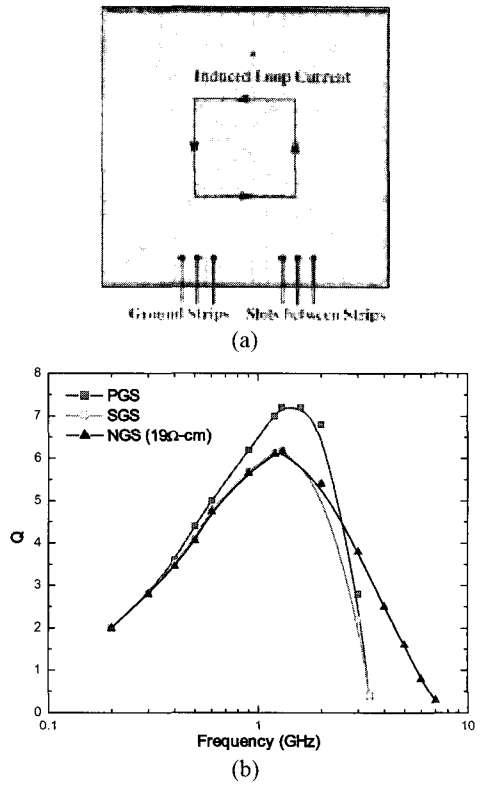
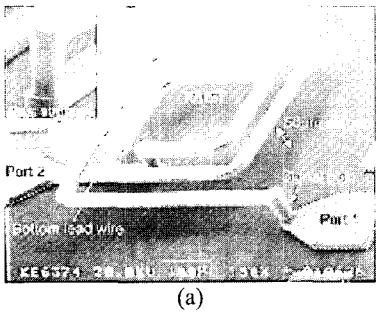


Fig. 16. (a) Schematic of patterned ground shield (PGS) and (b) quality factors of solid ground shield (SGS), PGS, and no ground shield (NGS) (after [28]).

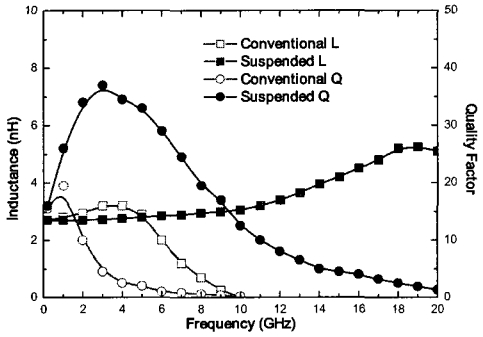
1.2 Substrate Removal

Another way to enhance Q is to increase the substrate resistance. In order to elevate R_{Si} to approaching infinity, one idea is to use insulator as substrate. Quartz or glass shows better Q and higher self-resonant frequency than Si [35]. For Si technology, however, it is not possible to use a high resistive substrate as an effective RF ground, and via contacts through the chip to define RF grounds on both the chip front side and back side is usually not available. In other words, for CMOS-based on-chip inductors, we cannot avoid using a low resistive Si substrate. Nonetheless, instead of building the whole circuit on a low resistive substrate, we can make a region with high resistivity for placing the inductor [36]. This can be accomplished by using the proton implantation, and Chan et al. [36] achieved a 7% higher self-resonant frequency and 61% higher Q through this approach.

Researchers have come up with other novel ideas to keep the inductor away from substrate so that substrate coupling and loss can be greatly reduced. Using an advanced micromachinary process, an inductor can be built above the silicon surface [30], [37]-[38], as shown in Figs. 17 and 18, or the silicon underneath the inductor can be removed using the deep-trench technology [39], as shown in Fig. 19.

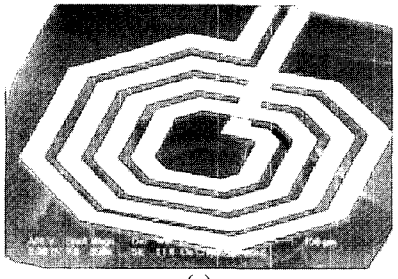


(a)

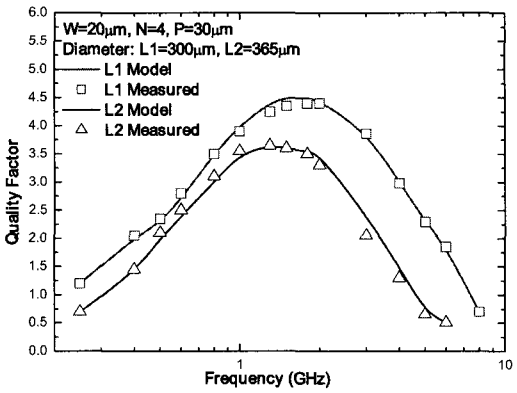


(b)

Fig. 17. (a) Topology of the suspended inductor and (b) comparison of inductances and Q factors of conventional and suspended inductors (after [37]).

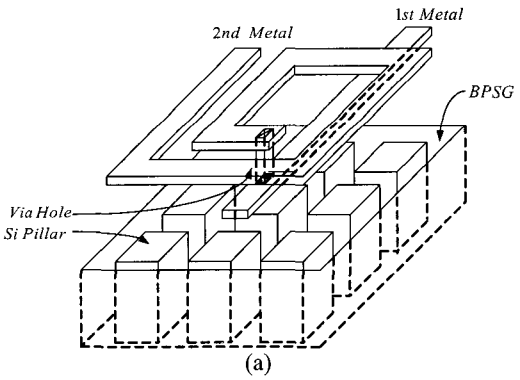


(a)

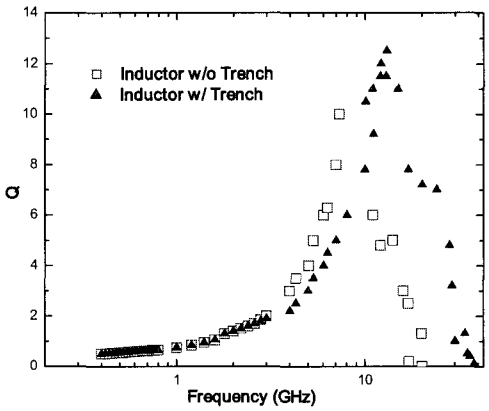


(b)

Fig. 18. (a) Topology of the micromachined inductor and (b) Q factors of such an inductor with two different diameters (after [30]).



(a)

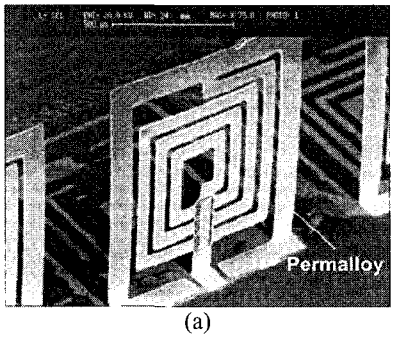


(b)

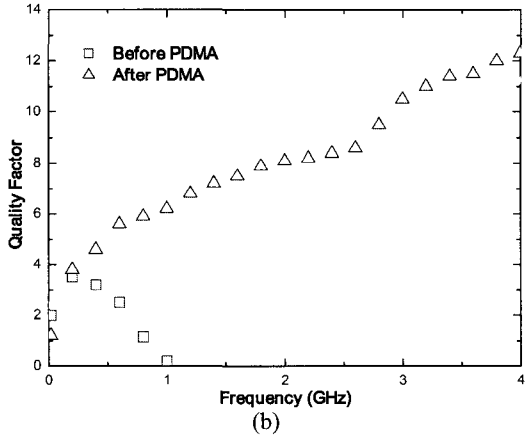
Fig. 19. (a) Inductor with substrate removed by a deep trench technology and (b) Q factors of conventional and trenched inductors (after [39]).

1.3 Horizontal Inductors

An alternative way to reduce magnetic field coupling to substrate is to have the magnetic field parallel to the substrate. To this end, research works have been done to fabricate horizontal inductors with multilayer of interconnects [40]-[41]. Using this layout, the magnetic field is parallel to the substrate surface and the magnetic coupling to the substrate is minimal. This structure nevertheless gives rise to an increased in the coupling capacitance. Since a large metal is needed for the bottom layer of the horizontal inductor, the inductor-substrate capacitance increases tremendously if the inductor is on silicon. Again, researchers tried to use high resistive substrate [41], suspend the inductor in air [42], or even rectify the inductor with the so-called plastic deformation magnetic assembly (PDMA) [43]. Figs. 20(a) and (b) show the topology and performance of a horizontal inductor using the PDMA.



(a)



(b)

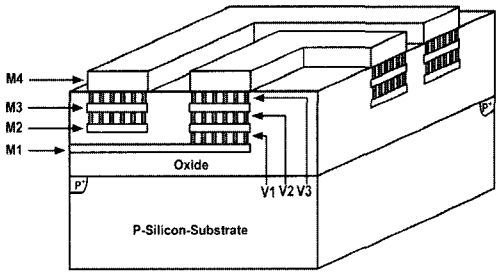
Fig. 20. (a) Topology of the horizontal inductor based on the PDMA process and (b) Q factors of conventional and horizontal inductors (after [43]).

2. Structures to Reduce Series Resistance

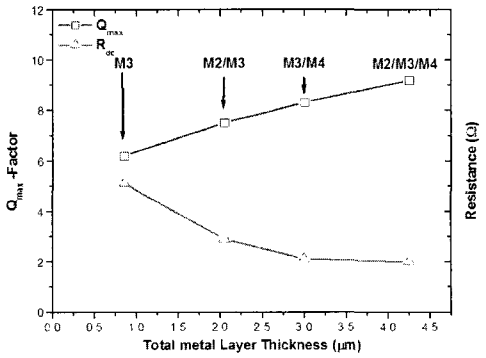
Metal resistivity gives rise to the series resistance R_S, and it is always desired to reduce the resistance in order to improve the quality factor. One simple idea is to increase the line width. This method may work at low frequencies where the current density in a wire is uniform; however, as the frequency increases, the skin effect pushes the more current to the outer cross section of the metal wire and the so-called skin depth (i.e., the depth in which the current flows) is reduced with increasing frequency (see Eq. (12)). Thus, the skin effect increases the series resistance at high frequencies, and the approach of increasing the line width would not be effective. According to an earlier study, the larger the cross section, the lower the onset frequency at which the skin effect dominates the series resistance. Furthermore, a wider metal line would occupy more area, which increases the fabrication cost. Several possible solutions to this problem are given below.

2.1 Vertical Shunt

In this approach, the inductor is made of multiple metal layers and the neighboring metal layers are shunted through via arrays, so the effective thickness of the spiral inductor is increased, the skin effect is weakened, and the series resistance is reduced. A detailed study and comparison on the multilayer inductors are presented in [44].



(a)



(b)

Fig. 21. (a) Inductor with multiple metal layers and vertical shunt and (b) maximum Q factors and resistances for the inductor having different numbers of vertical shunt (after [44]).

The inductors are fabricated with multiple metal layers (M1 to M4), and these layers can be shunted through via arrays, as shown in Fig. 21(a) for the case of shunting M2, M3 and M4. The results in Fig. 21(b) show a reduced series resistance and thus an improved Q as the number of shunts is increased (i.e., the case of M3 has no vertical shunt). The performance of the inductor is therefore optimized with the increment of total metal thickness without occupying more area. One important aspect the inductor in Fig. 21 did not address is that the inductor may experience a lower self-resonant frequency with the utilization of lower metal layers. This is because 1) the reduction of metal-substrate distance could cause a significant increase in C_{ox}, and 2) the capacitance among the metal lines would also increase.

2.2 Horizontal Shunt

Instead of shunting vertically, the spiral inductor can be split into several shunting current paths, each with an identical resistance and inductance. This approach, called the horizontal shunt, can suppress the current crowding and increase the Q factor [45]. Figs. 22(a) and (b) show such an inductor and its Q factor, respectively. It is shown that for the same line width, the Q factor increases with increasing number of splits.

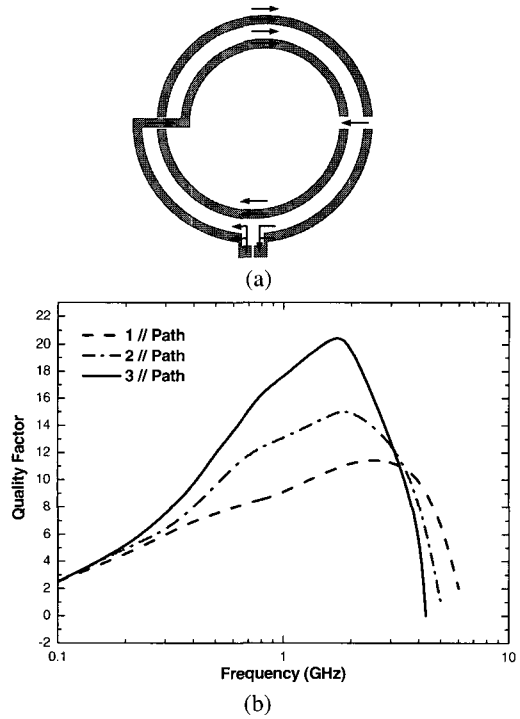


Fig. 22. (a) Inductor with metal line split into shunt current paths and (b) Q factors of horizontally shunt inductor with one, two, and three splits in the metal line (after [45]).

2.3 Line Width Optimization

For inductors fabricated with a constant line width, the influence of magnetically induced losses is much more significant in the inner turns of the spiral, where the magnetic field reaches its maximum. To avoid this effect, one method is to employ the so-called tapered inductor, in which the line width decreases toward the center of the spiral [46], as shown in Fig. 23(a). A reduced series resistance can also be achieved from this approach. Detailed study was performed in [47] regarding the optimization of line width in order to enhance the RF performance. The frequency- and position-dependent optimum width W_{opt} is given by:

$$W_{opt,n} = \sqrt[3]{\frac{r_s(f)}{2 \cdot C \cdot g_n^2 \cdot f^2}} \tag{26}$$

where $r_s(f)$ is the sheet resistance of the metal strip, f is the frequency, C is a fitting constant, and g_n is a geometric dependent parameter. As can be seen in Fig. 23(b), the Q factor of a spiral inductor is much improved when the line width is not uniform and is optimized.

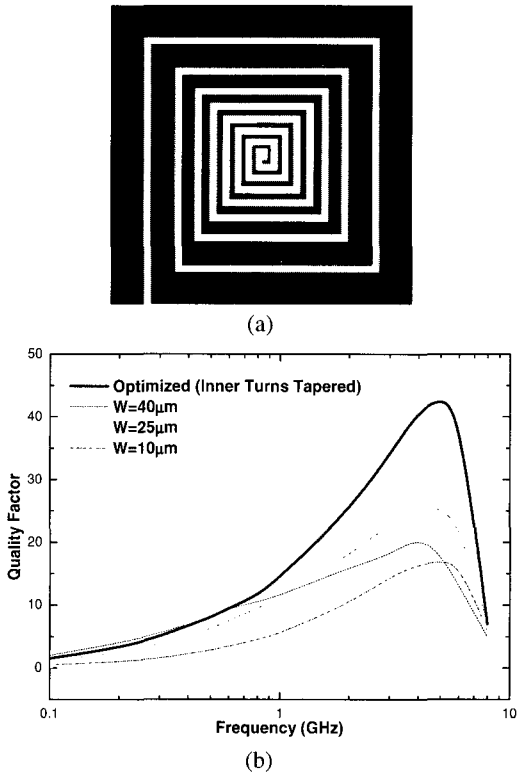


Fig. 23. (a) Topology of a tapered inductor and (b) Q factors of a tapered inductor and three non-tapered inductors (after [47]).

3. Structures to Increase Inductance

Since the quality factor is directly proportional to the series inductance, approaches to increase the inductance have also been suggested for on-chip inductor performance enhancement.

3.1 Stacked Inductor

A stacked inductor is a set of series inductors made from different metal layers, as illustrated in the schematic in Fig. 24(a). This method maximizes the inductance per unit area. It has been reported that a 10 nH inductor can be achieved with an area of 22 μm × 23 μm, as opposed to several hundreds μm by several hundreds μm for regular inductors [48]. This is the main advantage that this technology can offer. Shortcomings are relatively low Q factor and self-resonant frequency, due to the increased substrate capacitance and line to line coupling capacitance. The Q factor and inductance of such an inductor are illustrated in Fig. 24(b).

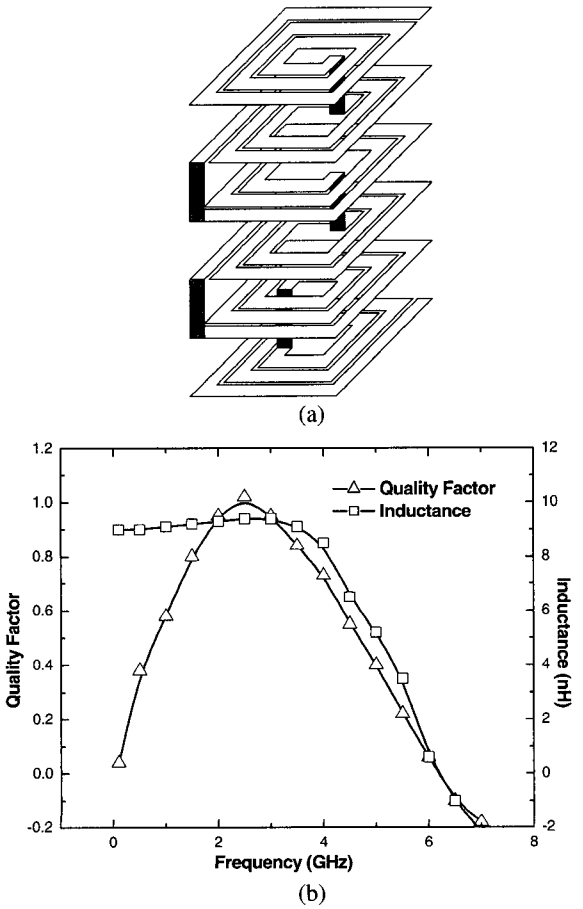


Fig. 24. (a) Stacked inductor with six metal layers and (b) Q factor and inductance of the stacked inductor (after [48]).

3.2 Miniature 3-D Inductor

A high-performance stack-like inductor, called the miniature 3-D inductor, was proposed in [49]. Fig. 25(a) shows such an inductor, which consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in every metal layer. The miniature inductor, while quite complicated, possesses a minimal coupling capacitance. This leads to a much higher self-resonant frequency and a wider frequency range for high quality factor. Comparisons of capacitances and Q factors obtained from this inductor and a typical stacked inductor are given in Figs. 25(b) and (c), respectively.

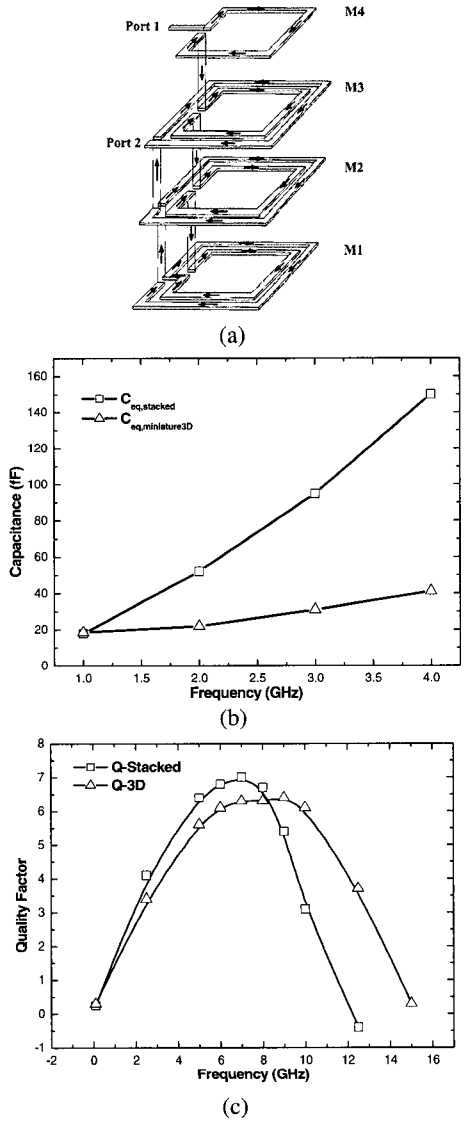


Fig. 25. (a) Structure of the miniature 3-D inductor, (b) capacitances of typical stacked and 3-D inductors, and (c) Q factors of typical stacked and 3-D inductors (after [49]).

4. Symmetrical Inductor

Traditionally, the winding of an inductor spiral starts from the outer turn to inner turn and then goes back out through an underpass. This is called the non-symmetrical inductor, as shown in Fig. 26(a). An improved structure with a symmetrical winding, called the symmetrical inductor shown in Fig. 26(b), will yield better performances [50]. This is because in the symmetrical inductor the geometric center of the symmetrical inductor is exactly the magnetic and electric center, which increases the mutual inductance and consequently the total inductance. Performances of the symmetrical and non-symmetrical inductors are illustrated in Figs. 27(a), (b) and (c). While the Q factor and series resistance of the symmetrical inductor are improved, the self-resonant frequency (i.e., frequency at which the inductance is zero) of such an inductor is reduced. This is due to an increased ac potential difference between the neighboring turns in the symmetrical inductor, a mechanism that increases the coupling capacitance and degrades the self-resonant frequency [26].

The symmetrical inductor can be further enhanced with a dual-layer structure, as shown in Fig. 28(a) [51]. The results in Fig. 28(b) suggest that this structure possesses a much higher Q factor over its single-layer counterpart.

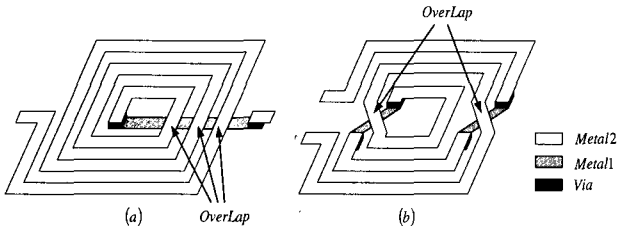
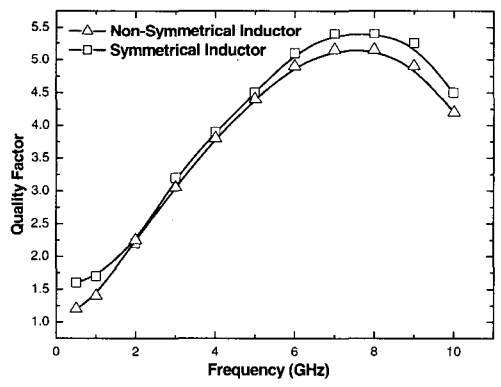
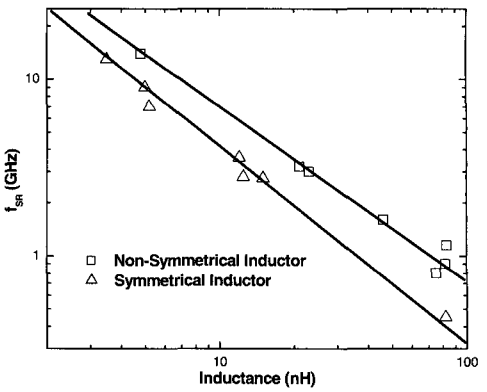


Fig. 26. Spiral pattern of (a) non-symmetrical inductor and (b) symmetrical inductor.



(a)



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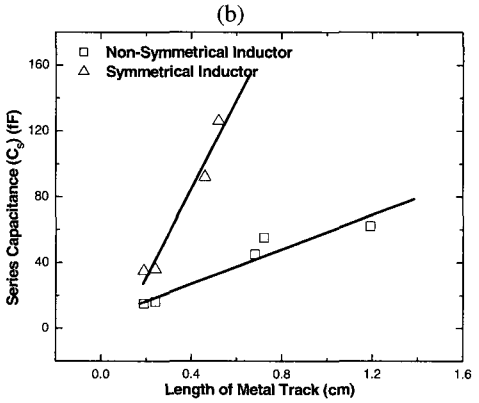
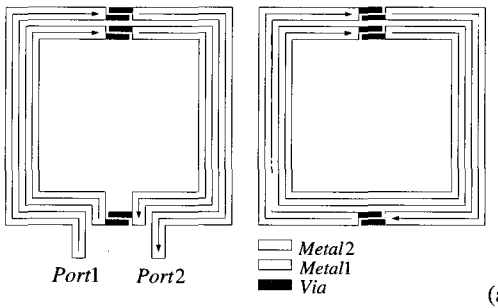
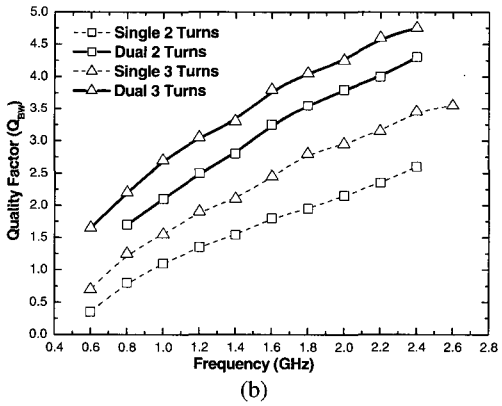


(c)

Fig. 27. Comparison of (a) Q factor [50], (b) self-resonant frequency [27], and (c) capacitance [27] of non-symmetrical and symmetrical inductors.



(a)



(b)

Fig. 28. (a) Structure of the dual-layer symmetrical inductor and (b) Q factors of single and dual-layer symmetrical inductors (after [51]).

5. Alternative Patterns

The preceding discussions have focused mainly on square shaped spiral inductors. As mentioned earlier, while the circular shaped inductor yields better performance, such a pattern is more difficult to realize than its square counterpart. On the other hand, alternatives like the hexagonal and octagonal patterns are more feasible and good compromises. For these inductors, as the number of sides is increased, less metal length is needed to achieve the same number of turns. Thus series resistance is compressed and Q factor improved. On the other hand, the square shaped inductor is more area efficient. For example, for a square area on the wafer, square shape utilizes 100% of the area, whereas hexagonal, octagonal and circular shapes use 65%, 82.8% and 78.5%, respectively. As a result, square inductor can accommodate more metal line, thus yielding a larger inductance, within the same square area.

Selection of the pattern shape is a compromise between quality factor and area. Mohan [15] studied inductors with different shapes having a fixed inductance of 5 nH. As shown in Fig. 29, the quality factor is improved with increasing number of sides (note that circular pattern can be considered as having infinite number of sides). The study further suggested that an octagonal spiral inductor suffers a 3~5% lower Q factor but achieves a 3~5% smaller effective chip area than the circular spiral inductor [15].

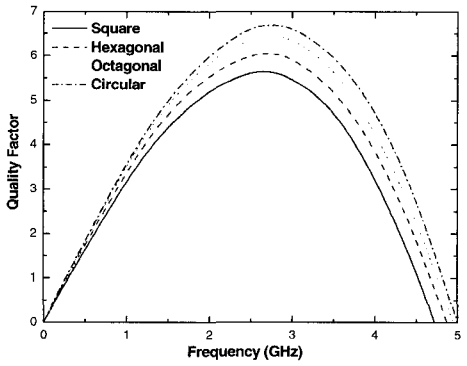


Fig. 29. Q factors of different shaped inductors with a fixed inductance of 5 nH (after [15]).

The quality factor and inductance of square and octagonal shaped inductors having the same inner diameter are compared in Figs. 30(a) and (b) [52]. The square inductor possesses a higher peak inductance but a lower self-resonant frequency. This is because the longer metal line of square inductor induces a larger metal to substrate coupling capacitance, which reduces the inductance at high frequencies. For low frequencies, the inductor performance depends mainly on the length of the spiral wire, and the square pattern possesses a larger inductance in this region. Experiments of other research works also indicated an up to 10% resistance reduction of circular and octagonal inductor over the square inductor with the same inductance [8], as illustrated in Fig. 31.

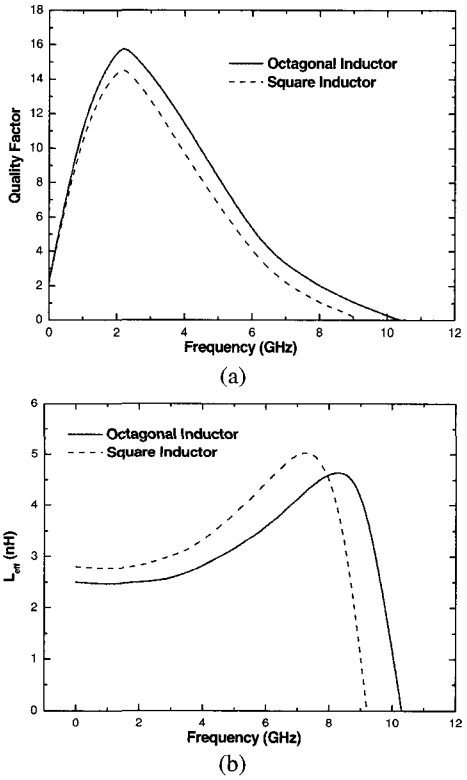


Fig. 30. (a) Q factor and (b) inductance of octagonal and square inductors having the same inner-diameter of 100 μm, number of turns of 3.5, and line width of 6 μm (after [52]).

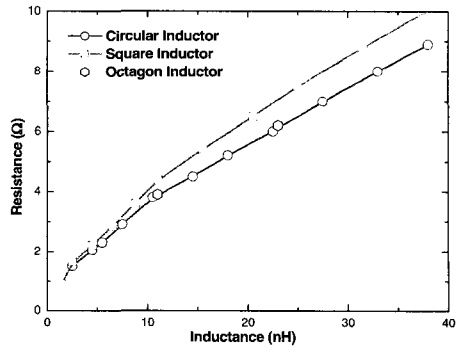


Fig. 31. Resistance vs. inductance characteristics of square, octagon and circular inductors operating at 1 GHz (after [8]).

IV. CONCLUSIONS

The dynamic growth in RF electronics has demanded and vitalized the need of high-performance on-chip passive components. One of these components, the on-chip spiral inductor, has been considered and reviewed in this paper. Many aspects of the design and modeling of the on-chip inductor have been presented, and their impacts on RF performance addressed. It is demonstrated that while it is cost effective and technology reliable to fabricate such devices on Si substrate, the conductive nature of Si material gives rise to a large substrate loss and consequently relatively poor RF performance. The spiral pattern and geometry can also be optimized to enhance the quality factor, but these alternatives often come with trade-offs or compromises. This work should provide a useful and sufficient breath to researchers and engineers who are interested in the design and development of RF IC's involving passive components.

Acknowledgements—The authors thank Dr. Yun Yue at Conexant Systems, Palm Bay, Florida for providing helpful information on spiral inductor modeling.

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