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Low Noise and High Linearity GaAs LNA MMIC with Novel Active Bias Circuit for LTE Applications

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Abstract

In this work, we demonstrated a low noise and high linearity low noise amplifier (LNA) monolithic microwave integrated circuit (MMIC) with novel active bias circuit for LTE applications. The device technology used in this work relies on a process involving a 0.25-μm GaAs pseudomorphic high electron mobility transistor (PHEMT). The LNA MMIC with a novel active bias circuit has a small signal gain of 19.7±1.5 dB and output third order intercept point (OIP3) of 38–39 dBm in the frequency range 1.75–2.65 GHz. The noise figure (NF) is less than 0.58 dB over the full bandwidth. Compared with the characteristics of the LNA MMIC without using the novel active bias circuit, the OIP3 is improved about 2–3 dBm. The small signal gain and NF showed no significant change after using the active bias circuit. The novel active bias circuit indeed improves the linearity performance of the LNA MMIC without degradation.

Index Terms: Active bias circuit, GaAs, Low noise amplifier, MMIC, PHEMT

I. INTRODUCTION

With the rapid development of wireless communication and multimedia applications, the mobile communication technology needs to accommodate increasing usage of mobile data and multimedia operations. In order to meet the demand for higher data rates and quality of service, Long Term Evolution (LTE) technology was specified by the 3rd Generation Partnership Project (3GPP) as the emerging mobile communication technology for the next generation broadband mobile wireless networks [1, 2]. The LTE system employs multiple carriers in order to achieve the high data rate and better spectral efficiency demanded [3]. This means that it is essential to maximize the dynamic range of the LTE system.

The low noise amplifier (LNA) is one of the most critical components in the LTE applications. The LNA serves as the first block of the receiver, and it needs to amplify the input signal without adding much noise and distortion. Due to the large interference signal from a corrupted carrier signal, LNA has to provide high linearity. The output power of the LNA causes degradation of the whole receiver sensitivity due to the inter-modulation characteristic. Several circuit techniques (such as predistortion and feedforward linearization) have been widely used for improving the linearity performance of the amplifier. However, these techniques involve complex methods requiring precise control of phase, and may require additional hardware that is not economically feasible to employ on a monolithic microwave integrated circuit (MMIC) [4, 5]. Other MMIC linearization techniques employ active and passive FET feedback [6]. However this feedback degrades the noise

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figure (NF) performance [7]. Many traditional linearization techniques are not feasible for LNA MMICs. Although the LNA techniques are well developed, the high linearity LNA MMIC is still a popular research topic [8]. In order to obtain high linearity, which is usually evaluated using the third order intermodulation intercept point (IP3); we proposed a novel active bias circuit. The proposed circuit is composed of a PHEMT-based diode, a capacitor, and an inductor as a linearizer. It improves the linearity performance without degradation of the LNA MMIC.

In this paper, we described a low-noise, high-linearity LNA MMIC with a novel active bias circuit, on a GaAs substrate in the frequency range 1.75–2.65 GHz. The design specification of the LNA MMIC was set as requested by RF-module companies for commercial products.

II. LNA MMIC DESIGN

The LNA MMIC with novel active bias circuit was designed using the 0.25 μm AlGaAs/InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) MMIC library by the Wireless Information Networking (WIN) Semiconductor foundry. The 0.25 μm PHEMT with a total gate width of 75 μm and eight gate fingers typically exhibits a cut-off frequency of 75 GHz and peak transconductance of around 600 mS/mm. The schematic diagram of the designed LNA MMIC with novel active bias circuit is shown in Fig. 1. The design strategy was optimized for simultaneous low noise and high linearity performance.

The proposed active bias circuit was composed of a PHEMT-based diode, an inductor, and a capacitor as a linearizer to improve the linearity. An inductor (L2) and capacitor (C2) connected in series were set to bypass unwanted frequency components using a choke inductor (L1) and a bypass capacitor (C1) connected in parallel at the DC bias feed line, which decreases third order intermodulation

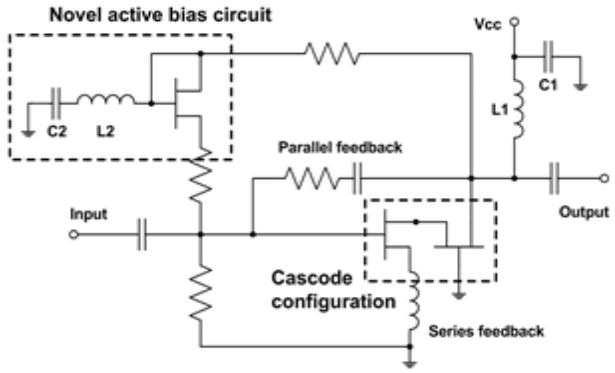

Fig. 1. Schematic diagram of the designed LNA MMIC with novel active bias circuit.

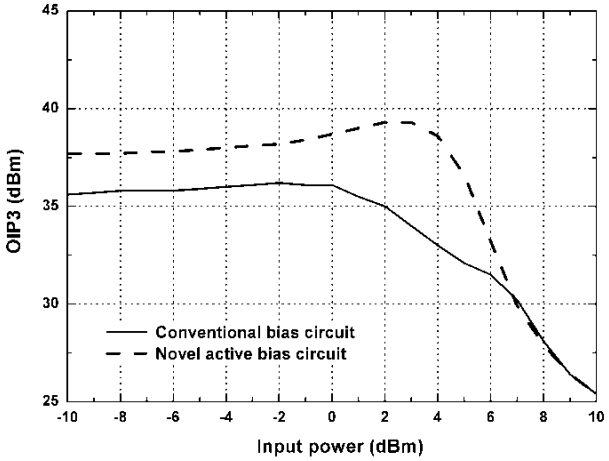

Fig. 2. Comparison of the OIP3 characteristics of the LNA MMIC at the center frequency of 2.2 GHz.

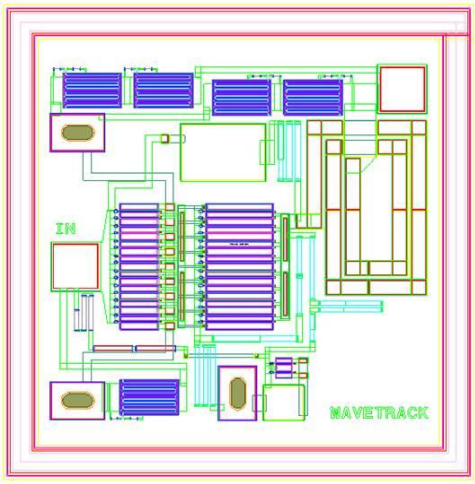

Fig. 3. Chip layout of the designed LNA MMIC with the novel active bias circuit.

(IM3) components from the PHEMT devices with cascode configuration. This characteristic should be used to improve the output IP3 (OIP3) performance of the LNA MMIC. Fig. 2 shows the comparison of the OIP3 characteristics of the LNA MMIC without using the novel active bias circuit at the center frequency of 2.2 GHz. The OIP3 was improved about 2–3 dBm.

In addition, the designed LNA MMIC also uses parallel feedback, which provides the advantages of increasing the stability factor, improving input and output return losses, and improving the flat gain characteristic over a wide bandwidth.

The circuit was simulated, and then refined electro-magnetically, using the Microwave Office (MWO) from the Advanced Wireless Revolution (AWR), in order to ensure minimum deviation between the model and the actual circuit layout. From the EM simulation results, the OIP3 of over 38

dBm, a NF of under 0.5 dB, and a small signal gain of over 18 dB were obtained in the frequency range 1.75–2.65 GHz. Fig. 3 shows the layout of the newly designed LNA MMIC with the novel active bias circuit. The chip dimensions were 0.60 mm × 0.65 mm.

III. MEASUREMENT RESULTS

Measurements of the fabricated LNA MMIC were performed on an evaluation board. The fabricated LNA MMIC was packaged in an industry standard Quad Flat No-lead (QFN) 3 mm × 3 mm plastic package. The inductance of the bonding wires at the input and output ports was considered during circuit simulation. An evaluation board including DC bias supply was designed and the packaged LNA MMIC was attached to the evaluation board. The K-type connectors and RO400C substrate 0.508 mm thick (provided by Rogers), was used to minimize signal loss and change of the 50-Ω line widths between the packaged LNA MMIC and RO400C substrate. A photograph of the packaged LNA MMIC and evaluation board is shown in Fig. 4.

Fig. 4. Photograph of the plastic DFN packaged LNA MMIC and evaluation board.

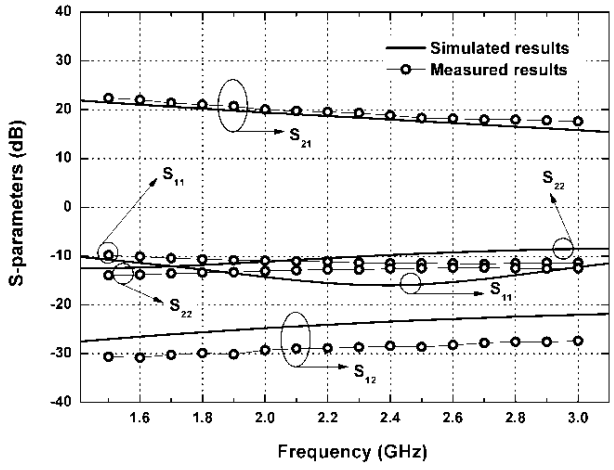

Fig. 5. Measured *S*-parameters of the packaged LNA MMIC.

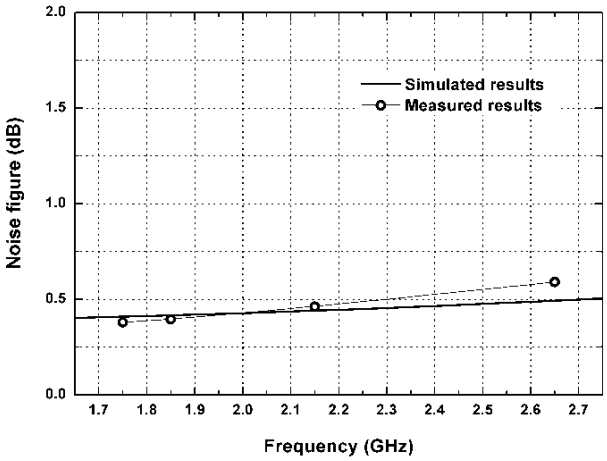

Fig. 6. Measured noise performance of the packaged LNA MMIC.

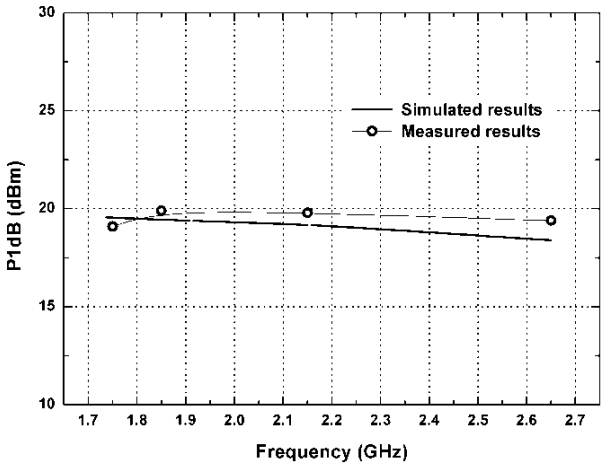

Fig. 7. Measured P1dB performance of the packaged LNA MMIC.

Typical *S*-parameters of the packaged LNA MMIC are shown in Fig. 5 at a bias condition of 5 V and 72 mA. The small signal gain (S_{21}) of 19.7±1.5 dB was obtained over the range 1.75–2.65 GHz. The input return loss (S_{11}) and the output return loss (S_{22}) were better than –10 dB over the entire frequency range. Good agreement between the measured and simulated *S*-parameters was achieved with minor influence from the packaging.

Fig. 6 shows the noise performance of the packaged LNA MMIC. From the measurement results, the NF was less than 0.58 dB over the full bandwidth under the same bias condition.

The frequency dependence of the linear output power, which was evaluated with a 1 dB compression point (P1dB), is shown in Fig. 7. At the drain bias of 5 V and 72 mA, a flat P1dB characteristic of 19.5±0.4 dBm was achieved over the bandwidth.

Two-tone linearity measurements with tone spacing of 1 MHz were performed under the bias condition of 5 V and 72

Table 1. The comparison of the LNA MMIC operating in similar bands with other reported data

Reference	[9]	[10]	[11]	[12]	[13]	This work
Device technology	GaN HEMT	GaAs PHEMT	GaN HEMT	GaAs PHEMT	GaAs PHEMT	GaAs PHEMT
Type	MMIC	MMIC	Package	Package	Package	Package
Frequency (GHz)	0.3–3.0	0.1–3.0	0.5–3.0	1.7–2.7	1.5–2.7	1.75–2.65
Gain (dB)	20.0±1.0	13.5±3.5	33.0±1.0	31.0±2.5	15.2±1.2	19.7±1.5
NF (dB)	<1.3	<3.3	<1.9	<1.2	<1.0	<0.58
P1dB (dBm)	30.5	-	22	24	23±2.0	19.5±0.5
OIP3 (dBm)	37–43	40–42.5	35–38	36–40	33–35.5	38–39

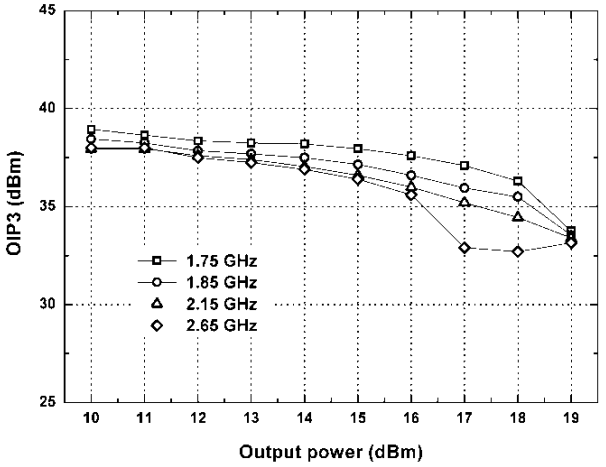

Fig. 8. Measured OIP3 characteristics of the packaged LNA MMIC.

mA. Fig. 8 shows the behavior of OIP3 versus frequency. The measurement data shows that the OIP3 was better than 38 dBm over the bandwidth in the output power range of <11 dBm.

Finally, Table 1 shows comparison of the results for the newly developed LNA MMIC with other reported data. The results from this work indicate the best performance demonstrated from a LNA MMIC employing GaAs-based HEMTs from 1.75–2.65 GHz, in terms of the NF, as well as the OIP3 characteristics.

The measurement results satisfied the design requirements of the LTE companies. The packaged LNA MMIC is expected to be applied for LTE applications as well as for cellular applications.

IV. CONCLUSION

In this paper, we reported our demonstration of a low noise and high linearity LNA MMIC with novel active bias circuit for LTE applications. The device technology used relies on a 0.25-μm GaAs PHEMT process. The LNA MMIC with novel active bias circuit has the small signal gain of 19.7±1.5 dB and the OIP3 of 38–39 dBm in the frequency range 1.75–2.65 GHz. The NF is less than 0.58 dB over the full bandwidth. Compared with the characteristics of the LNA MMIC without using the novel active bias circuit, the OIP3 was improved about 2–3 dBm. The small signal gain and NF showed no significant change after using the active bias circuit. The packaged LNA MMIC is expected to be applied for LTE applications as well as for cellular applications.

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